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SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION THEREOF

The present invention relates to a semiconductor device having two circuits on the same semiconductor substrate and to a method of fabrication of such a circuit.

Miniaturisation of semiconductor devices (ICs) has been attempted to increase their operating speed and improve their integration density. MOS elements (MOSFETs), which are typical examples of MIS elements (MISFETs), are no exception. To miniaturise MOS elements, the thickness of their gate oxide films has been reduced and the length of their channels has become shorter and shorter. This means that a relatively strong electric field is generated within the device, so that injection of hot carriers into the gate oxide film occurs, and the threshold voltage shifts or there is a degradation of mutual conductance.

A double-diffused drain structure such as that shown in Figure 1 of the accompanying drawings has been proposed to solve these problems. Figure 1 is a section through a typical N-channel MOSFET. A P-type silicon semiconductor substrate 1 has a silicon dioxide (SiO_2) film 2, a gate oxide film 3 and a gate electrode 4 formed thereon. In order to reduce the strong electric field in the proximity of the drain, both drain and source have a double-diffused drain structure consisting of an N^--type layer 5 of phosphorous (P) and an N^+-type layer 6 of

arsenic (As) (refer for example to the aricle by E. Takeda, et al, entitled "An As-P (N+-N) Double Diffused Drain MOSFET for VLSI's", published in the Digest of Technical Papers, Symp. on VLSI Technology, OISO, Japan, pp. 40-41 (Sept. 1982)).

A protective circuit is usually formed on the same semiconductor substrate to protect the MIS element from abnormal signals from outside the IC. As shown in Figure 12 of the accompanying drawings, the protective circuit (e.g., electrostatic protective circuit) is a circuit to prevent the destruction of the gate insulating film of a MISFET 71 of a first stage inverter 68, the gate electrode of which is connected to a bonding pad 8 through a resistor 10. Destruction occurs when electrostatic energy is applied to the bonding pad.

A circuit such as that represented by the equivalent circuit diagram of Figure 2 of the accompanying drawings is a typical protective circuit 9 used for protecting circuits other than the protective circuit, e.g. an internal circuit of an IC. A signal to the internal circuit is applied to a bonding pad 8 through a diffusion resistor 10, one end of which is connected to the pad 8, and a clamping MOSFET 11 whose gate and source are earthed is connected to the junction between the resistor 10 and the internal circuit.

The inventors of the present invention have produced sample semiconductor devices of a double-diffused drain structure, and have discovered the following problem.

In this semiconductor device, the protective circuit 9 has also a double-diffused drain structure. A section through the circuit 9 is shown in Figure 3 of the accompanying drawings. A P-type silicon semiconductor substrate 12, has an isolation SiO_2 film 13, a resistor 10, a clamping MOSFET 11, a source region 14, a gate oxide film 15, a gate electrode 16, a phosphosilicate glass (PSG) film 17 and 18 an aluminium electrode formed thereon. Both the diffused resistor 10 and the semiconductor regions of the source and drain regions of the clamping MOSFET 11 have a double-diffused drain structure, and consist of an N^+-type layer and an N^--type layer.

In the semiconductor device of this kind, however, destruction of the insulating film of a MISFET forming a first stage inverter and having a double-diffused drain tends to occur. This is because the backward breakdown voltage at the junction of a MISFET (Diode) and having a double-diffused drain rises, the electrostatic energy is applied to the insulating film before it can leak to a substrate by breakdown of the clamping MISFET.

The present invention seeks to overcome, or at least ameliorate these problems, by forming a first circuit, e.g. an internal circuit such as a memory cell, with a double-diffused drain structure, and a second circuit, e.g. the protective circuit, with a single-diffused drain structure. The second circuit may be an electrostatic protective circuit which, as mentioned above, protects the

region of the at least one MISFET comprising a first doped region of high concentration and a second doped region of relatively low concentration of the same conductivity type as the first doped region, and in contact with the first doped region, wherein a protective element of a second circuit electrically connected to the first circuit for protecting the first circuit from an external surge voltage introduced through an external terminal, has a doped region of a high concentration substantially the same as the first doped region and of the same conductivity type and no region having a concentration and conductivity type substantially the same as the second doped region and which is in contact with the region of high concentration of the protective element, wherein the region of high concentration of the protective element is formed simultaneously with the first doped region, and wherein the second doped region is formed in self-alignment with the gate electrode, and the first doped region is formed in self-alignment with one of the side wall spacers and the gate electrode. The second circuit may be an electrostatic protective circuit which, as mentioned above, protects the first circuit from damage due to abnormal external signals. Such a device reduces degradation of characteristics due to hot carriers, and also reduces degradation of the destruction voltage. In this way the field intensity acting upon the gate oxide film of e.g. a clamping MOSFET may be reduced.

The present invention also provides, in a second

aspect a method of fabricating a semiconductor device having at least one MISFET for a first circuit, the at least one MISFET having a diffused drain region and a gate electrode with side wall spacers on either side of the gate electrode and a protective element of a second circuit electrically connected to the first circuit for protecting the first circuit from an external surge voltage introduced through an external terminal, the first and second circuits being formed in a major surface of a semiconductor substrate; the method including; forming by diffusion first and second doped regions for the drain region of the at least one MISFET, the first doped region being of high concentration and being formed in self-alignment with one of the side wall spacers and the gate electrode, and the second doped region being of relatively low concentration, of the same conductivity type as the first doped region, being in contact with the first doped region, and being formed in self-alignment with the gate electrode; and forming by diffusion a doped region of the protective element, the doped region being formed simulataneously with the first doped region and having a high concentration substantially the same as the first doped region;

wherein no region of the protective element is formed which has a concentration and conductivity type substantially the same as the second doped region and which is in contact with the region of high concentration of the protective element.

The two diffusion layers of the first circuit may be formed either by first masking the second circuit for the formation of the first diffusion layer, and then removing the mask, or by selective ion implantation scanning.

An embodiment of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a section through an N-channel MIS element with a double-diffused drain structure and has already been described;

Figure 2 is an electric equivalent circuit diagram of an example of an electrostatic protective circuit and has already been described;

Figure 3 is a section through a device corresponding to the equivalent circuit of Figure 2 and has already been described;

Figure 4 is a plan view of an example of the chip pattern of a DRAM provided with an electrostatic protective circuit and an internal circuit on the same semiconductor substrate;

Figures 5 to 8 are sections through a semiconductor device, showing the fabrication method useful in understanding the present invention;

Figures 9 and 10 are schematic plan views corresponding to the electrostatic protective circuit and the internal circuit of Figure 8, respectively;

Figure 11 is a graph of experimental results showing

the dielectric breakdown voltage of an electrostatic protective circuit with a single-diffused drain structure, compared with that of an electrostatic protective circuit with a double-diffused drain structure;

Figure 12 is a circuit diagram showing an electrostatic protective circuit and a specific internal circuit protected thereby;

Figures 13 and 14 are respectively circuit diagrams showing the present invention applied to a MISFET composing a first stage of an input buffer and a MISFET composing a final stage of an output buffer;

Figures 15, 16, and 17 show circuit diagrams of CMISICS useful in understanding the present invention;

Figure 18 is a cross-sectional view of part of the circuit of Figure 15 according to a first arrangement not being an embodiment of the present invention; and

Figure 19 is a cross-sectional view of part of the circuit of Figure 15 according to an embodiment of the present invention.

A first embodiment of a semiconductor device and a method of fabricating it in accordance with the present invention will now be described with reference to Figures 4 to 10. However, such description exemplifies, not limits the invention.

Figure 4 shows an example of the layout of a chip 7 of a dynamic random access memory (DRAM). The DRAM consists of bonding pads 8, a protective circuit 9 provided for each

bonding pad 8, a signal generation circuit 100 which generates read and write timing signals, etc., a memory array 101 in which MIS elements are used as memory cells, and column and row decoders 102.

Figures 5 to 8 are cross-sectional views showing, step-by-step, the process of fabricating a semiconductor device useful in understanding the present invention. The protective circuit is shown on the left of each drawing and a memory cell, which is part of the internal circuit, is shown on the right. Figure 8 is a section through a completed semiconductor device, and Figures 9 and 10 are schematic plan views of the semiconductor device of Figure 8.

Figure 5 shows the state in which the process has been completed up to the formation of the gate electrode of the MOSFET of the DRAM. This state may be completed by

conventional techniques shown in Figure 5 are a semiconductor substrate 20, a gate oxide film 21, and a gate electrode 22. The semiconductor substrate 20 is, e.g., a P-type monocrystalline silicon substrate having a (100) crystal plane, for example, and the gate oxide film 21 is an SiO_2 film, for example. The gate electrode 22 is a conductive layer forming a second layer, and is formed by depositing polycrystalline silicon by chemical vapour deposition (CVD), and then diffusing e.g. phosphorus ions to form polycrystalline silicon of a reduced resistance. The gate electrode may consist of a layer of a metal which has a high melting point, a layer of the silicide of such a metal, or a two-layered structure consisting of polycrystalline silicon and the silicide of a metal with a high melting point. The circuit shown in Figure 2 illustrates an example of the protective circuit on the left of Figure 5, and the memory cell of the DRAM is shown as one example of an internal circuit on the right of Figure 5.

A thick oxide film 23 providing isolation is formed by selective thermal oxidation of the surface of the silicon substrate 20, for example. A silicon nitride (Si_3N_4) film 25 acting as a dielectric film of a storage capacitor is formed on the surface of the field oxide film 23 on the memory cell side, and also on the surface of a thin SiO_2 film 24 that continues from the film 23. A polycrystalline silicon electrode 27 is formed on the thin film 25 through

an SiO_2 film 26 and is diffused with e.g. phosphorus ions so as to reduce its resistance. The conductive layer which is the first layer consisting of this polycrystalline silicon electrode 27 forms one of the electrodes of the capacitor of the memory cell. Ion implantation for an inversion prevention layer (that is, a channel stopper layer), or for controlling the threshold voltage, etc., has already been completed by this stage.

Next, as shown in Figure 6, a photoresist film 28 is selectively formed over the surface of the protective circuit alone, by a photolithographic process. More specifically, the photoresist film 28 (1 μm) is formed only over the region A in Figure 4. Ion implantation is then effected using this photoresist film 28 as a mask, in order to form N^--type diffusion layers 29 which act as source and drain regions in the memory cell. This ion implantation uses phosphorus ions as the N-type impurity, for example. The impurity dose is $1 \times 10^{14}/cm^2$ and the implantation energy is 50 KeV. Arsenic ions can be used as the impurity.

Referring to Figure 7, the photoresist film 28 is removed, and then N-type impurity ions such as arsenic ions are implanted to form an N^+-type layer 30, and hence a double-diffused drain structure. This ion implantation also forms a diffusion resistance layer 31 of the protective circuit, as well as a source-drain region 32 of the clamping MOSFET. The impurity dose is $8 \times 10^{15}/cm^2$ and the

implantation energy is 80 KeV. Phosphorus ions can be used as the impurity.

As can be appreciated, the diffusion resistor can be formed from a polysilicon layer, e.g., formed over the semiconductor substrate.

As can be seen from Figures 6 and 7, the protective circuit has a single-diffused drain structure while the internal circuit (memory cell) has a double-diffused drain structure. In this case, the photoresist film 28 is selectively formed to prevent the implantation of the N^--type phosphorus ions into the protective circuit. However, the implantation of phosphorus ions into the protective circuit can also be prevented by controlling the scanning of the ion implantation (by avoiding scanning of the region including the protective circuit, i.e., region A in Figure 4). This is relatively easy because the electrostatic protective circuit is usually formed in a certain region around the periphery of the chip, as shown in Figure 4, and so inhibit the ion implantation may be limited by avoiding scanning this region.

After the electrostatic protective circuit of the single-diffused drain structure and the internal circuit of the double-diffused drain structure have thus been formed, a phosphosilicate glass film (PSG film) 33 and an aluminium layer acting as a third conductive layer are formed as shown in Figure 8. The aluminium layer acts as an output electrode 34 for the diffusion resistor 31, an

output electrode 35 for the internal circuit, a source electrode 36, and a data line 37 of the memory cell. After the PSG film 33 is formed, photoetching is used to form contact holes for these electrodes, and aluminium sputtering is done to form the electrodes. Finally, a PSG film 38 is formed as a protective film.

Figures 9 and 10 are schematic plan views of the electrostatic protective circuit and internal circuit of Figure 8, respectively. A section along the line B - B of Figure 9 and a section along the line C - C of Figure 10 correspond to the protective circuit region and the internal circuit region of Figure 8, respectively.

In Figure 9 is shown a bonding pad 40, a diffusion layer 41 for an input portion, a contact hole 42, and a diffused resistor 43. Also shown is a clamping MOSFET 44 which consists of a region 45 connected electrically to the diffused resistor 43, a gate electrode 46 and a source 47. The region 45 is connected to an aluminium signal line 45B through contacts 45A, and the aluminium signal line 45B is electrically connected to the internal circuit. Similarly, the source 47 is connected to an aluminium line 47B through contacts 47A, and one end of the aluminium line 47B is connected to the gate electrode through a contact 48, with the other end earthed.

In Figure 10, a boundary line 50 of the field oxide film defines the active region of the memory cell, and a polycrystalline silicon word line 51 corresponds to the

gate electrode of the MOSFET. Polycrystalline silicon 52 acts as one of the electrodes of the capacitor of the memory cell, and an aluminium electrode 53 is wired to a contact hole 54 of the data line.

Figure 11 is a graph of typical experimental data comparing the electrostatic destruction voltage of a protective circuit with a single-diffused drain structure and that of a protective circuit with the double-diffused drain structure. The percentage accumulative defect ratio is shown along the ordinate, and the electrostatic destruction voltage (V) along the abscissa. The segmented line a denotes the data from devices having a double-diffused drain structure, and the segmented line b data from the devices having a single-diffused drain structure. The voltage resistance of the same pin of five samples was examined. It can be seen from the graph that a protective circuit with a single-diffused drain structure exhibits a much better electrostatic destruction voltage.

As described above, since the protective circuit has a single-diffused drain structure and the internal circuit has a double-diffused drain structure, the electric field concentration in the internal circuit and the electric field concentration in the gate oxide film of the first stage MISFET of the internal circuit can be reduced, ameliorating the problems of hot carriers and of destruction voltage.

Since a mask is applied to the protective circuit

to prevent the formation of one of the diffusion layers of the double-diffused drain, the semiconductor device of this invention can be easily fabricated by adding only one photolithographic step.

Alternatively a method may be used of locally controlling the ion implantation scanning to avoid the protective circuit.

The protective circuit described above consists of one diffused resistor and one clamping MOSFET, but this is not necessary and protective circuits may utilize the junction breakdown in a diffusion layer and the surface breakdown at the drain end of a clamping MOSFET to improve the dielectric breakdown voltage may be used. Moreover, the clamping MOSFET can be replaced by one or two junction diodes. In this case, the junction of the diode is between the P-type substrate and the N^+-type layer formed simultaneously with the N^+-type layers 30, 31 and 32.

Similarly, a DRAM has been described as an example of the internal circuit, but the internal circuit is not limited to a DRAM, and other circuits provided with MIS elements may be used which have at least a double-diffused drain structure. Thus, the MISFET may have a single-diffused drain structure, applied to a MISFET forming the first stage of an input buffer or to a MISFET forming a final stage of an output buffer. Circuit diagrams for such MISFETs having the single-diffused structure, applied to the MISFET forming the first stage of an input buffer and the

MISFET forming the final stage of an output buffer are shown in Figures 13 and 14. In Figures 13 and 14, respectively, there are shown an input pad 81 and an output pad 82, and the structure within dotted lines 83,84 represents the single-diffused drain structure.

Moreover, N-channel MISFETs of a CMISIC, where N-channel MOSFETs are formed in a P-well region or a P-substrate may be used.

Figures 15,16 and 17 show the circuit diagrams for such a CMISIC. The structure within dotted lines 85,86 and 87 has a single-diffused drain structure. The structures of the MISFETs 88,89 and 90 in Figure 15 are shown in more detail in Figure 18. The N-channel MISFET 89 has a double-diffused drain structure with an N^+-type layer 58 and N^--type layer 59, which are formed in a P^--type substrate 56. P^+-type regions 61 act as source and drain regions of the P-channel MISFET 90 formed in an N^--type well region 57. The MISFET 88 has a single diffused drain structure with an N^+-type layer 60 formed in the substrate 56. A diode 91 has a same structure as the MISFET 88. Junction diodes 93,94 (Figure 16) 96 and 97 (Figure 17) are formed between a P-type substrate and N^+-type layers such as the N^+-type layers 60 shown in Figure 18. The N^+-type layers 60 are drains of MISFETs and are formed simultaneously. If a resistor 92 is made of an N^+-type layer, e.g. simultaneously with layers 60, the diode 94 can be formed parasitically between the resistor 92 and the P-type substrate 56.

In the present invention, however, the N-channel MISFETs 91 have the structure shown in Figure 19. The source and/or drain region of the MISFET 91 is formed by an N^--type layer 64 formed in self-alignment with a gate electrode 65 and an N^+-type layer 63 formed in self-alignment with a side wall spacer 62 and the gate electrode 65. The MISFET 91 replaces the MISFET 89, for example.

Thus, while the foregoing description has been directed to a DRAM and its protective circuit, the present invention may be applied to ordinary MOS integrated circuits such as DRAMS (e.g., 256 K bits DRAMS), SRAMs, MOS logic circuits, and so forth.

This application has been divided out of UK Patent Application No. 84.32417 (published under No. 2152284) and describes matter also described in that application. Attention is therefore drawn to UK Patent Application No. 84.32417.

CLAIMS:

1. A semiconductor integrated circuit device, formed in a major surface of a semiconductor substrate, having at least one MISFET for a first circuit, the at least one MISFET having a diffused drain region, and a gate electrode with side wall spacers on either side of the gate electrode, each drain region of the at least one MISFET comprising a first doped region of high concentration and a second doped region of relatively low concentration of the same conductivity type as the first doped region, and in contact with the first doped region, wherein a protective element of a second circuit electrically connected to the first circuit for protecting the first circuit from an external surge voltage introduced through an external terminal, has a doped region of a high concentration substantially the same as the first doped region and of the same conductivity type and no region having a concentration and conductivity type substantially the same as the second doped region and which is in contact with the region of high concentration of the protective element, wherein the region of high concentration of the protective element is formed simultaneously with the first doped region, and wherein the second doped region is formed in self-alignment with the gate electrode, and the first doped region is formed in self-alignment with one of the side wall spacers and the gate electrode.

2. A semiconductor device according to claim 1, wherein the first circuit is an internal circuit, and the second

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circuit is an electrostatic protective circuit.

3. A semiconductor device according to claim 2, wherein the electrostatic protective circuit includes at least one diffused resistor and at least one clamping MIS element.

4. A semiconductor device according to claim 3, wherein the diffused resistor has a high concentration substantially the same as the first doped region and no region which has a conductivity type and concentration substantially the same as the second doped region.

5. A semiconductor device according to claim 3 or claim 4 having an input bonding pad, the resistor being electrically connected to the internal circuit and to the bonding pad.

6. A semiconductor device according to any one of claims 2 to 5, wherein the internal circuit has a dynamic RAM element.

7. A semiconductor device substantially as herein described with reference to and as illustrated in Fig. 19.

8. A method of fabricating a semiconductor device having at least one MISFET for a first circuit, the at least one MISFET having a diffused drain region and a gate electrode with side wall spacers on either side of the gate electrode and a protective element of a second circuit electrically connected to the first circuit for protecting the first circuit from an external surge voltage introduced through an external terminal, the first and second circuits being formed in a major surface of a semiconductor substrate;

the method including;

forming by diffusion first and second doped regions for the drain region of the at least one MISFET, the first doped region being of high concentration and being formed in self-alignment with one of the side wall spacers and the gate electrode, and the second doped region being of relatively low concentration, of the same conductivity type as the first doped region, being in contact with the first doped region, and being formed in self-alignment with the gate electrode; and forming by diffusion a doped region of the protective element, the doped region being formed simulataneously with the first doped region and having a high concentration substantially the same as the first doped region;

wherein no region of the protective element is formed which has a concentration and conductivity type substantially the same as the second doped region and which is in contact with the region of high concentration of the protective element.

9. A method according to claim 8, wherein a mask is formed over the second circuit prior to the formation of the second doped region, and the mask is removed after the formation of the second doped region but before the formation of the first doped region.

10. A method according to claim 9, wherein said mask is made from a photoresist film.

11. A method according to claim 8, wherein the second diffused region is formed by ion implantation scanning over

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only the first circuit, and the first diffused region and the region of high concentration of the protective element are formed by ion implantation scanning over the entire surface of the device.

12. A method according to any one of claims 8 to 11 wherein the first circuit is an internal circuit, and second circuit is an electrostatic protective circuit.

13. A method according to any one of claims 8 to 12, wherein the first and second doped regions, and the doped region of high concentration of the protective element, are each formed by ion implantation.

14. A method according to claim 13, wherein the second doped region is an N^- layer formed by ion implantation of phosphorous ions, and the first doped region and the region of high concentration of the protective element are N^+ layers formed by ion implantation of arsenic ions.

15. A method according to any one of claims 8 to 14, wherein the electrostatic protective circuit is positioned at a peripheral portion of the semiconductor substrate in an offset arrangement.