Description

The invention relates to a data processing system comprising a memory for buffering sequential data units for the duration of cyclically recurrent delay lengths.

The invention likewise relates to selecting means for generating a periodic sequence of time slots having lengths corresponding with the delay lengths for each one of at least two memory locations, suitable for use in such a system. A data processing system of the type mentioned in the opening paragraph is known from "Efficient Code Generation for Horizontal Architectures: Compiler Techniques and Architectural Support", by Rau et al., 9th Annual Symposium on Computer Architecture, Austin, 1982, pp. 131-139. This literature also extensively discusses a field of application namely parallel and iterative data processing. In this kind of data processing new streams are created from various parallel streams of sequential data units. Before allowing the data units of the new streams to undergo processes again, these data units are to be delayed with respect to one another in order to be in a position to combine them with one another at the proper instant and in the proper manner. Since the series of operations is repeated cyclically, the delay of data units is effected by means of a temporary storage in a memory for the duration of cyclically recurrent delay times. Buffering the data units in the prior-art data processing system is effected with the aid of compacting means. These compacting means provide that, if so desired, after a data unit has been read out from one of the memory locations, the remaining stored data units can be rearranged over logically linked memory locations. When a new data unit is written, it is written into an unoccupied memory location having an address which is as near as possible to an address of the occupied memory locations. This rearranging of the data units, as well as the updating of the address of the nearest unoccupied memory location leads to an efficient use of the available memory locations, admittedly, but requires a considerable amount of hardware.

Therefore, it is an object of the invention to provide a data processing system in which the available memory locations are utilized substantially as efficiently as done according to the state of the art while utilizing less hardware. For this purpose, a data processing system according to the invention is characterized in that selecting means are provided for generating, for each one of at least two memory locations, a periodic sequence of time slots having lengths corresponding to the delay lengths, each time slot for a memory location beginning with a write phase for the relevant data unit and ending in a read phase, in which read phase the relevant data unit is read for the last time, and in which sequence a sequence period includes a permutation of the time slots whose lengths correspond to the cyclically recurrent delay lengths, in which permutation the read phase of the preceding time slot is followed by a next-sequentially possible write phase of a further time slot, and a mutual shift between the sequences at consecutive memory locations amounts to a single cycle, and the period is equal to a sum of the mutual shifts.

A data occupation attained thus with the selecting means provides an efficient utilization of memory locations without rearrangements and without the hardware required for the rearrangements. No larger number of memory locations are required than the number of consecutive cycles in which the period of the sequence of time slots can be fitted. The period itself contains a permutation of time slots organised according to a first-fit algorithm, which time slots correspond with the delay lengths assigned per cycle. As a result of the mutual shift between the various occupied memory locations the joint memory locations have a time slot occupation per cycle which corresponds with the time slot occupation of the period.

An embodiment of a data processing system according to the invention is characterized, in that the selecting means include reference means for generating a next reference value at the start of each next cycle of delay lengths, a sequence of reference values being recurrent with a period of the sequence of time slots, and also include first and second combining means respectively, for generating for the memory read and write addresses respectively, by means of linearly combining cyclically recurrent first and second increments respectively, with a current reference value. The read and write addresses are determined per cycle, relative to the reference value. Since the reference value leaps at the start of a next cycle, the read and write addresses will leap as well relative to those from the previous cycle. After the number of cycles, covering a period, the read and write addresses will repeat again.

A further embodiment of a data processing system according to the invention is characterized in that the reference means include a modulo counter whose count represents the current reference value. This provides a simple manner to produce periodic reference values. A still further embodiment of a data processing system according to the invention is characterized in that a leap between sequential reference values is adjustable and also the said increments are adjustable. The adjustability of the reference value and the increments renders the system suitable for use in more than one application.

Another embodiment of a data processing system according to the invention is characterized in that the selecting means include third and fourth combining means respectively, for consecutively generating first and second addresses for the memory, respectively, by consecutively linearly combining a cyclically recurrent third and fourth increment respectively, with a preceding first address, the first address respectively, the first and the second addresses being either the write addresses and the read addresses or the read addresses and the write addresses. With a suitable choice of the increments to be fed to the combining means, this arrangement saves a modulo counter when compared to one of the embodiments mentioned hereinbefore.

The invention will be illustrated with reference to a drawing Figure in which:

Fig. 1 shows a block diagram of a data processing system of the above type,

Fig. 2 shows an example of the way in which data occupation is created on memory locations in the prior art data processing system,

Fig. 3 shows an example of the way in which data occupation is created on memory locations in a data processing system according to the invention,

Fig. 4 shows a first implementation of a memory having selecting means in a data processing system according to the invention, and

Fig. 5 shows a second implementation of a memory having selecting means in a data processing system according to the invention.

Fig. 1 shows in a block diagram an example of a data processing system of the aforementioned type. The example shows a data processing element 10 having data outputs 11 and 12 which are linked via data output lines 13 and 14 and data input lines 15 and 16 to data inputs 17 and 18. The link is provided by an interconnecting network 19 in which junction elements 20, 21, 22 and 23 are provided at the junctions of a data output line and a data input line. These junction elements are instrumental in distributing data units from the various streams fed via output lines 13 and 14 over the input lines before the data are subjected to a new process in element 10. In order to combine data units that are not simultaneously available on the data output lines, the junction elements comprise memory locations for buffering data units for the duration of predetermined periods of time. Because the data units are subjected to a cyclic sequence of processes, these periods of time are also cyclically recurrent.

Fig. 2 shows an example of the way in which data occupation is created of memory locations of the prior art data processing system. In a five-phase cycle, having the phases 0, 1, 2, 3 and 4, data units are buffered at memory locations having addresses 0, 1, 2 and 3. The phases (ph) are plotted horizontally, the addresses of the memory locations (ma) vertically. In phases 0, 1, 3 and 4 of a cycle, data units are written which are buffered for the duration of 6, 1, 2 and 5 phases, respectively. Reading out these data units is then effected in phase 1 of the next cycle, phase 2 of the same cycle, phase 0 of the next cycle and phase 4 of the next cycle. The data units having write phases 0, 1 and 4 are all written in the memory location having the address 3. The data unit of the write phase 3 is written in memory location 2. As soon as a memory location of a lower address falls vacant, the data units at memory locations of a higher address are transferred to this lower address. Admittedly, this will lead to an efficient use of the available memory locations, but on the other hand requires a considerable amount of logic for monitoring the logically nearest unoccupied memory location and for rearranging the data units among the memory locations.

Fig. 3 shows an example of the way in which data occupation is created on memory locations in a data processing system in accordance with the invention. The cycle which was used for the previous Figure is used here too. Now, a data occupation per memory location is attained which is periodic and has a period of four cycles in each one of the time slots, which time slots correspond to the dedicated delay lengths per cycle. Memory location 0 is occupied by a first data unit for 6 consecutive phases. After this memory location is read, the next, second data unit is written into the same memory location with a write phase which is the earliest in succession to the read phase of the first data unit and of which a delay length has not yet been included in the said period. This will then be the data unit having write phase 3 and read phase 0 of a next cycle. The same selection criteria apply for the data units having write phases 1 and 4. The illustrated time slot permutation will realise the shortest period length. Corresponding data occupations are realised at memory locations 1, 2 and 3. The data occcupations at the memory locations are shifted relative to one another by one cycle. The data occupation provided in this example requires as many memory locations as the data occupation which was discussed with reference to Fig. 2, but requires considerably less hardware because rearrangements of the data units over the memory locations are avoided. For clarity, the above examples are restricted to cycles of four different delay lengths. The advantages of a data processing system according to the invention already present themselves as being non-trivial when, in one cycle, three data units are buffered and are evident when, in one cycle, a large number

(for example: twenty) of data units are buffered.

Fig. 4 represents a first implementation of a memory having selecting means in a data processing system in accordance with the invention. A memory 30 is shown having memory locations for buffering sequential data units. The incoming data stream is designated by reference numeral 32, the outgoing data stream by reference numeral 34. Through input 36, 38 respectively, write addresses and read addresses, respectively, of the memory are addressed. The periodicity per memory location and the mutual shift in the sequences are realised by a modulo counter 40 whose contents leaps per cycle by a predetermined value, induced by a trigger pulse on input terminal 42 preceding a next cycle. Thereto, for each cycle a fixed leap value is added to the current count. An output signal at output terminal 46 then represents a reference value leaping by a fixed step per cycle. This reference value is fed to adding circuits 48 and 50. Adding circuit 48 receives the cyclic first increments and adding circuit 50 to the cyclic second increments via terminals 52 and 54, respectively. These circuits furnish the current write address and the actual read address of a memory location in memory 30 by adding said increments to the current reference value. It will be readily understood that a modulo counter having the counts 0, 1, 2 and 3 is suitable for the example discussed with reference to Fig. 3, while per cycle a fixed step equal to the number one is subtracted from the current count value representing the current reference value.

Fig. 5 represents a second implementation of a memory having selecting means in a data processing system in accordance with the invention. The elements corresponding with those in Fig. 4 are designated by the same reference numerals. The selecting means now include a first and a second adding circuit 60 and 62 respectively, as well as a memory element 64 which is inserted between the output 66 and the first input 68 of adding circuit 60. The second input 70 of adding circuit 60 receives sequential, cyclically recurrent third increments. The current third increment is added to the content of the memory element 64. The sum represents the next write address. The sum is also applied to a first input of the second adding circuit 62, to a second input 72 of which sequential, cyclically recurrent fourth increments are applied. The sum furnished by the second adding circuit then represents the next read address.

The selecting means, parts of which are represented in Figs. 4 and 5, may be restricted to embodiments in which each time no more than one single address is applied to the memory. However, means will then be provided indeed for establishing whether the address provided is a read address or a write address. The disadvantage that reading and writing are mutually exclusive per operation, during which the address is provided, will then be offset by the advantage that a relatively low-speed memory can be used.

Claims

1. A data processing system comprising a memory (30) for buffering sequential data units for the duration of cyclically recurrent delay lengths, characterized in that selecting means (40, 48, 50) are provided for generating, for each one of at least two memory locations, a periodic sequence of time slots having lengths corresponding to the delay lengths, each time slot for a memory location beginning with a write phase for the relevant data unit and ending in a read phase, in which read phase the relevant data unit is read for the last time, and in which sequence a sequence period includes a permutation of the time slots that correspond to the cyclically recurrent delay lengths, in which permutation the read phase of the preceding time slot is followed by a next-sequentially possible write phase of a further time slot, and a mutual shift between the sequences of consecutive memory locations amounts to a single cycle, and the period is equal to a sum of the mutual shifts.

2. A data processing system as claimed in Claim 1, characterized in that the selecting means (40, 48, 50) include reference means for generating a next reference value at the start of each next cycle of delay lengths, a sequence of reference values being recurrent with a period of the sequence of time slots, and also include first (48) and second (50) combining means respectively, for generating for the memory read and write addresses respectively, by linearly combining cyclically recurrent first and second increments respectively, with a current reference value.

3. A data processing system as claimed in Claim 2, characterized in that the reference means include a modulo counter (40) whose count represents the current reference value.

4. A data processing system as claimed in Claim 2 or 3, characterized in that a leap between sequential reference values is adjustable.

5. A data processing system as claimed in Claim 1 characterized in that the selecting means include third (60) and fourth (62) combining means respectively, for consecutively generat-

(for example: twenty) of data units are buffered.

Fig. 4 represents a first implementation of a memory having selecting means in a data processing system in accordance with the invention. A memory 30 is shown having memory locations for buffering sequential data units. The incoming data stream is designated by reference numeral 32, the outgoing data stream by reference numeral 34. Through input 36, 38 respectively, write addresses and read addresses, respectively, of the memory are addressed. The periodicity per memory location and the mutual shift in the sequences are realised by a modulo counter 40 whose contents leaps per cycle by a predetermined value, induced by a trigger pulse on input terminal 42 preceding a next cycle. Thereto, for each cycle a fixed leap value is added to the current count. An output signal at output terminal 46 then represents a reference value leaping by a fixed step per cycle. This reference value is fed to adding circuits 48 and 50. Adding circuit 48 receives the cyclic first increments and adding circuit 50 to the cyclic second increments via terminals 52 and 54, respectively. These circuits furnish the current write address and the actual read address of a memory location in memory 30 by adding said increments to the current reference value. It will be readily understood that a modulo counter having the counts 0, 1, 2 and 3 is suitable for the example discussed with reference to Fig. 3, while per cycle a fixed step equal to the number one is subtracted from the current count value representing the current reference value.

Fig. 5 represents a second implementation of a memory having selecting means in a data processing system in accordance with the invention. The elements corresponding with those in Fig. 4 are designated by the same reference numerals. The selecting means now include a first and a second adding circuit 60 and 62 respectively, as well as a memory element 64 which is inserted between the output 66 and the first input 68 of adding circuit 60. The second input 70 of adding circuit 60 receives sequential, cyclically recurrent third increments. The current third increment is added to the content of the memory element 64. The sum represents the next write address. The sum is also applied to a first input of the second adding circuit 62, to a second input 72 of which sequential, cyclically recurrent fourth increments are applied. The sum furnished by the second adding circuit then represents the next read address.

The selecting means, parts of which are represented in Figs. 4 and 5, may be restricted to embodiments in which each time no more than one single address is applied to the memory. However, means will then be provided indeed for establishing whether the address provided is a read address or a write address. The disadvantage that reading and writing are mutually exclusive per operation, during which the address is provided, will then be offset by the advantage that a relatively low-speed memory can be used.

Claims

1. A data processing system comprising a memory (30) for buffering sequential data units for the duration of cyclically recurrent delay lengths, characterized in that selecting means (40, 48, 50) are provided for generating, for each one of at least two memory locations, a periodic sequence of time slots having lengths corresponding to the delay lengths, each time slot for a memory location beginning with a write phase for the relevant data unit and ending in a read phase, in which read phase the relevant data unit is read for the last time, and in which sequence a sequence period includes a permutation of the time slots that correspond to the cyclically recurrent delay lengths, in which permutation the read phase of the preceding time slot is followed by a next-sequentially possible write phase of a further time slot, and a mutual shift between the sequences of consecutive memory locations amounts to a single cycle, and the period is equal to a sum of the mutual shifts.

2. A data processing system as claimed in Claim 1, characterized in that the selecting means (40, 48, 50) include reference means for generating a next reference value at the start of each next cycle of delay lengths, a sequence of reference values being recurrent with a period of the sequence of time slots, and also include first (48) and second (50) combining means respectively, for generating for the memory read and write addresses respectively, by linearly combining cyclically recurrent first and second increments respectively, with a current reference value.

3. A data processing system as claimed in Claim 2, characterized in that the reference means include a modulo counter (40) whose count represents the current reference value.

4. A data processing system as claimed in Claim 2 or 3, characterized in that a leap between sequential reference values is adjustable.

5. A data processing system as claimed in Claim 1 characterized in that the selecting means include third (60) and fourth (62) combining means respectively, for consecutively generat-

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ing first and second addresses for the memory, respectively, by consecutively linearly combining a cyclically recurrent third and fourth increment respectively, with a preceding first address and the first address respectively, the first and the second addresses being either the write addresses and the read addresses or the read addresses and the write addresses.

6. A data processing system as claimed in Claim 5, characterized in that of the third combining means (60) a first input receives the third increment and an output is fed back to a second input via a memory element (64), a first input of the fourth combining means (62) receiving the fourth increment and a second input being connected to the output of the third combining means (60).

7. A data processing system as claimed in Claim 2, 3, 4, 5 or 6, characterized in that various streams of sequential data units can be applied to the memory (30), various pairs of the said combining means being provided for the purpose of (buffering) these streams and respective pairs of further streams of the said cyclically recurrent increments can be applied to each one of the pairs of the combining means.

8. A data processing system as claimed in Claim 6, characterized in that in addition to a first stream of sequential data units further streams of sequential data units can be applied to the memory (30), for the purpose of (buffering) these further streams, the selecting means including further pairs of further combining means, the relevant second two inputs of these further combining means being connected to the output of the third combining means (60) and the relevant first inputs receiving further, cyclically recurrent increments.

9. A data processing system as claimed in one of the Claims 2 to 8, characterized in that the said increments are adjustable.

10. Selecting means suitable for use in a data processing system comprising a memory (30) for buffering sequential data units for the duration of cyclically recurrent delay lengths, characterized in that said selecting means (40, 48, 50) are provided for generating, for each one of at least two memory locations, a periodic sequence of time slots having lengths corresponding to the delay lengths, each time slot for a memory location beginning with a write phase for the relevant data unit and ending in a read phase, in which read phase the relevant data unit is read for the last time, and in which sequence a sequence period includes a permutation of the time slots that correspond to the cyclically recurrent delay lengths, in which permutation the read phase of the preceding time slot is followed by a next-sequentially possible write phase of a further time slot, and a mutual shift between the sequences of consecutive memory locations amounts to a single cycle, and the period is equal to a sum of the mutual shifts.

11. Selecting means as claimed in claim 10, characterized in that the selecting means (40, 48, 50) include reference means for generating a next reference value at the start of each next cycle of delay lengths, a sequence of reference values being recurrent with a period of the sequence of time slots, and also include first (48) and second (50) combining means respectively, for generating for the memory read and write addresses respectively, by linearly combining cyclically recurrent first and second increments respectively, with a current reference value.

Patentansprüche

1. Datenverarbeitungssystem mit einem Speicher (30) zur Pufferung sequentieller Dateneinheiten für die Dauer von sich zyklisch wiederholenden Verzögerungszeiten, dadurch gekennzeichnet, daß Selektionsmittel (40, 48, 50) vorgesehen sind zur Erzeugung einer periodischen Folge von Zeitschlitzen, deren Länge der Dauer der Verzögerungszeiten entspricht, für jeden einzelnen der mindestens zwei Speicherplätze, wobei jeder Zeitschlitz für einen Speicherplatz mit einer Schreibphase für die jeweilige Dateneinheit beginnt und mit einer Lesephase endet, in der die betreffende Dateneinheit zum letzten Mal gelesen wird, und wobei eine Periode der Folge eine Permutation der Zeitschlitze umfaßt, deren Länge den sich zyklisch wiederholenden Verzögerungszeiten entspricht, bei welcher der Lesephase des vorhergehenden Zeitschlitzes eine nächstfolgende mögliche Schreibphase eines weiteren Zeitschlitzes folgt, und wobei eine Staffelung zwischen den Folgen bei aufeinanderfolgenden Speicherplätzen einen einzigen Zyklus ausmacht und die Periode der Summe der Staffelungen entspricht.

2. Datenverarbeitungssystem nach Anspruch 1, dadurch gekennzeichnet, daß die Selektionsmittel (40, 48, 50) Referenzmittel zur Erzeugung eines nächsten Referenzwertes zu Be-

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ginn jedes nächsten Zyklus der Verzögerungszeiten enthalten, wobei eine Folge von Referenzwerten mit einer Periode der Folge von Zeitschlitzen periodisch ist, und auch erste (48) beziehungsweise zweite (50) Kombinationsmittel zur Erzeugung der Speicherleseadressen bzw. der Speicherschreibadressen durch lineare Kombination der sich zyklisch wiederholenden ersten bzw. zweiten Inkremente mit einem aktuellen Referenzwert enthalten.

3. Datenverarbeitungssystem nach Anspruch 2, dadurch gekennzeichnet, daß die Referenzmittel einen Modulo-Zähler (40) enthalten, dessen Zählerstand den aktuellen Referenzwert darstellt.

4. Datenverarbeitungssystem nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß ein Sprung zwischen sequentiellen Referenzwerten einstellbar ist.

5. Datenverarbeitungssystem nach Anspruch 1, dadurch gekennzeichnet, daß die Selektionsmittel dritte (60) beziehungsweise vierte (62) Kombinationsmittel enthalten, um nacheinander eine erste beziehungsweise eine zweite Adresse für den Speicher zu erzeugen, indem ein sich zyklisch wiederholendes drittes beziehungsweise viertes Inkrement mit einer vorhergehenden ersten Adresse beziehungsweise der ersten Adresse linear kombiniert wird, wobei die erste und die zweite Adresse entweder die Schreibadressen und die Leseadressen oder die Leseadressen und die Schreibadressen sind.

6. Datenverarbeitungssystem nach Anspruch 5, dadurch gekennzeichnet, daß ein erster Eingang der dritten Kombinationsmittel (60) das dritte Inkrement erhält und ein Ausgang über ein Speicherelement (64) an einen zweiten Eingang zurückgekoppelt wird, wobei ein erster Eingang der vierten Kombinationsmittel (62) das vierte Inkrement erhält und ein zweiter Eingang mit dem Ausgang der dritten Kombinationsmittel (60) verbunden ist.

7. Datenverarbeitungssystem nach Anspruch 2, 3, 4, 5 oder 6, dadurch gekennzeichnet, daß verschiedene Ströme von sequentiellen Dateneinheiten einem Speicher (30) zugeführt werden können, verschiedene Paare der genannten Kombinationsmittel zur Pufferung dieser Ströme vorgesehen sind und entsprechende Paare der weiteren Ströme der genannten sich zyklisch wiederholenden Inkremente jedem der Paare der Kombinationsmittel zugeführt werden können.

8. Datenverarbeitungssystem nach Anspruch 6, dadurch gekennzeichnet, daß zusätzlich zu einem ersten Strom von sequentiellen Dateneinheiten einem Speicher (30) weitere Ströme von sequentiellen Dateneinheiten zugeführt werden können, wobei zur Pufferung dieser weiteren Ströme die Selektionsmittel weitere Paare von weiteren Kombinationsmitteln enthalten, wobei die entsprechenden beiden zweiten Eingänge dieser weiteren Kombinationsmittel mit dem Ausgang der dritten Kombinationsmittel (60) verbunden sind und die entsprechenden ersten Eingänge weitere, sich zyklisch wiederholende Inkremente erhalten.

9. Datenverarbeitungssystem nach einem der Ansprüche 2 bis 8, dadurch gekennzeichnet, daß die genannten Inkremente einstellbar sind.

10. Selektionsmittel geeignet für die Verwendung ein einem Datenverarbeitungssystem mit einem Speicher (30) zur Pufferung sequentieller Dateneinheiten für die Dauer von sich zyklisch wiederholenden Verzögerungszeiten, dadurch gekennzeichnet, daß die genannten Selektionsmittel (40, 48, 50) vorgesehen sind zur Erzeugung einer periodischen Folge von Zeitschlitzen, deren Lange der Dauer der Verzögerungszeiten entspricht, für jeden einzelnen der mindestens zwei Speicherplätze, wobei jeder Zeitschlitz für einen Speicherplatz mit einer Schreibphase für die jeweilige Dateneinheit beginnt und mit einer Lesephase endet, in der die betreffende Dateneinheit zum letzten Mal gelesen wird, und wobei eine Periode der Folge eine Permutation der Zeitschlitze umfaßt, deren Länge den sich zyklisch wiederholenden Verzögerungszeiten entspricht, bei welcher der Lesephase des vorhergehenden Zeitschlitzes eine nächstfolgende mögliche Schreibphase eines weiteren Zeitschlitzes folgt, und wobei eine Staffelung zwischen den Folgen bei aufeinanderfolgenden Speicherplätzen einen einzigen Zyklus ausmacht und die Periode der Summe der Staffelungen entspricht.

11. Selektionsmittel nach Anspruch 10, dadurch gekennzeichnet, daß die Selektionsmittel (40, 48, 50) Referenzmittel zur Erzeugung eines nächsten Referenzwertes zu Beginn jedes nächsten Zyklus der Verzögerungszeiten enthalten, wobei eine Folge von Referenzwerten mit einer Periode der Folge von Zeitschlitzen periodisch ist, und auch erste (48) beziehungsweise zweite (50) Kombinationsmittel zur Erzeugung der Speicherleseadressen bzw. der

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Speicherschreibadressen durch lineare Kombination der sich zyklisch wiederholenden ersten bzw. zweiten Inkremente mit einem aktuellen Referenzwert enthalten.

Revendications

1. Système de traitement de données comprenant une mémoire (30) pour stocker temporairement des unités de données séquentielles pendant la durée de temporisation à récurrence cyclique, caractérisé en ce que des moyens de sélection (40, 48, 50) sont prévus pour générer, pour chacun d'au moins deux emplacements de mémoire, une séquence périodique de tranches de temps ayant des longueurs correspondant aux temporisations, chaque tranche de temps d'un emplacement de mémoire commençant par une phase d'écriture pour l'unité de données en question et se terminant par une phase de lecture, au cours de laquelle l'unité de données correspondante est lue pour la dernière fois, la séquence étant telle qu'une période de séquence comprenne une permutation des tranches de temps dont les longueurs correspondent aux temporisations à récurrence cyclique, permutation dans laquelle la phase de lecture de la tranche de temps précédente est suivie de la première phase d'écriture séquentiellement possible et un décage mutuel entre les séquences à des emplacements de mémoire successifs s'élève à un seul cycle, la période étant égale à une somme des décalages mutuels.

2. Système de traitement de données selon la revendication 1, caractérisé en ce que les moyens de sélection (40, 48, 50) comprennent des moyens de référence pour générer une valeur de référence suivante au début de chaque cycle suivant de longueurs de temporisations, une séquence de valeurs de référence étant récurrente avec une période de la séquence de tranches de temps, et comprennent également un premier moyen (48) et un deuxième moyen (50) de combinaison, respectivement, pour générer pour la mémoire des adresses de lecture et d'écriture, respectivement, par combinaison linéaire d'un premier incrément et d'un deuxième incrément récurrents de manière cyclique, respectivement, avec une valeur de référence courante.

3. Système de traitement de données selon la revendication 2, caractérisé en ce que les moyens de référence comprennent un compteur modulo (40) dont le comptage représente la valeur de référence courante.

4. Système de traitement de données selon la revendication 2 ou 3, caractérisé en ce qu'un saut entre des valeurs de référence séquentielles est réglable.

5. Système de traitement de données selon la revendication 1, caractérisé en ce que les moyens de sélection comprennent un troisième moyen (60) et un quatrième moyen (62) de combinaison, respectivement, pour générer consécutivement une première adresse et une deuxième adresse pour la mémoire, respectivement, en combinant linéairement de manière consécutive un troisième incrément et un quatrième incrément à récurrence cyclique, respectivement, avec une première adresse précédente, et la première adresse respectivement, la première adresse et la deuxième adresse étant les adresses d'écriture et de lecture ou les adresses de lecture et d'écriture.

6. Système de traitement de données selon la revendication 5, caractérisé en ce que, dans les troisièmes moyens de combinaison (60), une première entrée reçoit le troisième incrément et une sortie est réacheminée à une deuxième entrée via un élément de mémoire (64), une première entrée du quatrième moyen de combinaison (62) recevant le quatrième incrément et une deuxième entrée étant connectée à la sortie du troisième moyen de combinaison (60).

7. Système de traitement de données selon la revendication 2, 3, 4, 5 ou 6, caractérisé en ce que divers flux d'unités de données séquentielles peuvent être appliqués à la mémoire (30), diverses paires desdits moyens de combinaison étant prévues dans le but de stocker temporairement ces flux et des paires respectives des autres flux desdits incréments à récurrence cyclique peuvent être appliquées à chacune des paires des moyens de combinaison.

8. Système de traitement de données selon la revendication 6, caractérisé en ce que, en plus d'un premier flux d'unités de données séquentielles, d'autres flux d'unités de données séquentielles peuvent être appliqués à la mémoire (30) dans le but de stocker temporairement ces autres flux, les moyens de sélection comprenant d'autres paires d'autres moyens de combinaison, les deux deuxièmes entrées concernées de ces autres moyens de combinaison étant connectées à la sortie du troisième moyen de combinaison (60) et les premières entrées concernées recevant d'autres incréments à récurrence cyclique.

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9. Système de traitement de données selon l'une quelconque des revendications 2 à 8, caractérisé en ce que lesdits incréments sont réglables.

10. Moyens de sélection susceptibles d'être utilisés dans un système de traitement de données comprenant une mémoire (30) pour stocker temporairement des unités de données séquentielles pendant la durée de temporisations à récurrence cyclique, caractérisés en ce que lesdits moyens de sélection (40, 48, 50) sont prévus pour générer, pour chacun d'au moins deux emplacements de mémoire, une séquence périodique de tranches de temps ayant des longueurs correspondant aux temporisations, chaque tranche de temps d'un emplacement de mémoire comment par une phase d'écriture pour l'unité de données en question et se terminant par une phase de lecture, au cours de laquelle l'unité de données correspondante est lue pour la dernière fois, la séquence étant telle qu'une période de séquence comprenne une permutation des tranches de temps dont les longueurs correspondent aux temporisations à récurrence cyclique, permutation dans laquelle la phase de lecture de la tranche de temps précédente est suivie de la première phase d'écriture séquentiellement possible et un décalage mutuel entre les séquences à des emplacements de mémoire successifs s'élève à un seul cycle, la période étant égale à une somme des décalages mutuels.

11. Moyens de sélection selon la revendication 10, caractérisés en ce que les moyens de sélection (40, 48, 50) comprennent des moyens de référence pour générer une valeur de référence suivante au début de chaque cycle suivant de longueurs de temporisations, une séquence de valeurs de référence étant récurrente avec une période de la séquence de tranches de temps, et comprennent également un premier moyen (48) et un deuxième moyen (50) de combinaison, respectivement, pour générer pour la mémoire des adresses de lecture et d'écriture, respectivement, par combinaison linéaire d'un premier incrément et d'un deuxième incrément récurrents de manière cyclique, respectivement, avec une valeur de référence courante.

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