Low pass digital averaging filter and method of recovering a low frequency component of a composite analog waveform

This invention relates generally to low pass filters and more particularly to a low pass filter and a method employing analog to digital conversion and digital averaging techniques.

Background Art

Low pass filters for recovering low frequency components of a signal spectrum are well known in the art. Analog techniques utilizing linear R—C networks are often employed to filter an analog signal. However, R—C networks do not lend themselves to practical implementation with complex IC technology. Additionally, the stability of linear filters is a function of the resistor and capacitor component parameters, which may vary with age and temperature and which vary from one component to another, thereby requiring alignment in the factory. Also, linear R—C type filters are not ideal filters in that the signal passed by such a filter includes small contributions from signals received in the past.

Digital filtering techniques have also been used in the past, but these techniques often require high speed multipliers, shift registers, read-only memories (ROM's), and a plurality of adders. These prior art digital filters require large amounts of chip area when fabricated as an integrated circuit, thereby reducing wafer yields and resulting in higher cost.

U.S. Patent No. 3,487,405, for example, describes a radar system density zone suppressor having two multistage registers, three adders, four subtractors, two dividers, one multiplier, two accumulators, and one comparator. The suppressor averages a succession of digital inputs for modifying amplitudes of video signals applied to a radar screen. Thus, it will be appreciated by those skilled in the art that a low pass digital averaging filter which can easily be implemented within an integrated circuit and which requires a small amount of chip area is a significant improvement over the prior art.

Brief Summary of the Invention

An object of the present invention is to provide a low pass filter which may easily be implemented within an integrated circuit.

It is also an object of the present invention to provide a low pass filter having filtering characteristics which are independent of variations in the parameters of the components used to implement the filter.

It is a further object of the present invention to provide a low pass digital averaging filter which provides a digital output signal corresponding to the magnitude of the desired low frequency component.

It is a further object of the present invention to provide a low pass digital averaging filter having filtering characteristics solely dependent upon an input clock pulse.

According to one aspect of the present invention there is provided a low pass averaging filter for providing a low frequency component of an analog input signal, including an analog to digital converter having an input terminal for receiving the analog input signal and having output terminals for providing a digital representation of the received analog input signal; timing circuitry for providing at least one timing signal which defines sequential sample periods; storage circuitry responsive to the at least one timing signal for storing an average digital signal during each sample period; and a sample register in the form of delay circuitry coupled to the analog to digital converter and responsive to the at least one timing signal for storing a digital representation provided by the output terminals during a present sample period and for providing the stored digital representation as an output digital signal during a sample period which occurs a predetermined number of sample periods subsequent to the present sample period characterised by an arithmetic circuit having a multiplexer and an adder-subtractor circuit, the multiplexer being for coupling the input digital signal received during the present sample period from the analog to digital converter to the adder-subtractor circuit during a first portion of the present sample period and coupling the output digital signal from the delay circuitry to the adder-subtractor circuit during a second portion of the present sample period, the adder-subtractor circuit being operative to add the input digital signal received during the present sample period to the average digital signal during the first portion and being operative to subtract the output digital signal from the average digital signal during the second portion for providing the updated average digital signal.

According to another aspect of the invention there is provided a method of recovering a low frequency component of a composite analog waveform, including the steps of converting the analog waveform to a digital representation during periodic sample intervals, storing an average digital signal and storing a digital representation provided by the converting step characterised by providing the stored digital representation as a delayed representation a predetermined number of sample intervals following the sample intervals during which the digital representation was stored; and updating the average digital signal during each sample interval, the updating step including the steps of adding the digital representation provided by the converting step to the average digital signal and subtracting the delayed representation from the average digital signal. In a preferred embodiment, an analog to digital converter receives an analog input signal and is a source

of the input digital signals. In this embodiment, the running average of the input digital signals corresponds to the low frequency component of the analog signal received by the digital to analog converter.

Brief Description of the Drawings

Fig. 1 is a block diagram of a preferred embodiment of the invention including an analog to digital converter for receiving an analog signal.

Fig. 2 is a series of timing waveforms including (A) a high frequency component of an analog signal, (B) a low frequency component of an analog signal, (C) the composite analog signal which is formed by combining the low frequency and high frequency components, and (D) the low frequency digital component of the composite analog signal as derived according to the invention.

Fig. 3 is a more detailed block diagram of one embodiment of the adder/subtractor block shown in Fig. 1.

Fig. 4 is a more detailed logic diagram of the adder/subtractor block shown in Fig. 1 which employs a multiplexing technique for performing addition and subtraction.

Description of the Preferred Embodiments

Fig. 1 illustrates a low pass digital averaging filter according to a preferred embodiment of the invention. An analog to digital converter 2 has an input terminal 4 for receiving a composite analog input signal. The output of analog to digital converter 2 is coupled to node 6, and node 6 is coupled to conductors 8 and 10. Those skilled in the art will realize that the output of analog to digital converter 2 consists of a plurality of binary bits, each of which is typically associated with a particular binary weighting so that the plurality of binary bits corresponds to the magnitude of the received analog signal. The output of the analog to digital converter 2 may also include a sign bit for indicating positive and negative magnitudes. However, for the ease of illustration, conductors 8 and 10 are shown as single lines in Fig. 1. Analog to digital converters are well known in the art and will not be further described herein. For a more detailed description of analog to digital conversion, see Digital Electronics with Engineering Applications by Sifferlen and Vartanian, Prentiss-Hall Inc., 1970.

Conductor 10 couples the output of analog to digital converter 2 to the input of sample register 12. In the preferred embodiment, sample register 12 is a shift register having a predetermined number of storage locations for storing a predetermined number of digital words. Each of the stored digital words has as many binary bits as are provided by the output of analog to digital converter 2. Sample register 12 has an output coupled to conductor 14.

A timing signal or clock, T_1, is coupled to sample register 12 by conductor 16. Timing signal T_1 is pulsed at a periodic rate so as to define a plurality of sample periods. During each sample period, timing signal T_1 is pulsed, and the digital signal currently being output by analog to digital converter 2 is shifted into sample register 12 via conductor 10. If it is assumed that sample register 12 contains eight storage locations, for example, then sample register 12 will be filled with eight digital values after the first eight sample periods. During the ninth sample period, timing signal T_1 will again be pulsed, and a new digital value will be shifted into sample register 12. Simultaneously the digital value shifted into sample register 12 during the first sample period will be shifted out onto conductor 14 as an output value.

Thus, sample register 12 acts as a delay element to provide the digital value received eight sample periods prior to the present sample period. Although sample register 12 has been characterized in this preferred embodiment as a shift register, it will be obvious to those skilled in the art that various other storage means may be used to implement sample register 12.

Conductors 8 and 14 are coupled to first and second inputs, respectively, of adder/subtractor block 18. Adder/subtractor block 18 is coupled to storage register 20 by conductor 22. It should again be realized that conductor 22 symbolizes a group of conductors sufficient to transmit a digital value having a number of binary bits corresponding to the number of binary bits provided by the output of analog to digital converter 2. Timing signal T_2 is coupled to storage register 20 by conductor 24 and, when pulsed, causes storage register 20 to store the digital value presented by conductor 22. Storage register 20 provides an output coupled to conductor 26 for providing the digital value currently being stored. The output of storage register 20 is also coupled to output terminal 28 such that other circuitry (not shown) can access the digital value being stored by storage register 20. The output of storage register 20 is fed back by conductor 26 to a third input of adder/subtractor block 18.

The operation of the circuitry shown in Fig. 1 will now be described. It will again be assumed that sample register 12 contains eight storage locations for storing eight digital values, it being understood that the number eight is chosen only as an example. Sample register 12 is initialized to contain eight digital values, each equal to a zero value, and storage register 20 is initialized to contain a zero value. During the first sample period, timing signal T_1 is pulsed, and the first digital value is shifted into sample register 12. A zero value is shifted out of sample register 12 onto conductor 14. Adder/subtractor block 18 adds the first digital value presented by conductor 8 to the zero value presented by conductor 26 and subtracts the zero value presented by conductor 14 such that the output provided to conductor 22 is equal to the digital value provided by conductor 8.

Timing signal T_2 is then pulsed, and storage register 20 stores this initial digital value.

During the second sample period, a second digital value is output by analog to digital converter 2 and timing signal T_1 is again pulsed so as to shift this second digital value into sample register 12. A zero value is again shifted out onto conductor 14. During this second sample period, adder/subtractor block 18 adds the second digital value on conductor 8 to the first digital value stored by storage register 20 and presented by conductor 26, and subtracts the zero value provided by conductor 14 such that the output provided to conductor 22 is equal to the sum of the first and second digital values. Timing signal T_2 is then pulsed to store this sum into storage register 20. This sequence of events is repeated up to and including the eighth sample period, after which time storage register 20 contains the sum of the first eight sampled digital values. The sum stored by storage register 20 is thus proportional to the average of the first eight digital values.

During the ninth sample period, a new digital value is provided by analog to digital converter 2 which is shifted into sample register 12. Simultaneously sample register 12 causes the first digital value which was received during the first sample period to be shifted out onto conductor 14. During this ninth sample period, adder/subtractor block 18 adds the new digital value on conductor 8 to the sum previously stored by storage register 20 and provided by conductor 26. Adder/subtractor block 18 is also operative to subtract the digital value received during the first sample period such that the output provided to conductor 22 equals the sum of the digital values received during the second through ninth sample periods. Timing signal T_2 is again pulsed to store this result in storage register 20. Thus the value now stored by storage register 20 is proportional to the average of the digital values received during the most recent eight sample periods. In this manner, storage register 20 maintains a running average of only those digital values received during the most recent eight sample periods.

In Fig. 2, the operation of the low pass digital averaging filter is illustrated. Waveform A illustrates a high frequency component of a signal and waveform B illustrates a low frequency component of the same signal. Waveform C illustrates the composite signal formed by combining the high frequency and low frequency components illustrated in waveforms A and B, respectively. The composite analog waveform C is presented to input terminal 4 of analog to digital converter 2 (Fig. 1). The points at which the analog composite waveform are sampled by analog to digital converter 2 are indicated by the dots which intersect the composite voltage waveform. Waveform D is a plot of the sign and magnitude of the digital value, represented by the direction and length of each line segment, stored by storage register 20 (Fig. 1) during each sample period. It will be appreciated that waveform D effectively recovers the low frequency component shown in waveform B from composite voltage waveform C.

The analog equivalent of the circuit illustrated in Fig. 1 is a low pass filter with a corner frequency located at $\omega_c = 1/T$, where T is the time required to process the predetermined number of sampled digital signals. Assuming that the sample register contains eight storage locations, then T corresponds to eight sample periods. Thus, the operation of the low pass digital averaging filter is dependent solely upon the clock frequency and is not dependent upon device parameters of particular circuit components.

In Figure 3 one embodiment of adder/subtractor 18 is shown in greater detail. An adder block 30 receives the previous average digital value stored by storage register 20 via conductor 26 and receives a new digital value from analog to digital converter 2 via conductor 8. The digital values are added and the result of the addition is output on conductor 32 which is coupled to a first input of subtractor block 34. A second input of subtractor 34 is coupled by conductor 14 to the output of the sample register 12. Subtractor block 34 causes the digital value presented by conductor 14 to be subtracted from the digital value provided by conductor 32 and provides an output to conductor 22 to allow the result of the subtraction to be stored in storage register 20. As circuitry for implementing adder block 30 and subtractor block 34 is well known in the art, this circuitry will not be further described.

In Fig. 4, a second embodiment of adder/subtractor block 18 is shown in greater detail. The embodiment illustrated by Fig. 4 employs a multiplexing technique whereby a first portion of the sample period is used to add the new digital value output from the analog to digital converter to the previously stored average value, and the result of this addition is temporarily stored in storage register 20. During a second portion of the sample period, the output from the sample register 12 is subtracted from the temporarily stored value to form the updated average value, which is then stored in storage register 20.

Conductor 36 is an add/subtract control line which is a logic "0" level to select the addition operation and which is a logic "1" level to select the subtraction operation. In this embodiment, it is assumed that digital values are represented in two's-complement notation. Conductor 36 is coupled to the input of inverter 38 which has an output coupled to a first input of logic AND gate 40. A second input of AND gate 40 receives the digital value output by analog to digital converter 2 via conductor 8. It should be realized that in reality there are a plurality of logic gates corresponding to gate 40 corresponding to the number of binary bits output by

analog to digital converter 2. A single AND gate 40 is shown for the ease of illustration only. The output of AND gate 40 is coupled to a first input of logic OR gate 42 which has a second input coupled to the output of logic AND gate 44. Conductor 36 is coupled to a first input of gate 44 while a second input of gate 44 is coupled to the output of inverter gate 46. Inverter gate 46 receives at its input the digital value provided by the output of sample register 12 via conductor 14. The output of OR gate 42 is coupled by conductor 48 to a first input of adder circuit 50. A second input of adder 50 is coupled to conductor 26 which provides the digital value output from the storage register 20. Conductor 36 is also coupled to a carry-in C_{IN} input of adder 50 for causing the result of the addition to be incremented. The output of adder 50 is coupled by conductor 22 to the input of storage register 20.

When conductor 36 is at a logic "0" level, the output of inverter gate 38 will be a high level and gate 40 will be enabled while gate 44 will be disabled. The new digital value provided by conductor 8 will be passed to conductor 48 to be added within adder block 50 with the previously stored average value provided by conductor 26. The result of the addition is not incremented, and the result is temporarily stored in storage register 20. Conductor 36 is then switched to a logic "1" level which causes gate 44 to be enabled and gate 40 to be disabled. The digital value provided by the sample register is complemented (one's-complement) by inverter 46, and the complemented value is passed to conductor 48 to be added to the value temporarily stored in storage register 20 during the previous portion of the sample period. The result of the addition is incremented such that adder circuit 50 adds the two's-complement of the digital value provided from the sample register which is the same as subtracting the digital value provided from the sample register. The result of the two's-complement addition is then stored in storage register 20 and corresponds to the updated average value. It will be obvious to those skilled in the art that the order of the addition and subtraction operations can be reversed without materially affecting the performance of the low pass averaging filter.

While the invention has been described with reference to a preferred embodiment the description is for illustrative purposes only and is not to be construed as limiting the scope of the invention. Various modifications and changes may occur to those skilled in the art without departing from the scope of the invention as defined in the appended claims.

Claims

1. A low pass averaging filter for providing a low frequency component of an analog input signal, including an analog to digital converter (2) having an input terminal (4) for receiving the analog input signal and having output terminals (6) for providing a digital representation of the received analog input signal; timing circuitry for providing at least one timing signal (16, 24) which defines sequential sample periods; storage circuitry (20) responsive to the at least one timing signal for storing an average digital signal during each sample period; and a sample register in the form of delay circuitry (12) coupled to the analog to digital converter (2) and responsive to the at least one timing signal for storing a digital representation provided by the output terminals (6) during a present sample period and for providing the stored digital representation as an output digital signal during a sample period which occurs a predetermined number of sample periods subsequent to the present sample period, characterized by an arithmetic circuit (18) having a multiplexer (40, 42, 44) and an adder-subtractor circuit (50), the multiplexer being for coupling the input digital signal received during the present sample period from the analog to digital converter (2) to the adder-subtractor circuit (50) during a first portion of the present sample period and coupling the output digital from the delay circuitry (12) to the adder-subtractor circuit (50) during a second portion of the present sample period, the adder-subtractor circuit (50) being operative to add the input digital signal received during the present sample period to the average digital signal during the first portion and being operative to subtract the output digital signal from the average digital signal during the second portion for providing the updated average digital signal.

2. A method of recovering a low frequency component of a composite analog waveform, including the steps of converting the analog waveform to a digital representation during periodic sample intervals; storing an average digital signal and storing a digital representation provided by the converting step characterized by providing the stored digital representation as a delayed representation a predetermined number of sample intervals following the sample intervals during which the digital representation was stored; and

updating the average digital signal during each sample interval, the updating step including the steps of adding the digital representation provided by the converting step to the average digital signal and subtracting the delayed representation from the average digital signal.

Revendications

1. Filtre passe-bas à détermination de moyenne destiné à produire une composante à basse fréquence d'un signal analogique d'entrée, comprenant un convertisseur analogique-numérique (2) avec une borne

analog to digital converter 2. A single AND gate 40 is shown for the ease of illustration only. The output of AND gate 40 is coupled to a first input of logic OR gate 42 which has a second input coupled to the output of logic AND gate 44. Conductor 36 is coupled to a first input of gate 44 while a second input of gate 44 is coupled to the output of inverter gate 46. Inverter gate 46 receives at its input the digital value provided by the output of sample register 12 via conductor 14. The output of OR gate 42 is coupled by conductor 48 to a first input of adder circuit 50. A second input of adder 50 is coupled to conductor 26 which provides the digital value output from the storage register 20. Conductor 36 is also coupled to a carry-in C_{IN} input of adder 50 for causing the result of the addition to be incremented. The output of adder 50 is coupled by conductor 22 to the input of storage register 20.

When conductor 36 is at a logic "0" level, the output of inverter gate 38 will be a high level and gate 40 will be enabled while gate 44 will be disabled. The new digital value provided by conductor 8 will be passed to conductor 48 to be added within adder block 50 with the previously stored average value provided by conductor 26. The result of the addition is not incremented, and the result is temporarily stored in storage register 20. Conductor 36 is then switched to a logic "1" level which causes gate 44 to be enabled and gate 40 to be disabled. The digital value provided by the sample register is complemented (one's-complement) by inverter 46, and the complemented value is passed to conductor 48 to be added to the value temporarily stored in storage register 20 during the previous portion of the sample period. The result of the addition is incremented such that adder circuit 50 adds the two's-complement of the digital value provided from the sample register which is the same as subtracting the digital value provided from the sample register. The result of the two's-complement addition is then stored in storage register 20 and corresponds to the updated average value. It will be obvious to those skilled in the art that the order of the addition and subtraction operations can be reversed without materially affecting the performance of the low pass averaging filter.

While the invention has been described with reference to a preferred embodiment the description is for illustrative purposes only and is not to be construed as limiting the scope of the invention. Various modifications and changes may occur to those skilled in the art without departing from the scope of the invention as defined in the appended claims.

Claims

1. A low pass averaging filter for providing a low frequency component of an analog input signal, including an analog to digital converter (2) having an input terminal (4) for receiving the analog input signal and having output terminals (6) for providing a digital representation of the received analog input signal; timing circuitry for providing at least one timing signal (16, 24) which defines sequential sample periods; storage circuitry (20) responsive to the at least one timing signal for storing an average digital signal during each sample period; and a sample register in the form of delay circuitry (12) coupled to the analog to digital converter (2) and responsive to the at least one timing signal for storing a digital representation provided by the output terminals (6) during a present sample period and for providing the stored digital representation as an output digital signal during a sample period which occurs a predetermined number of sample periods subsequent to the present sample period, characterized by an arithmetic circuit (18) having a multiplexer (40, 42, 44) and an adder-subtractor circuit (50), the multiplexer being for coupling the input digital signal received during the present sample period from the analog to digital converter (2) to the adder-subtractor circuit (50) during a first portion of the present sample period and coupling the output digital from the delay circuitry (12) to the adder-subtractor circuit (50) during a second portion of the present sample period, the adder-subtractor circuit (50) being operative to add the input digital signal received during the present sample period to the average digital signal during the first portion and being operative to subtract the output digital signal from the average digital signal during the second portion for providing the updated average digital signal.

2. A method of recovering a low frequency component of a composite analog waveform, including the steps of converting the analog waveform to a digital representation during periodic sample intervals; storing an average digital signal and storing a digital representation provided by the converting step characterized by providing the stored digital representation as a delayed representation a predetermined number of sample intervals following the sample intervals during which the digital representation was stored; and

updating the average digital signal during each sample interval, the updating step including the steps of adding the digital representation provided by the converting step to the average digital signal and subtracting the delayed representation from the average digital signal.

Revendications

1. Filtre passe-bas à détermination de moyenne destiné à produire une composante à basse fréquence d'un signal analogique d'entrée, comprenant un convertisseur analogique-numérique (2) avec une borne

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d'entrée (4) pour recevoir le signal analogique d'entrée et des bornes de sortie (6) pour produire une représentation numérique du signal analogique d'entrée reçu; un circuit de cadence pour produire au moins un signal de cadence (16, 24) qui définit des périodes d'échantillon successives; un circuit de mémorisation (20) réagissant audit au moins un signal de cadence pour mémoriser un signal numérique de moyenne pendant chaque période d'échantillon et un registre d'échantillon sous la forme d'un circuit à retard (12) connecté au couvertisseur analogique-numérique (2) et réagissant audit au moins un signal de cadence en mémorisant une représentation numérique produite par les bornes de sortie (16) pendant une période d'échantillon présente, et produisant la représentation numérique mémorisée comme un signal numérique de sortie pendant une période d'échantillon qui apparaît à un nombre prédéterminé de périodes d'échantillon après la période d'échantillon présente, caractérisé par une unité arithmétique (18) comprenant un multiplexeur (40, 42, 44) et un circuit additionneur-soustracteur (50), le multiplexeur ayant pour fonction de coupler le signal numérique d'entrée reçu pendant la présente période d'échantillon, provenant du convertisseur analogique-numérique (2) avec le circuit additionneur-soustracteur 50 pendant une première partie de la présente période d'échantillon, et couplant le signal numérique de sortie provenant du circuit à retard (12) avec le circuit additionneur-soustracteur (50) pendant une seconde partie de la présente période d'échantillon, le circuit additionneur-soustracteur ayant pour fonction d'additionner le signal numérique d'entrée reçu pendant la présente période d'échantillon avec le signal numérique de moyenne pendant la première partie, et également de soustraire le signal numérique de sortie du signal numérique de moyenne pendant la seconde partie pour produire le signal numérique de moyenne corrigé.

2. Procédé de restitution d'une composante à basse fréquence d'une forme d'onde analogique composite, comprenant les phases de conversion de la forme d'onde analogique en une représentation numérique pendant des intervalles périodiques d'échantillon; de mémorisation d'un signal numérique de moyenne et de mémorisation d'une représentation numérique produite par la phase de conversion, caractérisé par la production de la représentation numérique mémorisée comme une représentation retardée d'un nombre prédéterminé d'intervalles d'échantillon suivant les invervalles d'échantillon pendant lesquels la représentation numérique a été mémorisée et de correction du signal numérique de moyenne pendant chaque intervalle d'échantillon, la phase de correction comprenant les phases d'addition de la représentation numérique produite par la phase de conversion avec le signal numérique de moyenne et de soustraction de la représentation retardée du signal numérique de moyenne.

Patentansprüche

1. Tiefpaß-Mittelungsfilter zum Erzeugen einer Niederfrequenzkomponente eines analogen Eingangssignals, mit einem Analog-Digital-Wandler (2) mit einer Eingangsklemme (4) zum Empfangen des analogen Eingangssignals und mit Ausgangsklemmen (6) zum Erzeugen einer digitalen Darstellung des empfangenen analogen Eingangssignals; mit einer Zeitgeberschaltung zum Erzeugen von wenigstens einem Zeitgebersignal (16, 24), das aufeinander folgende Abtastperioden festlegt; mit einer Speicherschaltung (20), die auf das wenigstens eine Zeitgebersignal anspricht, um ein gemitteltes digitales Signal während jeder Abtastperiode zu speichern; und mit einem Abtastregister in der Form einer Verzögerungsschaltung (12), die an den Analog-Digital-Wandler (2) angeschlossen ist und auf das wenigstens eine Zeitgebersignal anspricht, um eine digitale Darstellung zu speichern, die durch die Ausgangsklemmen (6) während einer momentanen Abtastperiode geschaffen wird, und um die gespeicherte digitale Darstellung als ein digitales Ausgangssignal während einer Abtastperiode zu erzeugen, die eine vorbestimmte Anzahl von Abtastperioden nach der momentanen Abtastperiode auftritt, gekennzeichnet durch eine arithmetische Schaltung (18) mit einem Multiplexer (40, 42, 44) und einer Additions-Subtraktions-Schaltung (50), wobei der Multiplexer vorgesehen ist für die Kopplung des digitalen Eingangssignals, das während der momentanen Abtastperiode von dem Analog-Digital-Wandler (2) empfangen wird, mit der Additions-Subtraktions-Schaltung (50) während eines ersten Teils der momentanen Abtastperiode, und für die Kopplung des digitalen Ausgangssignals von der Verzögerungsschaltung (12) mit der Additions-Subtraktions-Schaltung (50) während eines zweiten Teils der momentanen Abtastperiode, wobei die Additions-Subtraktions-Schaltung betätigbar ist, um das während der momentanen Abtastperiode empfangene digitale Eingangssignal zu dem gemittelten digitalen Signal während des ersten Teiles zu addieren und um das digitale Ausgangssignal von dem gemittelten digitalen Signal während des zweiten Teils zu subtrahieren, um das aufgebesserte gemittelte digitale Signal zu schaffen.

2. Verfahren zum Wiedergewinnen einer Niederfrequenzkomponente einer zusammengesetzten analogen Wellenform, mit den Verfahrensschritten des Umwandelns der analogen Wellenform in eine digitale Darstellung während periodischen Abtastintervallen, des Speicherns eines gemittelten digitalen Signals und des Speicherns einer digitalen Darstellung, die

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durch den Umwandlungsschritt geschaffen wurde, gekennzeichnet durch die Erzeugung der gespeicherten digitalen Darstellung als eine verzögerte Darstellung, die den Abtastintervallen, während der die digitale Darstellung gespeichert wurde, um eine vorbestimmte Anzahl von Abtastintervallen nachfolgt; und durch Aufbessern des gemittelten digitalen Signals während jedem Abtastintervall, wobei der Aufwertungsschritt die Verfahrensschritte des Addierens der digitalen Darstellung, die durch den Umwandlungsschritt in ein gemitteltes digitales Signal geschaffen wurde, und des Subtrahierens der verzögerten Darstellung von dem gemittelten digitalen Signal unfaßt.

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