(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 November 2005 (03.11.2005)

PCT

(10) International Publication Number
WO 2005/104190 A3

(51) International Patent Classification[7]: H01L 21/288, 21/768

(21) International Application Number: PCT/US2005/009781

(22) International Filing Date: 23 March 2005 (23.03.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/822,030 8 April 2004 (08.04.2004) US

(71) Applicant *(for all designated States except US)*: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 South Federal Way, Boise, Idaho 83716 (US).

(72) Inventors: **SINHA, Nishant**; 4008 Federal Way D-101, Boise, ID 83706 (US). **CHOPRA, Dinesh**; 2832 East Red Fir Court, Boise, ID 83716 (US). **FISHBURN, Fred, D.**; 1608 North 8th Street, Boise, ID 83702 (US).

(74) Agents: **LATWESEN, David, G.** et al.; Wells St. John, 601 W. First Avenue, Spokane, WA 99201 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

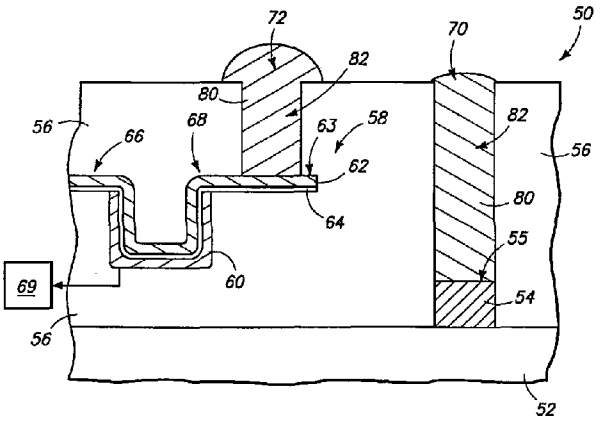
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
23 February 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR PROCESSING METHODS FOR FORMING ELECTRICAL CONTACTS, AND SEMICONDUCTOR STRUCTURES



(57) Abstract: Electroless plating can be utilized to form electrical interconnects associated with semiconductor substrates. For instance, a semiconductor substrate can be formed to have a dummy structure (102) thereover with a surface suitable for electroless plating, and to also have a digit line (54) thereover having about the same height as the dummy structure. A layer (56) can be formed over the dummy structure and digit line, and openings (120, 122) can be formed through the layer to the upper surfaces of the dummy structure and digit line. Subsequently, a conductive material can be electroless plated within the openings to form electrical contacts within the openings. The opening (122) extending to the dummy structure can pass through a capacitor electrode (62), and accordingly the conductive material formed within such opening can be utilized to form electrical contact to the capacitor electrode.

WO 2005/104190 A3