

ABSTRACT

A circuit is added to a complementary metal-oxide silicon (CMOS) integrated circuit (IC) to provide an intentional, non-
5 reverse-biased VDD-to-VSS shunt path for transient currents such as electrostatic discharges (ESD). This circuit protects the IC from ESD damage by turning on before any other path, thus directing the ESD transient current away from easily damaged structures. Specifically, the ESD transient current is steered
10 from the VDD rail to the VSS rail through the on conduction of a P-channel transistor whose source and drain are connected to VDD and VSS respectively. The voltage on the gate of this transistor follows the VDD supply rail because it is driven by a delay network formed by a second transistor and a capacitor.
15 This VDD-tracking delay network turns the VDD-to-VSS transistor on during a transient and off during normal operation of the IC.

Figure 4

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