~~What is claimed is:~~

1. A method for manufacturing an integrated circuit system comprising:

providing a substrate including front-end-of-line circuitry;

forming a first metallization layer over the substrate and electrically connected to the substrate;

forming a viabar or a via group over the first metallization layer; and

forming a second metallization layer over the first metallization layer and electrically connected to the first metallization layer through either the viabar or the via group.

2. The system as claimed in claim 1 wherein:

forming the viabar includes a staggered configuration or an adjacent configuration.

3. The system as claimed in claim 1 wherein:

forming the viabar includes a continuous configuration.

4. The system as claimed in claim 1 wherein:

forming the via group includes a staggered configuration.

5. The system as claimed in claim 1 wherein:

forming the via group includes an adjacent configuration.

6. A method for manufacturing an integrated circuit system comprising:

providing a substrate including front-end-of-line circuitry;

forming a first metallization layer including a first conductive trace electrically connected to a first terminal and a second conductive trace electrically connected to a second terminal over the substrate and electrically connected to the substrate;

forming a viabar or a via group over each of the first conductive trace and the second conductive trace; and

forming a second metallization layer including a first conductive trace electrically connected to a first terminal and a second conductive trace electrically connected to a second terminal over the first metallization layer and electrically connected to the first metallization layer through either the viabar or the via group.

7. The system as claimed in claim 6 wherein:

forming the first metallization layer and the second metallization layer includes forming an inter-digitated structure.

8. The system as claimed in claim 6 wherein:

forming the first conductive trace and the second conductive trace includes forming the first conductive trace and the second conductive trace of opposite polarity.

9. The system as claimed in claim 6 wherein:

forming the first conductive trace and the second conductive trace includes forming the first conductive trace and the second conductive trace with a pitch of 800 nanometers or less.

10. The system as claimed in claim 6 further comprising:

forming a vertical natural capacitor.

11. An integrated circuit system comprising:

a substrate including front-end-of-line circuitry;

a first metallization layer over the substrate and electrically connected to the substrate;

a viabar or a via group over the first metallization layer; and

a second metallization layer over the first metallization layer and electrically connected to the first metallization layer through either the viabar or the via group.

12. The system as claimed in claim 11 wherein:

the viabar includes a staggered configuration.

13. The system as claimed in claim 11 wherein:

the viabar includes an adjacent configuration

14. The system as claimed in claim 11 wherein:

the viabar includes a continuous configuration.

15. The system as claimed in claim 11 wherein:

the via group includes a staggered configuration.

16. The system as claimed in claim 11 wherein:

the via group includes an adjacent configuration.

17. The system as claimed in claim 11 wherein:

the first metallization layer and the second metallization layer include an inter-digitated structure.

18. The system as claimed in claim 11 wherein:

the first metallization layer and the second metallization layer each include a first conductive trace and a second conductive trace each of opposite polarity.

19. The system as claimed in claim 11 wherein:

the first metallization layer and the second metallization layer each include a first conductive trace and a second conductive trace with a pitch of 800 nanometers or less.

20. The system as claimed in claim 11 wherein:

the integrated circuit system includes a vertical natural capacitor.

What is claimed is:

1. A method for manufacturing an integrated circuit system comprising:

providing a substrate including front-end-of-line circuitry;

forming a first metallization layer over the substrate and electrically connected to the substrate;

forming a via group over the first metallization layer; and

forming a second metallization layer over the first metallization layer and electrically connected to the first metallization layer through the via group.

2. The system as claimed in claim 1 wherein:

forming the via group includes forming each of the via within the via group to act independently.

3. The system as claimed in claim 1 wherein:

forming the via group includes forming each of the via within the via group to act collectively.

4. The system as claimed in claim 1 wherein:

forming the via group includes a staggered configuration.

5. The system as claimed in claim 1 wherein:

forming the via group includes an adjacent configuration.

6. A method for manufacturing an integrated circuit system comprising:

providing a substrate including front-end-of-line circuitry;

forming a first metallization layer including a first conductive trace electrically connected to a first terminal and a second conductive trace electrically connected to a second terminal over the substrate and electrically connected to the substrate;

forming a via group over each of the first conductive trace and the second conductive trace; and

forming a second metallization layer including a first conductive trace electrically connected to a first terminal and a second conductive trace electrically connected to a second terminal over the first metallization layer and electrically connected to the first metallization layer through the via group.

7. The system as claimed in claim 6 wherein:
forming the first metallization layer and the second metallization layer includes forming an inter-digitated structure.

8. The system as claimed in claim 6 wherein:
forming the first conductive trace and the second conductive trace includes forming the first conductive trace and the second conductive trace of opposite polarity.

9. The system as claimed in claim 6 wherein:
forming the first conductive trace and the second conductive trace includes forming the first conductive trace and the second conductive trace with a pitch of 800 nanometers or less.

10. The system as claimed in claim 6 further comprising:
forming a vertical natural capacitor.

11. An integrated circuit system comprising:
a substrate including front-end-of-line circuitry;
a first metallization layer over the substrate and electrically connected to the substrate;
a via group over the first metallization layer; and
a second metallization layer over the first metallization layer and electrically connected to the first metallization layer through the via group.

12. The system as claimed in claim 11 wherein:
the via group includes each of the via within the via group acting independently.

13. The system as claimed in claim 11 wherein:
the via group includes each of the via within the via group acting collectively.

14. The system as claimed in claim 11 wherein:
the via group is configured to alter capacitance or the occurrence of short circuits.

15. The system as claimed in claim 11 wherein:
the via group includes a staggered configuration.

16. The system as claimed in claim 11 wherein:
the via group includes an adjacent configuration.

17. The system as claimed in claim 11 wherein:

the first metallization layer and the second metallization layer include an inter-digitated structure.

18. The system as claimed in claim 11 wherein:

the first metallization layer and the second metallization layer each include a first conductive trace and a second conductive trace each of opposite polarity.

19. The system as claimed in claim 11 wherein:

the first metallization layer and the second metallization layer each include a first conductive trace and a second conductive trace with a pitch of 800 nanometers or less.

20. The system as claimed in claim 11 wherein:

the integrated circuit system includes a vertical natural capacitor.