

CLAIMS

1. A method for processing in a data processing system including a system memory, the method comprising:
a processor core processing a translation load instruction, wherein the translation load instruction includes a protection field specifying a desired access protection to be specified in a translation entry for a memory page, and wherein processing the translation load instruction includes:
calculating an effective address within the memory page; and
ensuring that a translation entry containing the desired access protection is stored within at least one translation structure of the data processing system.
2. The method of Claim 1, wherein:
the at least one translation structure includes a translation structure in the processor core;
the translation load instruction includes a load field;
the method further comprises the processor core, based on the load field being set, installing the translation entry for the effective address in the translation structure in the processor core.
3. The method of Claim 2, wherein the translation structure comprises a translation lookaside buffer.
4. The method of any of the preceding claims, wherein the at least one translation structure includes a page frame table in the system memory.
5. The method of any of the preceding claims, wherein:
the protection field in the translation load instruction is a first protection field;
the translation entry includes a second protection field; and
the method further comprises the processor core invoking a protection fault handler based on a mismatch of access protections specified in the first and second protection fields.
6. The method of Claim 5, and further comprising:
determining whether a modification of access protections requested by the translation load instruction is legal; and
responsive to determining the modification of access protections requested by the translation load instruction is legal, updating the second protection field in the translation entry.
7. The method of any of the preceding claims, wherein:
the data processing system includes a nest memory management unit coupled to a system fabric of the data processing system; and

the processing comprises the processor core processing the translation load instruction based on receiving an interrupt initiated by the nest memory management unit.

8. A processing unit for a data processing system, the processing unit comprising:
 - a processor core including:
 - a memory management unit that translates effective addresses to real addresses; and
 - an execution unit that executes instructions;wherein the processor core is configured to perform:
 - processing a translation load instruction, wherein the translation load instruction includes a protection field specifying a desired access protection to be specified in a translation entry for a memory page, and wherein processing the translation load instruction includes:
 - calculating an effective address within the memory page; and
 - ensuring that a translation entry containing the desired access protection is stored within at least one translation structure of the data processing system.
9. The processing unit of Claim 8, wherein:
 - the at least one translation structure includes a translation structure in the processor core;
 - the translation load instruction includes a load field;
 - the processor core is configured, based on the load field being set, to install the translation entry for the effective address in the translation structure in the processor core.
10. The processing unit of Claim 9, wherein the translation structure comprises a translation lookaside buffer.
11. The processing unit of any of claims 8 to 10, wherein the at least one translation structure includes a page frame table in the system memory.
12. The processing unit of any of claims 8 to 11, wherein:
 - the protection field in the translation load instruction is a first protection field;
 - the translation entry includes a second protection field; and
 - the processor core invokes a protection fault handler based on a mismatch of access protections specified in the first and second protection fields.
13. The processing unit of Claim 12, wherein the processor core is further configured to perform:
 - determining whether a modification of access protections requested by the translation load instruction is legal; and

responsive to determining the modification of access protections requested by the translation load instruction is legal, updating the second protection field in the translation entry.

14. The processing unit of any of claims 8 to 13, wherein:

the data processing system includes a nest memory management unit coupled to a system fabric of the data processing system; and

the processor core processes the translation load instruction based on receiving, via the system fabric, an interrupt initiated by the nest memory management unit.

15. A data processing system including a plurality of processing units according to any of claims 8 to 14 and a system fabric coupling the plurality of processing units.

16. A computer program product for processing in a data processing system including a system memory, the computer program product comprising:

a computer readable storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method according to any of claims 1 to 7.

17. A computer program stored on a computer readable medium and loadable into the internal memory of a digital computer, comprising software code portions, when said program is run on a computer, for performing the method of any of claims 1 to 7.