

DRAM QUEUE MANAGER FOR A BUFFER

ABSTRACT

A bandwidth conserving queue manager for a FIFO buffer is provided, preferably on an ASIC chip (10) and including separate DRAM storage (22) that maintains a FIFO queue which can extend beyond the data storage space of the FIFO buffer to provide additional data storage space as needed. FIFO buffers (14, 32) are used on the ASIC chip (10) to store and retrieve multiple queue entries. As long as the total size of the queue does not exceed the storage available in the buffers (14, 32), no additional data storage is needed. However, when some predetermined amount of the buffer storage space in the FIFO buffers (14, 32) is exceeded, data are written to and read from the additional data storage (22), in packets of optimum size for maintaining peak performance and which are written to the data storage device in a first-in, first-out sequence. Preferably, the data are written to the DRAM in burst mode.

FIG. 1