

**SEMICONDUCTOR MEMORY CELL AND METHOD OF
MANUFACTURING THE SAME**

ABSTRACT

A semiconductor memory cell comprising (1) a first transistor of a first conductivity type for read-out having source/drain regions composed of a surface region of a third region and a second region and a channel forming region composed of a surface region of a first region, (2) a second transistor of a second conductivity type for write-in having source/drain regions composed of the first region and a fourth region and a channel forming region composed of a surface region of the third region, and (3) a junction-field-effect transistor of a first conductivity type for current control having gate regions composed of the fourth region and a portion of the first region facing the fourth region, a channel region composed of the third region sandwiched by the fourth region and the first region and source/drain regions composed of the third region.

Figure 1