

## Monolithic High Voltage Driver Circuit

### Field of the Invention

This invention relates to a monolithic high voltage driver circuit, and more particularly, though not exclusively to such a high voltage driver circuit for use as an interface between low voltage video signals input to a Cathode Ray Tube (CRT) display, such as a computer monitor, and the high voltages required at the cathodes of the CRT.

### Background of the Invention

The video driver circuit for a computer monitor is required to interface between the low voltage video input signals, which are generally between 1 and 5 Volts peak-to-peak, and the high voltages required at the cathodes of the monitor, which should be about 40-50 Volts peak-to-peak, with a bandwidth equivalent of 45-70 MHz or more. Known video driver circuits for computer monitors are generally built either using discrete components or as a hybrid circuit, for example circuit LM2407 manufactured by National Semiconductors. Such circuits are expensive, since separate components are required. Furthermore, the known circuits are difficult to drive, requiring high input current and about 4 volts peak-to-peak input voltage.

It would therefore be desirable to produce a high voltage driver circuit in monolithic form. However, such a circuit would usually need to be produced using high voltage analog manufacturing processes, due to the components necessary for the voltages involved. In such a manufacturing process, the PNP and NPN components are not symmetrical, causing a substantial asymmetry in the output signal, which is undesirable. Also it is difficult to provide high quality transistors of both PNP and NPN types in the same process. This asymmetry can be seen as waveform 17 in FIG. 5. Waveform 18 shows the theoretical ideal waveform.

### Brief Summary of the Invention

The present invention therefore seeks to provide a monolithic high voltage driver circuit which overcomes, or at least

reduces the above-mentioned problems of the prior

Accordingly, the invention provides a monolithic high voltage driver circuit comprising a circuit input for receiving a low voltage input signal, a circuit output for providing a high voltage output signal, a reference voltage source, a main amplifier coupled to a supply voltage source and having a first input coupled to the circuit input, a second input coupled to the reference voltage source, and an output, a pull-up output stage having an input coupled to the output of the main amplifier and an output coupled to the circuit output, a pull-down output stage having an input coupled to the circuit input and an output coupled to the circuit output, wherein the pull-down output stage comprises a current mirror having an input stage and an output stage, the input stage having a static input coupled to the reference voltage source and an output, the output stage having a dynamic input coupled to the circuit input and an output coupled to the circuit output, and the current mirror further comprising an impedance coupled between the output of the input stage and the dynamic input of the output stage.

In a preferred embodiment, the static input of the input stage is coupled to the reference voltage source via a transistor, the static input being coupled to a first current electrode of the transistor, the reference voltage source being coupled to a control electrode of the transistor and a second current electrode of the transistor being coupled to the circuit output. The output of the output stage of the current mirror is preferably coupled to the first electrode of the transistor.

In one embodiment, the dynamic input of the output stage of the current mirror is coupled to the circuit input via a capacitor. The input of the pull-up stage is preferably directly coupled to the output of the main amplifier. Preferably, the output stage of the current mirror comprises a darlington transistor arrangement, and, if desired, the input stage of the current mirror can comprise a darlington transistor arrangement.

In a preferred embodiment, the driver circuit further includes a black level clamping circuit having an input coupled to the circuit output and an output coupled to the circuit input. A

reference voltage input of the black level clamping circuit is preferably coupled to the supply voltage source. The input of the black level clamping circuit is preferably coupled to the circuit output via a relatively high value impedance. Preferably, the  
5 output of the black level clamping circuit is coupled to an output of a logic control circuit, the logic control circuit having an input coupled to a clamping voltage pulse source for enabling the output of the black level clamping circuit according to a voltage level of the clamping voltage pulse source.

10 In an embodiment, the black level clamping circuit comprises a comparator for comparing a voltage level at the input of the black level clamping circuit with a reference voltage level generated from the supply voltage source and providing an output at the output of the black level clamping circuit. The  
15 output of the black level clamping circuit preferably comprises a pair of current paths, a first of the current paths being coupled via a first current mirror to the circuit input to provide a pull-down current at the circuit input, and a second of the current paths being coupled via second and third cascaded current  
20 mirrors to the circuit input to provide a pull-up current at the circuit input. Preferably, when the voltage level at the input of the black level clamping circuit and the reference voltage level generated from the supply voltage source are substantially identical, and the logic control circuit enables the output of the  
25 black level clamping circuit, then the sum of the pull-up and the pull-down currents at the circuit input is substantially zero.

The sum of the pull-up and the pull-down currents at the circuit input preferably causes an external capacitor coupled to the circuit input to be charged or discharged.

30 Conveniently, the circuit is manufactured utilising active elements which are formed of any one or more of Metal Oxide Semiconductor (MOS) transistors, Field Effect Transistors (FET), Bipolar Junction Transistors (BJT), P-channel transistors, N-channel transistors, PNP transistors or NPN transistors.

35 Brief Description of the Drawings

One embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of

which:

FIG. 1 shows a schematic block diagram of a known video monitor application

FIG. 2 shows a schematic circuit diagram of a known hybrid  
5 video driver circuit used in the system of FIG.

FIG. 3 shows a schematic block diagram of a monolithic high voltage video driver circuit according to one embodiment of the present

FIG. 4 is a schematic circuit diagram showing the circuit of  
10 FIG. 3 in more detail;

FIG. 5 shows a sample output waveform showing the improvements made by the circuit of FIG. 4;

FIG. 6 shows a schematic block diagram of a system utilising the monolithic high voltage video driver circuit of FIG 3; and

15 FIG. 7 shows sample waveforms in the system of FIG.

#### Detailed Description of the Drawings

Thus, as shown in FIG. 1, a typical, known, circuit 1 used for the purpose of providing a high voltage drive at high frequency for driving CRT's in computer, and other, monitor applications,  
20 includes a preamplifier 2, whose output is coupled to a discrete or hybrid driver circuit 3, which is a discrete circuit of individual transistors discretely wired and including thin film, or thick film, resistors mounted on an insulating substrate. Such a hybrid circuit 3 is expensive because of the additional assembly work  
25 involved but has the advantage that optimized PNP and NPN transistors can be used in the same module. In this typical application the load capacitance  $C_{LOAD}$  represents the typical load presented by the cathode of the CRT and it's associated components.

30 The conventional hybrid circuit 3 has an internal circuit as shown in FIG. 2. A voltage amplifier is formed using transistors 4 and 5 and resistors 6 and 7. Resistor 7 is used to degenerate the voltage gain and to improve the linearity of the transfer characteristic of the amplifier. The base of transistor 4 is  
35 connected to a reference voltage supply  $V_{REF}$ , which is usually 12 Volts. The output of the amplifier, taken at the junction of resistor 6 and the collector of transistor 4 is coupled to the bases

of two transistors 8 and 9. Transistors 8 and 9 are coupled together to form a "Class B" output stage.

Transistors 4 and 5 are connected in a cascode arrangement used to minimize the "Miller" feedback capacitance, so as to  
5 maximize the frequency response. Since the circuit is built using discrete transistors, it is possible to select suitable PNP and NPN devices for this output stage. However, as mentioned above, the circuit is expensive to manufacture.

Referring now to FIG 3, a schematic block diagram of a  
10 Driver Circuit 16 according to an embodiment of the present invention is shown. A main amplifier 10, which is essentially similar to that described above with reference to FIG. 2, receives the input signal  $V_{IN}$  via an input buffer stage 15. The output from the main amplifier 10 is coupled to an active pull-up stage 11,  
15 whose output is coupled to provide the output signal  $V_{OUT}$ . The main amplifier 10, as well as the active pull-up stage 11 are supplied with a supply voltage  $V_{CC}$  and with the reference voltage supply  $V_{REF}$ , which is also supplied to the input buffer stage 15, as will be more fully described below.

20 The input to the main amplifier 10 is also coupled to an active pull-down stage 12, whose output is coupled to the output of the active pull-up stage 11 to provide the output signal  $V_{OUT}$  and to the input of a Black Level clamping stage 13, whose output is coupled to the input signal  $V_{IN}$  supplied to the input buffer  
25 stage 15. The Black Level clamping stage 13 also receives, as an input, a clamping voltage  $V_{CLAMP}$  via a logic stage 14. The Black Level clamping stage 13 is also coupled to receive the supply voltage  $V_{CC}$  and the reference voltage  $V_{REF}$ , which is also supplied to the pull-down stage 12 and the logic stage 14.

30 As shown in detail in FIG. 4, as main amplifier 10 includes transistors 20 and 21 and resistors 22 and 23, which correspond to transistors 4 and 5 and resistors 6 and 7 in FIG. 2, except that, in this case, transistor 21 is formed as a MOS device, which has some desirable characteristics, as will be described below.

35 The active pull-up stage 11 is essentially similar to transistor 8 used in the circuit of FIG. 2, except that this transistor 8 is replaced in the circuit shown in FIG. 4 by a pair of MOSFET

devices 24 and 25 coupled together in a Darlington arrangement, together with resistor 26.

It is a general requirement of most driver circuits that they use a minimum of power, so it is desirable that the active pull-down stage 12 only provides a small amount of current at low frequencies. Furthermore, in the monolithic manufacturing processes available at the present time, no suitable PNP transistor or P-channel MOSFET is available. Accordingly, in this embodiment of the present invention, the active pull-down circuit 10 12 includes a current mirror having an input stage formed by transistors 58 and 59 and resistor 60, and an output stage formed by transistors 55 and 56 and resistor 57. The input stage and the output stage of the current mirror are coupled by a resistor 62. Assuming the value of resistor 62 to be small, the source current 15 to the current mirror is supplied via a resistor 61, providing a static input. A capacitor 54 dynamically couples the signal from the input buffer stage 15 to modulate the output of the current mirror.

The output of the current mirror output stage is coupled to 20 the circuit output  $V_{OUT}$  via a MOSFET transistor 63, whose gate is coupled to the reference voltage supply  $V_{REF}$ . Since the signal provided from the input buffer stage comes from an emitter follower transistor 29, it is of suitable phase so as to increase the pull down current available at the drain of transistor 63. In this 25 way the pull down current under static or low frequency conditions is maintained at a low level while with fast transients the current can be significantly increased.

The input buffer stage 15 is used to provide an input buffering function so that the input impedance is high. As shown 30 in detail in FIG. 4, the input buffer stage 15 consists of transistors 27, 28, 29, 30 32, 34, 35, 36, 38 and 39 and resistors 31, 33 and 37. Transistors 29 and 30, which constitute separate emitter followers, provide signal drive to the capacitor 54 in the active pull-down stage 12, and, via resistor 31, to transistor 20 in the 35 main amplifier 10. In order to improve the linearity of the circuit, transistors 32, 34, 35 and 36 provide a three-output current mirror in combination with the current defining resistor

33 to provide active pull-down currents for the emitter follower transistors 27, 29, and 30. Transistors 38, 39 and 28 and resistor 37 are included to provide base current compensation for the input current, which forms the base current of transistor 27.

5       The Black Level clamping stage 13 is formed with transistors 44 and 45 forming a long-tailed pair comparator. Resistor 50, together with diode-connected transistor 49, are connected between the reference voltage supply  $V_{REF}$  and ground reference  $G_{ND}$ , provide a current which is then mirrored by  
10 transistor 51 into a second current mirror formed by transistors 46 and 47 to provide the tail current for transistors 44 and 45. Resistor 48 is included to provide some voltage shift of the voltage applied to the gate of transistor 44. This voltage shift provides a black level clamp voltage reference, which is relative  
15 to the supply voltage  $V_{CC}$ .

      The output signal  $V_{OUT}$  is applied to the gate of transistor 45 via a high value resistor 52 so as to be compared to the voltage applied at the gate of transistor 44. Diode 53 is included to limit the voltage difference that can otherwise occur between the gate  
20 of transistor 44 and the gate of transistor

      The outputs of the comparator formed by transistors 44 and 45 are taken from their respective drains and coupled through a pair of current mirrors formed by transistors 43 and 42 and 41 and 40, respectively, to the input buffer stage 15. The current  
25 output at the collector of transistor 40 is coupled to the base of transistor 27, via resistor 37. The current output at the collector of transistor 42 is coupled to the base of transistor 27, via the current mirror formed by transistors 38 and 39 and via resistor 37. The sum of the currents at the base of transistor 27 therefore  
30 cause a net pull up, or pull down current at the circuit input terminal, where the input signal  $V_{IN}$  is

      The outputs of the comparator formed by transistors 44 and 45 are further coupled to the logic stage 14, which contains a Transistor-Transistor Logic (TTL) input stage formed by  
35 transistors 65, 67 and 70, together with resistors 64, 66 and 68. The emitter of transistor 65 is coupled to receive the clamping voltage  $V_{CLAMP}$  which is used to enable the pull up, or pull down,

current and the output at the collector of transistor 70 is coupled through resistors 71 and 73 to the bases of transistors 72 and 74 respectively. The outputs at the collectors of transistors 72 and 74 are used to inhibit current from the Black Level clamping stage 13 from causing the net pull up or pull down current at the base of transistor

The current at the circuit input terminal can be stored in a capacitor 78  $C_{IN}$  used to couple the input signal  $V_{IN}$  into this driver circuit 16, as shown in FIG. 6. In the application shown in FIG. 6, a primary input signal  $V_{INX}$  is coupled through an input capacitor 78  $C_{IN}$  to become the input signal  $V_{IN}$ . Generally, the clamping voltage pulse  $V_{CLAMP}$  would be in a low state (0 - 0.4 volts according to the TTL specification) and the feedback current from the Black Level clamping stage 13 would be disabled. During the black reference phase of the video signal as indicated by the straight portions 75 depicted in the video waveform 76 shown in FIG. 7, the clamping voltage pulse 77 in FIG. 7 could be at a logical high state (2.4 volts or higher according to the TTL specification), when the current from the Black Level clamping stage 13 is enabled, causing a charging or discharging of the capacitor  $C_{IN}$ . In this way the output waveform which is the inverted and amplified form of the video waveform shown in FIG. 7, will have its black level voltage brought to a level defined by the black level clamp voltage reference relative to the supply voltage  $V_{CC}$ . Thus, the input signal  $V_{INX}$  to the driver circuit 16 can be coupled through the capacitor  $C_{IN}$  and the d.c levels at the output of any preamplifier used, such as preamplifier 2 in FIG.1, are not important. As the amplifier is intended to have sufficient gain, an input voltage on the order of 0.7V, or 1V, peak black to peak white is sufficient as an input signal  $V_{IN}$ , or  $V_{INX}$  before the capacitor  $C_{IN}$ .

As shown in FIG. 5, the driver circuit 16 produces a large improvement in the negative-going edge of the output waveform 19, as compared to the waveform 17 of known circuits. The rising edge is not ideal, but is relatively sharp.

Thus, there has been described a monolithic video driver circuit having a lower cost than previously known driver circuits,

but still providing the performance necessary for high voltage applications.

5 It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.



### Claims

1. A monolithic high voltage driver circuit comprising:  
a circuit input for receiving a low voltage input signal;  
5 a circuit output for providing a high voltage output signal;  
a reference voltage source;  
a main amplifier coupled to a supply voltage source and  
having a first input coupled to the circuit input, a second input  
coupled to the reference voltage source, and an output;  
10 a pull-up output stage having an input coupled to the output  
of the main amplifier and an output coupled to the circuit output;  
a pull-down output stage having an input coupled to the  
circuit input and an output coupled to the circuit output; wherein  
the pull-down output stage comprises a current mirror  
15 having an input stage and an output stage, the input stage having  
a static input coupled to the reference voltage source and an  
output, the output stage having a dynamic input coupled to the  
circuit input and an output coupled to the circuit output, and the  
current mirror further comprising an impedance coupled between  
20 the output of the input stage and the dynamic input of the output  
stage.
2. A monolithic high voltage driver circuit according to claim 1,  
wherein the static input of the input stage is coupled to the  
25 reference voltage source via a transistor, the static input being  
coupled to a first current electrode of the transistor, the reference  
voltage source being coupled to a control electrode of the  
transistor and a second current electrode of the transistor being  
coupled to the circuit output.
- 30 3. A monolithic high voltage driver circuit according to claim 2,  
wherein the output of the output stage of the current mirror  
being coupled to the first electrode of the transistor.
- 35 4. A monolithic high voltage driver circuit according to any  
preceding claim, wherein the dynamic input of the output stage of  
the current mirror is coupled to the circuit input via a capacitor.



5. A monolithic high voltage driver circuit according to any preceding claim, wherein the input of the pull-up stage is directly coupled to the output of the main amplifier.
- 5
6. A monolithic high voltage driver circuit according to any preceding claim, wherein the output stage of the current mirror comprises a darlington transistor arrangement.
- 10
7. A monolithic high voltage driver circuit according to any preceding claim, wherein the input stage of the current mirror comprises a darlington transistor arrangement.
8. A monolithic high voltage driver circuit according to any preceding claim, further comprising a black level clamping circuit having an input coupled to the circuit output and an output coupled to the circuit input.
- 15
9. A monolithic high voltage driver circuit according to claim 8, wherein a reference voltage input of the black level clamping circuit is coupled to the supply voltage source.
- 20
10. A monolithic high voltage driver circuit according to either claim 8 or claim 9, wherein the input of the black level clamping circuit is coupled to the circuit output via a relatively high value impedance.
- 25
11. A monolithic high voltage driver circuit according to any one of claim 8, 9 or 10, wherein the output of the black level clamping circuit is coupled to an output of a logic control circuit, the logic control circuit having an input coupled to a clamping voltage pulse source for enabling the output of the black level clamping circuit according to a voltage level of the clamping voltage pulse source.
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12. A monolithic high voltage driver circuit according to any one of claim 8 to 11, wherein the black level clamping circuit comprises a comparator for comparing a voltage level at the input
- 35



of the black level clamping circuit with a reference voltage level generated from the supply voltage source and providing an output at the output of the black level clamping circuit.

5 13. A monolithic high voltage driver circuit according to claim  
12, wherein the output of the black level clamping circuit  
comprises a pair of current paths, a first of the current paths  
being coupled via a first current mirror to the circuit input to  
provide a pull-down current at the circuit input, and a second of  
10 the current paths being coupled via second and third cascaded  
current mirrors to the circuit input to provide a pull-up current at  
the circuit input.

14. A monolithic high voltage driver circuit according to claim  
15 13, wherein, when the voltage level at the input of the black level  
clamping circuit and the reference voltage level generated from  
the supply voltage source are substantially identical, and the logic  
control circuit enables the output of the black level clamping  
circuit, then the sum of the pull-up and the pull-down currents at  
20 the circuit input is substantially zero.

15. A monolithic high voltage driver circuit according to claim  
14, wherein the sum of the pull-up and the pull-down currents at  
the circuit input causes an external capacitor coupled to the circuit  
25 input to be charged or discharged.

16. A monolithic high voltage driver circuit according to any  
preceding claim, wherein the circuit is manufactured utilising  
active elements which are formed of any one or more of Metal  
30 Oxide

Semiconductor (MOS) transistors, Field Effect Transistors (FET),  
Bipolar Junction Transistors (BJT), P-channel transistors, N-  
channel transistors, PNP transistors or NPN transistors.

35 17. A monolithic high voltage driver circuit substantially as  
hereinbefore described with reference to the FIGS. 3 to 7 of the  
drawings.

## Abstract

### Monolithic High Voltage Driver Circuit

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A monolithic high voltage driver circuit (16) includes a main amplifier (10) coupled to receive an input signal via an input buffer stage (15). The output from the main amplifier (10) is coupled to an active pull-up stage (11). The input to the main  
10 amplifier (10) is also coupled to an active pull-down stage (12), whose output is coupled to the output of the active pull-up stage (11) to provide an output signal  $V_{OUT}$ , and to the input of a Black Level clamping stage (13), whose output is coupled to the input signal supplied to the input buffer stage (15). The pull-down  
15 output stage (12) is formed of a current mirror having an input stage having a static input coupled to a reference voltage source and an output stage coupled to the output of the input stage via an impedance and having a dynamic input coupled to receive the input to the main amplifier and an output to provide the output  
20 signal from the circuit.

FIG. 3.

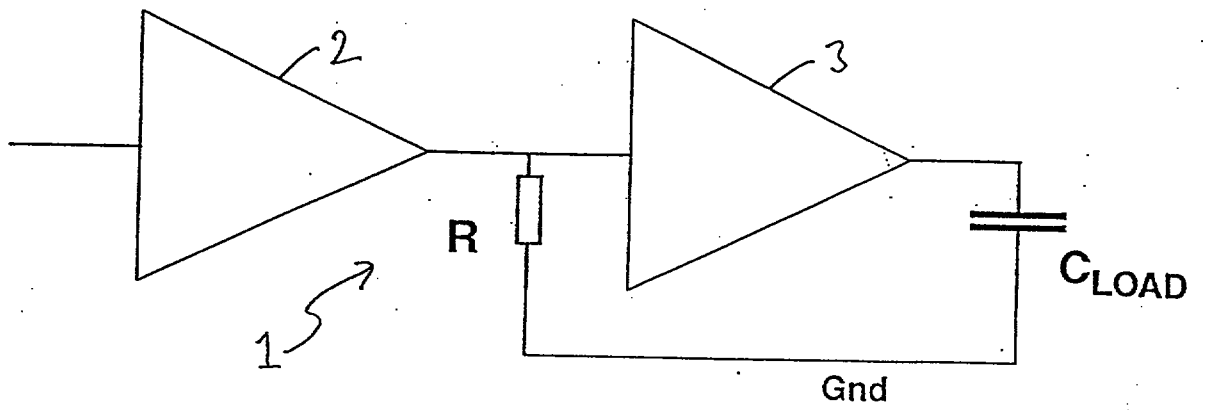


FIG 1 (PRIOR ART)

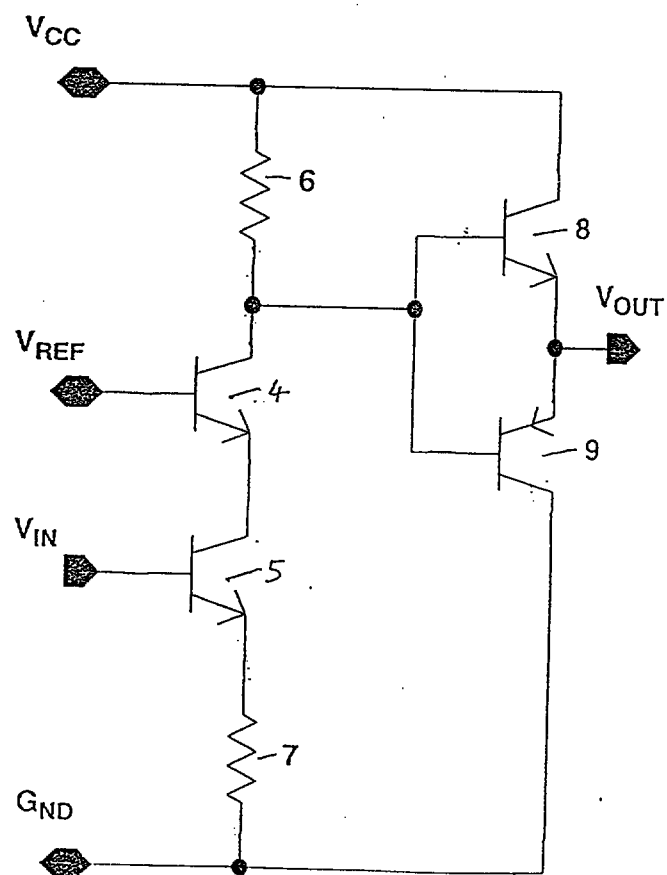
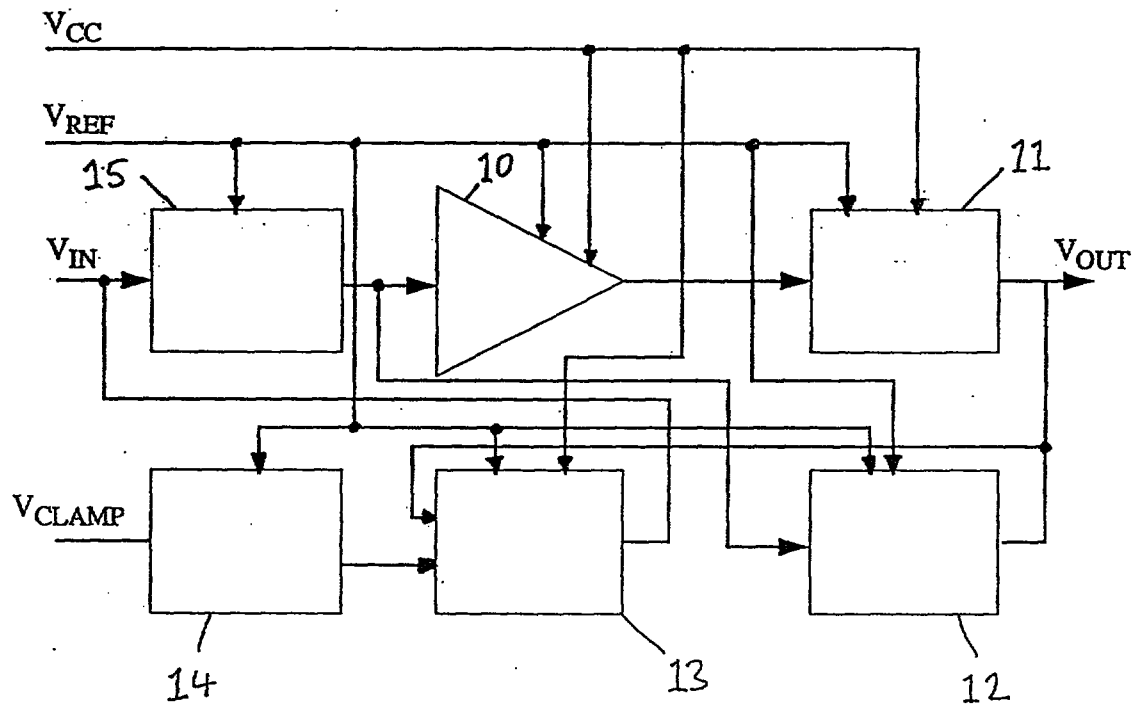


FIG. 2 (PRIOR ART)



16 ↗

FIG. 3

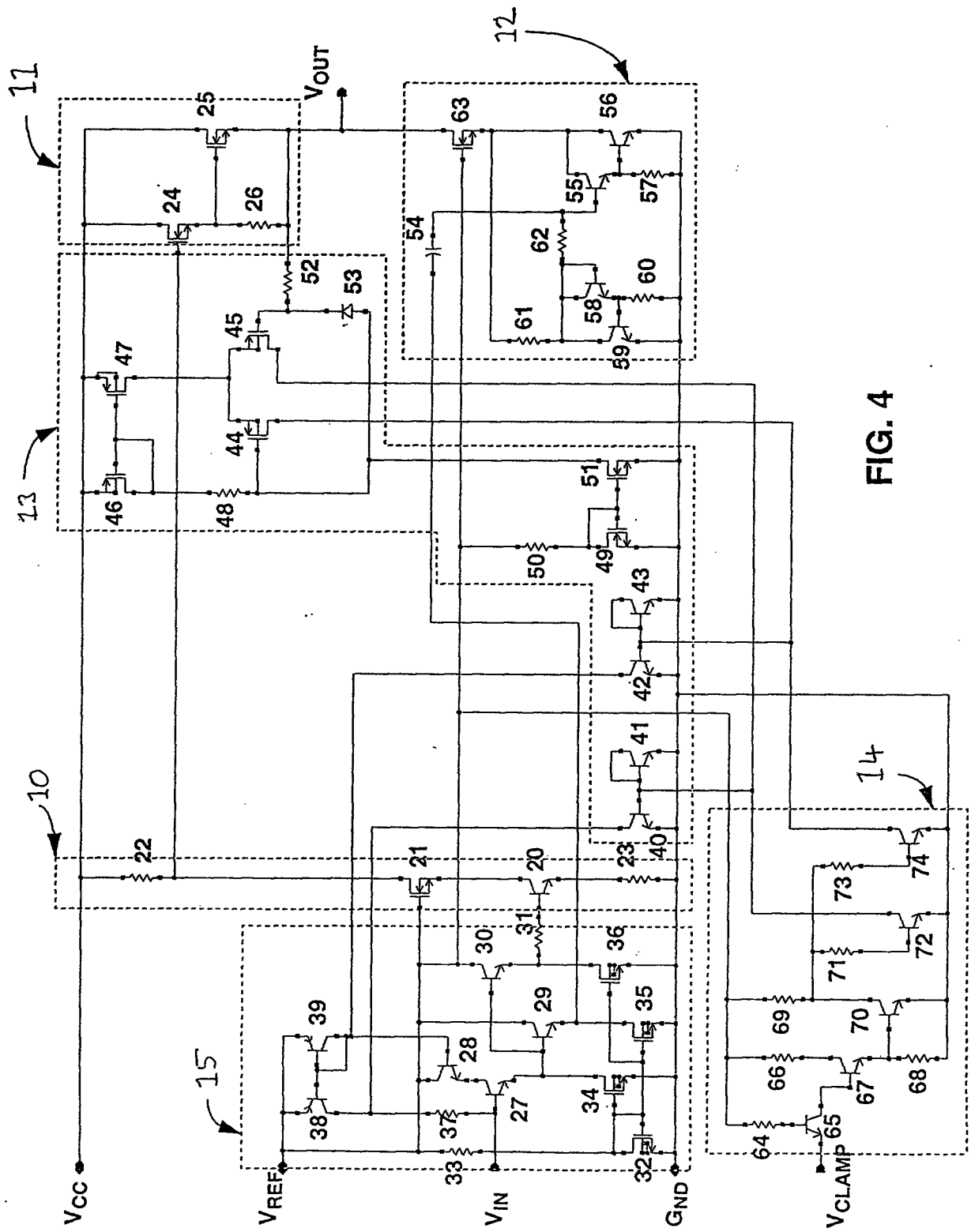


FIG. 4

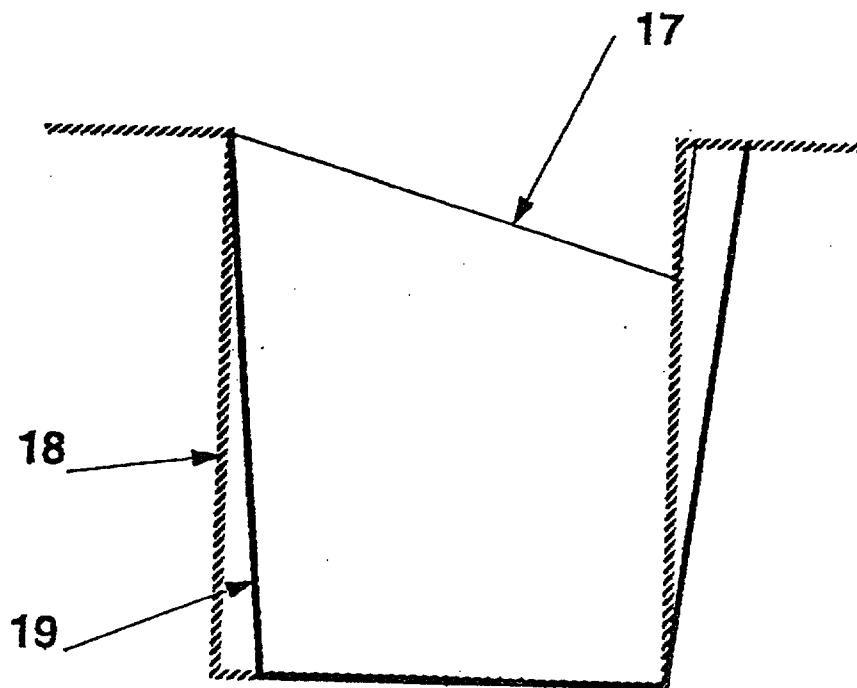


FIG. 5

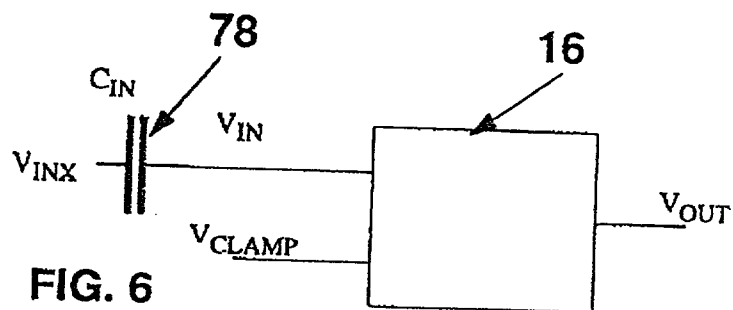


FIG. 6

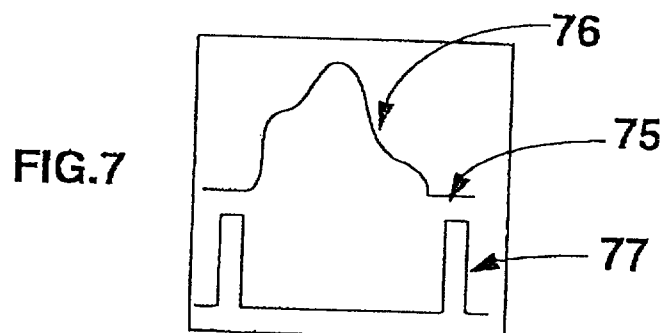


FIG. 7