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(19)



(54) PROCESS FOR FABRICATING INSULATED GATE FIELD EFFECT TRANSISTOR STRUCTURE

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION of 464 Ellis Street, Mountain View, California 94042, United States of America, a Company organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a process for fabricating complementary field effect transistor structures and, more particularly, to an improved and simplified process for fabricating a complementary field effect transistor structure wherein the source/drain regions of at least one of the complementary p-channel or n-channel field effect devices are formed by the steps of introducing an impurity of one conductivity type and then introducing an inpurity of the opposite conductivity type, one of the impurities having a relatively greater concentration than the other so that the one impurity counterdopes the other and the source/drain regions are characterized by the conductivity type of the one impurity.

Complementary field effect circuit arrangements employ n-channel and p-channel field effect transistors which are coupled so that the source or drain of one device is connected to the source or drain of the other device. In any mode of circuit operation, one of the devices will be functioning and the other will be off. When operating conditions within the circuit dictate that the functioning device turns off, the device which was previously off will begin to function due to interconnection of the sources and/or drains of the two devices. The concept was first disclosed by Wanlass in U.S. Patent No. 3,356,858. It is especially useful because no additional power is required to switch either of the devices. Switching is an inherent attribute of circuit operation.

Conventional complementary field effect devices are fabricated as conductor-insulator-semiconductor structures with interconnections between particular sources or drains of the n-channel and p-channel devices. The conductors may be metal or conductive polycrystalline silicon. Silicon dioxide is the most widely used insulator, and single crystal silicon is the most widely used semiconductor substrate. Typical complementary metal oxide semiconductor (CMOS) structures are fabricated on an n-type substrate rather than on a p-type substrate because it is easier to obtain desirable threshold voltages for both the n-channel and p-channel complementary devices. The p-well required for the n-channel complement is obtained by diffusing a lightly doped p-region into the n-type substrate. In some devices all n-channel devices are fabricated in a common p-well, and p-channel devices are fabricated in the n-substrate so that much of the overall area is taken up with interconnections between the n-channel and p-channel devices. Where individual p-wells are used for the n-channel devices, isolation of the p-channel field-effect transistors is sometimes achieved by heavily doped channel stops. These channel stops occupy a large amount of wafer surface area, degrade operating speed and limit the voltage range. Recently, polycrystalline silicon has been used in place of metal for the gate electrodes of the devices, but although transient performance is slightly improved, a negligible reduction in area has been effected. Also, the standard dopant, boron, which is placed in the polycrystalline silicon to render it conductive and to obtain a low threshold,

possesses the property that it may diffuse through the gate oxide in the presence of hydrogen and degrade the device. And, prior-art CMOS devices are known to experience impurity migration through both the gate and field oxides with resultant impairment of the operating characteristics of the devices. Finally, the presence of uncontrolled amounts of fixed surface state charges, due typically to non-stoichiometric composition of the SiO_2, also impairs the operating characteristics of the devices.

As recited in Patent Application 21285/75 (Serial No. 1,499,548) a new structure and process technology has been developed to fabricate complementary insulated gate field-effect structures which overcome the deficiencies of the prior art. As disclosed in application 21285/75, the process for fabricating complementary field effect structures and the structure realized incorporate oxide isolation of the active device regions, counterdoping of the p-well with impurities of opposite type to obtain a desirable composite doping profile, reduction of Q_{ss} in the isolation oxide, doping of the gate and field oxides with a chlorine species, and phosphorus doping of the polycrystalline silicon gates. The structures produced by this process technology are smaller, have better operating characteristics and can be produced with high yields. As described in application 21285/75 (Serial No. 1,499,548), an inherent requirement in the fabrication of p-channel and n-channel complementary devices in the same semiconductor substrate is the individual definition of the source/drain regions of the respective devices and introduction of appropriate impurities to them. Such an apparent inherent requirement is a yield-limiting factor since process complexity is proportional to achievable yield. It would be desirable, then, to form the source/drain regions of both the p-channel and n-channel devices by employing the same process steps.

In transistor electronics, it is known that an increase in the width of the space charge region surrounding a semiconductor junction is accompanied by an increase in the junction avalanche breakdown voltage. Increase in the width of the space charge region can be brought about by decreasing the background concentration of the substrate in which the junction is formed or by decreasing the overall magnitude of the doping of the diffused region or at least the slope of the doping profile of that region in the vicinity of the junction. With field-effect devices generally, it is known that breakdown across the junction of the drain and the bulk substrate may occur under severe loading conditions. In CMOS structures in which the n-channel device is fabricated in an implanted p-well, breakdown could occur across the n-type drain/p-well junction. Thus, it would be generally desirable to effect an increase in the junction avalance breakdown voltage across this junction.

The invention provides a process of fabricating a complementary insulated gate field-effect transistor structure having n-channel and p-channel devices in the same semiconductor substrate, the method having the steps of forming a well of a first conductivity type in a substrate of a second and opposite conductivity type, forming a conductor-insulator-semiconductor field-effect device having a second channel conductivity type within said well and forming a conductor-insulator-semiconductor field-effect device having a first channel conductivity type in said substrate, forming oxide-isolation regions in said substrate substantially surrounding and contiguous with said conductor-insulator-semiconductor devices, the source/drain regions of said conductor-insulator-semiconductor devices being formed by introducing an impurity of a first conductivity type into the source/drain regions of both of said devices, and introducing an impurity of a second conductivity type opposite to said first conductivity type into the source/drain regions of said device having said second channel conductivity type, the concentration of said impurity of said second conductivity type in said source/drain regions of said device having said second channel conductivity type being greater than the concentration of said impurity of said first conductivity type so that the impurity of said second conductivity type counterdopes said impurity of said first conductivity type to produce source/drain regions of said second conductivity type.

The invention will be more readily understood from the following illustrative description and the accompanying drawings, in which:

Figure 1 illustrates an intermediate process step after selective formation of a layer of silicon dioxide 12 on n-substrate 10, selective formation of a region of oxidation masking material 14 and introduction of a field implant to regions 17a, 17c and 17e;

Figure 2 is a further view of Figure 1 after growth of isoplanar isolation oxide 20, removal of oxidation masking material 14 and layer of silicon dioxide 12, application of photoresist layer 21 and introduction of p-well double ion implant 23d;

Figure 3 is a further view of Figure 2 after thermal drive in of the p-well implant to

form p-well 23d and of the field implant to form expanded field implant regions 17a, 17c and 17e, thermal growth of the gate oxide 30 and deposition of polycrystalline silicon layer 31;

Figure 4 is a further view of Figure 3 after definition of the polycrystalline silicon gate electrodes, predeposition of p^+-type impurities indiscriminately in the source/drain regions of both the p-channel and n-channel devices, and reoxidation of the exposed substrate surfaces by thermal growth;

Figure 5 is a further view of Figure 4 after removal of the thermally grown reoxidation on the exposed substrate of the n-channel device by a masking step, and predeposition of n^+-type impurities in the source/drain regions of the n-channel device;

Figure 6 is a further view of Figure 5 after deposition of additional insulating material, phosphorus gettering and source/drain drive-in, and opening up electrical contact windows;

Figure 7 is a further view of Figure 6 after conductive connectors have been applied and defined to interconnect one p^+-source/drain region of the p-channel device and one n^+-source/drain region of the n-channel device and to provide external electrical communication;

Figure 8 is a graph illustrating the constituent impurity concentrations as a function of depth within an idealized n^+-source/drain region in an n-channel device; and

Figure 9 is a pictorial diagram illustrating the location of space charge regions adjacent the NP junction of Figure 8.

Referring now to Figure 1, the substrate 10 is shown, in this preferred embodiment, to be n-conductivity-type silicon. With an n-conductivity-type substrate and associated p-well, the threshold voltages of the two complementary devices are matched more closely than is possible for devices in a p-conductivity-type substrate and associated n-well, if the compensating effect of p-well implantation is considered. Complementary devices formed in a p-type substrate with an associated n-well could have matched threshold voltage provided an additional impurity was introduced underneath the gate of the p-channel device. With this proviso, the disclosure herein of complementary field-effect devices formed in an n-substrate and associated p-well also pertains to complementary field-effect devices formed in a p-substrate and associated n-well with the appropriate substitution of analogous process steps.

A layer of oxidation masking material 14 is applied to the surface of substrate 10. This material serves to mask the active device regions while isolation regions are grown. It has been found advantageous to interpose a layer of silicon dioxide 12 between oxidation masking material 14 and the silicon substrate 10 in order to prevent defects in the substrate upon cooling and provide a more desirable geometry to the isoplanar oxide islands. The inclusion of a silicon dioxide layer 12 appears to reduce structural stresses experienced by the substrate upon cooling. For example, if the oxidation masking material 14 is silicon nitride, Si_3N_4, the silicon dioxide layer 12 will be in a state of compression while the silicon nitride 14 will be in a state of tension with respect to the silicon substrate due to the differences in coefficient of thermal expansion. The countervailing forces may protect the substrate. As shown, both the silicon dioxide and the silicon nitride are defined by carrying out a photoresist masking sequence to protect active device regions 15b and 15d and to expose isolation regions 15a, 15c and 15e.

As used above and throughout this specification, the phrase "photoresist masking sequence" refers to the well-known sequence of applying a uniform layer of a photoresist polymer, selectively exposing the photoresist by radiation of appropriate wavelength, developing the photoresist to leave a desired pattern, performing an active step such as diffusion or forming metal contacts, and removing the photoresist polymer. A complete photoresist masking sequence is also called a masking step. The details of each individual masking step are not shown in the drawings and should be inferred from the use of the term "masking step".

An n-type field implant, typically arsenic, is then introduced into field insulation regions 15a, 15c and 15e. Preferably the field implant is introduced by ion implantation because the dosage and energy of implantation can be carefully controlled. However, the field implant may also be introduced by diffusion. In either case the impurity atoms enter the surface of the substrate and repose at a shallow depth. This step is called predeposition. The silicon nitride overlying the silicon dioxide in the active device regions 15b and 15d masks the substrate regions and prevents any of the field implant impurity from reaching substrate 10. When driven into the substrate, such a field implant raises the surface concentration of n-type impurities in the n-substrate 10 and prevents inversion of the substrate underneath the field insulation regions. Such inversion would occur between p-type source/drain regions of the p-channel device and the p-well, i.e., between source/drain region 36d and p-well

23d of Figure 4. This inversion could connect the p^+-source/drain with all p-wells in a circuit since they are likely tied electrically at the same potential, thereby rendering the circuit disfunctional. In effect, the implant forms a channel stop but requires much less surface area. The concentration of the field implant is typically about one order of magnitude lower than either the substrate or p-well concentrations so that even though the n-type implant reduces the p-conductivity-type concentration and enhances the likelihood of inversion of the p-well between the n-type source/drain regions of the n-channel device and the n-substrate 10, the p-well is realtively so heavily doped beneath shallow well depths that the net p-type concentration under the isolation islands remains high enough to prevent inversion of the p-well for voltages up to about 25 volts.

Referring now to Figure 2, isolation islands 20 are formed in isolation regions 15a, 15c and 15e. Several versions of oxide isolation have been developed commercially. Generally, they include surrounding active device regions with thick layers of silicon dioxide, also called field oxide. The isoplanar process as set forth in U.S. Patent No. 3,648,125 is one such process. In the isoplanar process, silicon dioxide is grown from the silicon substrate by application of an oxidizing agent such as oxygen or water vapour at a temperature in the range of 900°—1250°C. In one embodiment, a 1.8 μ layer of isolation oxide is grown by subjecting the substrate to a temperature of 1000°C. in a wet oxygen ambient for 16 hours. The general thermal oxidation kinetics of this silicon dioxide growth have been reported previously. See B. E. Deal and A. S. Grove, "General Relationship for the Thermal Oxidation of Silicon", *Journal of Applied Physics*, V. 36, No. 12, pp. 3770—3778 (1965). The silicon dioxide grows into and rises above the surface of the substrate to form isolation islands 20a, 20c and 20e which surround (in a three-dimensional structure) active device regions 15b and 15d. The predeposited field implant moves into the substrate ahead of the expanding mass of silicon dioxide and, due to the elevated temperature, is dispersed even further into the substrate as shown by region 17c of Figure 3. Oxidation masking material 14 serves to prevent oxidation in the active device regions 15b and 15d. After formation of isolation islands 20, the masking material 14 along with the underlying silicon dioxide 12 is stripped by well-known etching techniques.

Next, a masking step as evidenced by a layer 21 of photoresist is performed to permit the predeposition of impurities in the p-well region. Then, both p-type and n-type impurities are introduced to the substrate and thermally driven in. This counterdoping procedure produces a highly desirable doping profile. The formation of this profile is described in detail in application 21285/75 (Serial No. 1,499,548). Briefly, a p-type impurity, e.g., boron, is implanted and thermally driven into the substrate to a depth of about 10 μ. Then a lesser amount of an n-type impurity, e.g., arsenic, is implanted and thermally driven into the substrate to a depth of about 4 μ. Alternatively, the two impurities are predeposited and driven in together. The arsenic counterdopes the boron to produce the composite concentration profile. The concentration of the p-type impurities in the profile achieved is great enough deep within the well so that the inversion threshold underneath the thick field oxide between the n-type substrate and the n-type source/drain regions of the n-channel device is suitably high and is low enough between the n-type source/drain regions of the n-channel device so that the n-channel device will operate at a suitably low threshold voltage. After the p-well drive-in, a layer of insulating material 30b and 30d is thermally grown on the major surface of substrate 10 in active device regions 15b and 15d. A layer of gate-forming conductive material 31 such as appropriately doped polycrystalline silicon is then formed over all regions of the device. As is well known in the semiconductor fabrication art, polycrystalline silicon can be used as a conductor of holes if impregnated with a p-type impurity, or as a conductor of electrons if impregnated with an n-type impurity. In the process and structure of the present invention, polycrystalline silicon serves as a primary layer of electrical interconnection of a double-layer device with aluminum serving as the upper or second layer.

Referring now to Figure 4, a masking step has been performed to define conductive material 31 and gate oxide 30b and 30d and thereby produce insulated gate electrodes 34 and 35. Then, a p-type impurity is indiscriminately introduced to the four source/drain diffusion regions 37, 38, 39 and 40. After predeposition they repose at a relatively shallow depth on the order of .2—.3 μ beneath the major surface of the substrate. In effect, the gate electrode structures serve as a mask so that the edges of the source/drain regions are self-aligned with the edges of the electrodes. The other edges of the source/drain diffusion regions are masked

by the islands of field oxide. The beneficial effects of self-aligned structures such as lowered capacitance and increased packing density will ultimately be obtained. At this point, however, the source/drain regions are not yet formed as p-type impurities are only predeposited in the four regions.

The specific character of the source/drain regions 39 and 40 of the n-channel device to be formed is then established by reoxidizing the exposed substrate areas of the p-channel and n-channel devices by thermal growth to produce thin oxide layers 32 and 33 (Figure 4). The thickness of the thermally grown oxide is capable of careful control and does not need to be densified as does commercially deposited silicon oxide. Thin layer 33 over source/drain regions 39 and 40 is then removed. An n^+-type impurity is then predeposited, for example by diffusion or ion implantation, in source/drain regions 39 and 40 to counterdope the p^+-type impurity previously predeposited. Polycrystalline silicon gate 35 again serves as a mask so that the boundaries of source/drain regions 39 and 40 remain self-aligned with the edges of gate electrode 35. If the n^+-type impurity is phosphorus and if diffusion is used to accomplish predeposition, the phosphorus will react with thin reoxidation layer 32 to form phosphosilicate glass during the elevated temperature segment of the predeposition cycle. This glass is readily removed by etching, e.g. in a hydrofluoric bath. The presence of the reoxidation layer 32 effectively eliminates the necessity for an additional masking step to achieve the character of the p^+-source/drain regions of the p-channel device. The relative concentrations of the p-type impurity and the n-type impurity introduced to source/drain regions 39 and 40 are such that a composite n^+ profile is achieved after thermal drive-in.

Referring now to Figure 6, a layer 43 of additional electrical insulating material is formed across the surface of the structure. This material may be chemically deposited silicon dioxide. When it is defined to open up source/drain regions 37, 38, 39 and 40 for subsequent electrical contact formation, the unreacted portion of reoxidation layer 32 is also removed. The amount of reoxidation layer 32 to be removed at this point is controllably small since the original thickness of reoxidation layer 32 was carefully controlled. Thus, no deleterious undercutting of the oxide islands adjacent source/drain regions 39 and 40 occurs due to the additional etch time required to remove the unreacted portion of reoxidation layer 32.

The standard thermal drive-in step is then completed. Typically the substrate is heated to a temperature of 1070°C. for a period of about thirty minutes. This drive-in is accomplished at the same time that phosphorus gettering is performed by passing a gas containing $POCl_3$, O_2 and N_2 over the substrate. The thermal drive-in of the source/drain diffusion regions 37, 38, 39 and 40 does not significantly affect the previously formed p-well 23d nor the n^+ field implant 17c because it previously was driven in at a temperature of 1200°C. for a period of about 16 hours. As can be seen, the depth of source/drain regions 37 and 38 is equal to the penetration of the p^+-type impurities in source/drain regions 39 and 40. In regions 39 and 40, however, the p^+-type impurities have lost their identity. The character of source/drain diffusion regions 39 and 40 is n^+-type because, as stated above, the n^+-type impurities counter-dope the p^+-type impurities. In essence the counterdoping procedure eliminates the separate masking and impurity-introduction steps normally required to produce the n^+-source/drain regions of the n-channel device.

A further advantage of the counterdoping procedure is the acquired ability to carefully control the characteristics of the composite doping profile of the n^+-source/drain regions at their boundary with the p-well, a PN junction. By reference to the idealized doping curves and PN junction of Figures 8 and 9, it can be seen that the control allows the breakdown voltage across the junction to be tailored. Figure 8 shows the concentration of n- and p-type impurities as a function of depth beneath the surface of a constant background (denoted by horizontal dotted line) substrate for a particular source/drain region. The composite doping profile is shown as a dotted line. The depth of the junction is the point at which the curve indicating the n-type impurity intersects the level of the background concentration, shown to be about 2×10^{16} atoms/cm^3. It is evident that the shape of either impurity curve can be altered by varying the amount of impurities predeposited and the conditions of thermal drive-in and that the composite doping profile can be altered thereby. Figure 9 illustrates pictorially the effect that the character of the slope of the doping profile has on the location of the space charge region about a PN junction. Generally, for a given breakdown voltage, the space charge region about a PN junction 61 will extend into the substrate as indicated by curve 60 and up into the diffused region as shown by curve 62. As is well known and as stated above, broadening the space charge

region will raise the avalanche junction breakdown voltage. This space charge region can be extended further into the substrate if the background concentration, i.e., the substrate doping, is reduced, or further into the diffused region as shown by dotted line 63 if either the diffused region is more lightly doped or the slope of the doping profile in the diffused region is reduced adjacent to the PN junction. The doping of the substrate cannot be varied solely to raise a particular avalanche breakdown voltage as other circuit design requirements must be met. And the magnitude of the source/drain region doping must be appropriate to achieve a suitable device threshold voltage. With a counterdoping procedure, however, the shape of the tail end of the composite doping profile can be tailored by adjusting the relative concentrations of the majority, e.g., n-type, and minority, e.g., p-type, impurities. The slope of the doping profile can then be reduced adjacent the PN junction. This is shown by the shape of the tail end of the composite coping profile of Figure 8. Such shaping will broaden the space charge region from the width w to the width w' as shown in Figure 9. Thus, the process of the present invention can be used to vary the avalanche junction breakdown voltage across the boundary of the source/drain region and the substrate or p-well and achieve a reduced value therefor.

An insulated gate complementary field effect device fabricated by the process of the present invention is shown in Figure 7. Metal connectors 50 and 51 have been applied and defined to interconnect source/drain region 38 of the p-channel device with source/drain region 39 of the n-channel device and to provide external electrical communication with the source/drain region 37 of the p-channel device and with source/drain region 40 of the n-channel device. In most commercial products a particular complementary field-effect transistor will be dedicated to perform a specified function in a particular circuit and will be electrically coupled in accordance wih circuit requirements. The strcture fabricated by the process of the present invention is functionally equivalent to the structure described in application 21285/75 (Serial No. 1,499,548), but requires fewer process steps. The counterdoping of at least one of the source/drain regions has resulted in the simplification of the process sequence with the added feature of tailoring the composite doping profile to increase avalanche breakdown voltage across the PN junction. The use of thermally grown silicon dioxide as a mask results in further simplification.

WHAT WE CLAIM IS:—

1. A process for fabricating a complementary insulated gate field-effect transistor structure having n-channel and p-channel devices in the same semiconductor substrate, the method having the steps of forming a well of a first conductivity type in a substrate of a second and opposite conductivity type, forming a conductor-insulator-semiconductor field-effect device having a second channel conductivity type within said well and forming a conductor-insulator-semiconductor field-effect device having a first channel conductivity type in said substrate, forming oxide-isolation regions in said substrate substantially surrounding and contiguous with said conductor-insulator-semiconductor devices, the source/drain regions of said conductor-insulator-semiconductor devices being formed by introducing an impurity of a first conductivity type into the source/drain regions of both of said devices, and introducing an impurity of a second conductivity type opposite to said first conductivity type into the source/drain regions of said device having said second channel conductivity type, the concentration of said impurity of said second conductivity type in said source/drain regions of said device having said second channel conductivity type being greater than the concentration of said impurity of said first conductivity type so that the impurity of said second conductivity type counterdopes said impurity of said first conductivity type to produce source/drain regions of said second conductivity type.

2. A process as claimed in Claim 1 in which the first conductivity type is p, said second and opposite conductivity type is n, said first channel conductivity type is p-channel and said second channel conductivity type is n-channel.

3. A process as claimed in Claim 2 having the step of introducing said p-type impurity into the source/drain regions of both of said devices by implanting ions of said p-type conductivity.

4. A process as claimed in Claim 3 in which the impurity of n-conductivity type is introduced to the source/drain region of said device having said n-channel conductivity type by implanting ions of said n-conductivity type.

5. A process as claimed in Claim 2 in which the impurity of a p-conductivity type is introduced to the source/drain regions of both of said devices by predepositing the p-conductivity type impurity by diffusion and subsequently thermally driving in the p-conductivity type impurity.

6. A process as claimed in Claim 5 in which the n-conductivity type impurity is

region will raise the avalanche junction breakdown voltage. This space charge region can be extended further into the substrate if the background concentration, i.e., the substrate doping, is reduced, or further into the diffused region as shown by dotted line 63 if either the diffused region is more lightly doped or the slope of the doping profile in the diffused region is reduced adjacent to the PN junction. The doping of the substrate cannot be varied solely to raise a particular avalanche breakdown voltage as other circuit design requirements must be met. And the magnitude of the source/drain region doping must be appropriate to achieve a suitable device threshold voltage. With a counterdoping procedure, however, the shape of the tail end of the composite doping profile can be tailored by adjusting the relative concentrations of the majority, e.g., n-type, and minority, e.g., p-type, impurities. The slope of the doping profile can then be reduced adjacent the PN junction. This is shown by the shape of the tail end of the composite coping profile of Figure 8. Such shaping will broaden the space charge region from the width w to the width w' as shown in Figure 9. Thus, the process of the present invention can be used to vary the avalanche junction breakdown voltage across the boundary of the source/drain region and the substrate or p-well and achieve a reduced value therefor.

An insulated gate complementary field effect device fabricated by the process of the present invention is shown in Figure 7. Metal connectors 50 and 51 have been applied and defined to interconnect source/drain region 38 of the p-channel device with source/drain region 39 of the n-channel device and to provide external electrical communication with the source/drain region 37 of the p-channel device and with source/drain region 40 of the n-channel device. In most commercial products a particular complementary field-effect transistor will be dedicated to perform a specified function in a particular circuit and will be electrically coupled in accordance wih circuit requirements. The strcture fabricated by the process of the present invention is functionally equivalent to the structure described in application 21285/75 (Serial No. 1,499,548), but requires fewer process steps. The counterdoping of at least one of the source/drain regions has resulted in the simplification of the process sequence with the added feature of tailoring the composite doping profile to increase avalanche breakdown voltage across the PN junction. The use of thermally grown silicon dioxide as a mask results in further simplification.

WHAT WE CLAIM IS:—

1. A process for fabricating a complementary insulated gate field-effect transistor structure having n-channel and p-channel devices in the same semiconductor substrate, the method having the steps of forming a well of a first conductivity type in a substrate of a second and opposite conductivity type, forming a conductor-insulator-semiconductor field-effect device having a second channel conductivity type within said well and forming a conductor-insulator-semiconductor field-effect device having a first channel conductivity type in said substrate, forming oxide-isolation regions in said substrate substantially surrounding and contiguous with said conductor-insulator-semiconductor devices, the source/drain regions of said conductor-insulator-semiconductor devices being formed by introducing an impurity of a first conductivity type into the source/drain regions of both of said devices, and introducing an impurity of a second conductivity type opposite to said first conductivity type into the source/drain regions of said device having said second channel conductivity type, the concentration of said impurity of said second conductivity type in said source/drain regions of said device having said second channel conductivity type being greater than the concentration of said impurity of said first conductivity type so that the impurity of said second conductivity type counterdopes said impurity of said first conductivity type to produce source/drain regions of said second conductivity type.

2. A process as claimed in Claim 1 in which the first conductivity type is p, said second and opposite conductivity type is n, said first channel conductivity type is p-channel and said second channel conductivity type is n-channel.

3. A process as claimed in Claim 2 having the step of introducing said p-type impurity into the source/drain regions of both of said devices by implanting ions of said p-type conductivity.

4. A process as claimed in Claim 3 in which the impurity of n-conductivity type is introduced to the source/drain region of said device having said n-channel conductivity type by implanting ions of said n-conductivity type.

5. A process as claimed in Claim 2 in which the impurity of a p-conductivity type is introduced to the source/drain regions of both of said devices by predepositing the p-conductivity type impurity by diffusion and subsequently thermally driving in the p-conductivity type impurity.

6. A process as claimed in Claim 5 in which the n-conductivity type impurity is

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introduced to the source/drain regions of said device having said n-channel conductivity type by predepositing the n-conductivity type impurity by diffusion and subsequently thermally driving in said n-conductivity type impurity.

7. A process for fabricating a complementary insulated gate field-effect transistor structure having n-channel and p-channel devices in the same semiconductor substrate substantially as herein described with reference to the accompanying drawings.

8. A complementary insulated gate field-effect transistor structure having n-channel and p-channel devices in the semiconductor substrate provided by the process of any preceding claim.

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