ISOLATION TRENCHES FOR MEMORY DEVICES

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to memory devices and in particular the present invention relates to isolation trenches for memory devices.

BACKGROUND OF THE INVENTION

Memory devices are typically provided as internal storage areas in computers. The term memory identifies data storage that comes in the form of integrated circuit chips. In general, memory devices contain an array of memory cells for storing data, and row and column decoder circuits coupled to the array of memory cells for accessing the array of memory cells in response to an external address.

One type of memory is a non-volatile memory known as flash memory. A flash memory is a type of EEPROM (electrically-erasable programmable read-only memory) that can be erased and reprogrammed in blocks. Many modern personal computers (PCs) have their BIOS stored on a flash memory chip so that it can easily be updated if necessary. Such a BIOS is sometimes called a flash BIOS. Flash memory is also popular in wireless electronic devices because it enables the manufacturer to support new communication protocols as they become standardized and to provide the ability to remotely upgrade the device for enhanced features.

A typical flash memory comprises a memory array that includes a large number of memory cells arranged in row and column fashion. Each of the memory cells includes a floating-gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed on an individual basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge on the floating gate.

Memory devices are typically formed on semiconductor substrates using semiconductor fabrication methods. The array of memory cells is disposed on the substrate. Isolation trenches formed in the substrate within the array and filled with a dielectric, e.g., shallow trench isolation (STI), provide voltage isolation on the memory array by acting to prevent extraneous current flow through the substrate between the memory cells. The isolation trenches are often filled using a physical deposition process, e.g., with high-density

plasma (HDP) oxides. However, the spacing requirements for flash memory arrays often require the isolation trenches to have relatively narrow widths, resulting in large aspect (or trench-depth-to-trench-width) ratios. The large aspect ratios often cause voids to form within the dielectric while filling these trenches using physical sputtering processes.

Filling the trenches with spin-on-dielectrics (SODs) can reduce the formation of voids within the dielectric during filling. However, spin-on-dielectrics usually have to be cured (or annealed) after they are disposed within the trenches, e.g., using a steam-oxidation process that can result in unwanted oxidation of the substrate and of layers of the memory cells overlying the substrate. To protect against such oxidation, the trenches can be lined with a nitride liner prior to filling the trenches with a spin-on-dielectric. One problem with nitride liners is that they can store trapped charges that can adversely affect the reliability of the memory cells and thus the memory device.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternatives to existing trench-fill methods.

SUMMARY

The above-mentioned problems with filling isolation trenches and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

For one embodiment, the invention provides a method of forming a portion of a memory device. The method includes forming a first dielectric plug in a portion of a trench that extends into a substrate so that an upper surface of the first dielectric plug is recessed below an upper surface of the substrate. The first dielectric plug has a layer of a first dielectric material and a layer of a second dielectric material formed on the layer of the first dielectric material. Forming a second dielectric plug of a third dielectric material on the upper surface of the first dielectric plug is included in the method.

For another embodiment, the invention provides a method of forming a portion of a memory device. The method includes lining a portion of a trench that extends into a substrate with a first dielectric layer by forming the first dielectric layer on the substrate and forming a second dielectric layer on the first dielectric layer. The method includes forming a third dielectric layer on the second dielectric layer so that the third dielectric layer fills a

portion of the trench and so that an upper surface of the third dielectric layer is located below an upper surface of the substrate. Removing a portion of the second dielectric layer to a level of the upper surface of the third dielectric layer to expose a portion of the first dielectric layer located between the upper surface of the third dielectric layer and the upper surface of the substrate is included in the method, as is forming a fourth dielectric layer within the trench so as to fill a remaining portion of the trench. A portion of the fourth dielectric layer is formed on the upper surface of the third dielectric layer and on the exposed portion of the first dielectric layer.

For another embodiment, the invention provides a memory device that has a trench that extends into a substrate. A first dielectric plug is disposed in the trench so that an upper surface of the first dielectric plug is located below an upper surface of the substrate. The first dielectric plug has a layer of a first dielectric material and a layer of a second dielectric material formed on the layer of the first dielectric material. A second dielectric plug of a third dielectric material is disposed in the trench on the upper surface of the first dielectric plug.

Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified block diagram of a memory system, according to an embodiment of the invention.

Figures 2A-2H are cross-sectional views of a portion of a memory device during various stages of fabrication, according to another embodiment of the invention.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The term wafer or substrate used in the following description includes any base semiconductor structure. Both

are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms wafer or substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

Figure 1 is a simplified block diagram of a memory system 100, according to an embodiment of the invention. Memory system 100 includes an integrated circuit memory device 102, such as a flash memory device, e.g., a NAND or NOR memory device, a DRAM, an SDRAM, etc., that includes an array of memory cells 104 and a region peripheral to memory array 104 that includes an address decoder 106, row access circuitry 108, column access circuitry 110, control circuitry 112, Input/Output (I/O) circuitry 114, and an address buffer 116. The row access circuitry 108 and column access circuitry 110 may include high-voltage circuitry, such as high-voltage pumps. Memory system 100 includes an external microprocessor 120, or memory controller, electrically connected to memory device 102 for memory accessing as part of an electronic system. The memory device 102 receives control signals from the processor 120 over a control link 122. The memory cells are used to store data that are accessed via a data (DQ) link 124. Address signals are received via an address link 126 that are decoded at address decoder 106 to access the memory array 104. Address buffer circuit 116 latches the address signals. The memory cells are accessed in response to the control signals and the address signals. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of Figure 1 has been simplified to help focus on the invention.

The memory array 104 includes memory cells arranged in row and column fashion. For one embodiment, the memory cells are flash memory cells that include a floating-gate field-effect transistor capable of holding a charge. The cells may be grouped into blocks. Each of the cells within a block can be electrically programmed on an individual basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation.

For one embodiment, memory array 104 is a NOR flash memory array. A control gate of each memory cell of a row of the array is connected to a word line, and a drain region of each memory cell of a column of the array is connected to a bit line. The memory array for NOR flash memory devices is accessed by row access circuitry, such as the row access circuitry 108 of memory device 102, activating a row of floating gate memory cells by selecting the word line connected to their control gates. The row of selected memory cells then place their data values on the column bit lines by flowing a differing current, depending upon their programmed states, from a connected source line to the connected column bit lines.

For another embodiment, memory array 104 is a NAND flash memory array also arranged such that the control gate of each memory cell of a row of the array is connected to a word line. However, each memory cell is not directly connected to a column bit line by its drain region. Instead, the memory cells of the array are arranged together in strings (often termed NAND strings), e.g., of 32 each, with the memory cells connected together in series, source to drain, between a source line and a column bit line. The memory array for NAND flash memory devices is then accessed by row access circuitry, such as the row access circuitry 108 of memory device 102, activating a row of memory cells by selecting the word line connected to a control gate of a memory cell. In addition, the word lines connected to the control gates of unselected memory cells of each string are driven to operate the unselected memory cells of each string as pass transistors, so that they pass current in a manner that is unrestricted by their stored data values. Current then flows from the source line to the column bit line through each series connected string, restricted only by the selected memory cells of each string. This places the current-encoded data values of the row of selected memory cells on the column bit lines.

Figures 2A-2H are cross-sectional views of a portion of a memory device, such as a portion of the memory device 102, during various stages of fabrication, according to another embodiment of the invention. Figure 2A depicts the portion of the memory device after several processing steps have occurred. Formation of the structure depicted in Figure 2A is well known and will not be detailed herein.

In general, the structure of Figure 2A is formed by forming a first dielectric layer 202 on a substrate 200, e.g., of silicon or the like. For one embodiment, the first dielectric layer 202 is a gate dielectric layer (or tunnel dielectric layer), such as a tunnel oxide layer. A

conductive layer 204, e.g., a layer of doped polysilicon, is formed on the first dielectric layer 202, and a hard mask layer 206 is formed on the conductive layer 204. The mask layer 206 can be a second dielectric layer, such as a nitride layer, e.g., a silicon nitride (Si_3N_4) layer.

Trenches 210 are subsequently formed through the mask layer 206, the conductive layer 204, and the first dielectric layer 202 and extend into substrate 200. This can be accomplished by patterning the mask layer 206 and etching. A third dielectric layer 212 may then be formed on portions of the substrate 200 exposed by the trenches 210 so as to line the portion of trenches 210 formed in substrate 200.

A fourth dielectric layer 220, such as a nitride layer, e.g., a silicon nitride layer, is formed on the structure of Figure 2A in Figure 2B, such as by blanket deposition, and acts as an oxidation barrier layer for one embodiment. Specifically, the fourth dielectric layer 220 is formed on an upper surface of mask layer 206 and on portions of the mask layer 206, the conductive layer 204, and the first dielectric layer 202 through which trenches 210 pass. The fourth dielectric layer 220 is also formed on the third dielectric layer 212. In this way, the fourth dielectric layer 220 lines trenches 210. For one embodiment, the third dielectric layer 212 acts to provide adhesion between substrate 200 and the fourth dielectric layer 220 and acts as a stress release layer for relieving stresses that would otherwise form between substrate 200 and the fourth dielectric layer 220. For another embodiment, the third dielectric layer 212 is a pad oxide layer and can be a thermal oxide layer. For another embodiment, the third dielectric layer 212 is, for example, of deposited silicon dioxide (SiO_2).

A fifth dielectric layer 230 is deposited within each of the trenches 210 on the fourth dielectric layer 220 in Figure 2C to either fill or partially fill trenches 210. For one embodiment, the fifth dielectric layer 230 is spin-on dielectric (SOD) material 230, such as a spin-on glass, hydrogen silsesquioxane (HSQ), hexamethyldisiloxane, octamethyltrisiloxane, etc. The fifth dielectric layer 230 is then cured (or annealed), e.g., using a steam-oxidation process, if necessary. For one embodiment, the fourth dielectric layer 204 acts to prevent oxidation of the substrate 200 and the conductive layer 204 during curing. In Figure 2D, a portion of the fifth dielectric layer 230 is removed, such as by etching in an etch-back process, so that an upper surface of the fifth dielectric layer 230 is recessed within the respective trenches 210, e.g., below an upper surface of substrate 200, exposing a portion of the fourth dielectric layer 220 lining each of trenches 210.

A portion of the fourth dielectric layer 220 is selectively removed in Figure 2E, e.g., using a controlled wet etch, to a level of the upper surface of the fifth dielectric layer 230 such that a remaining portion of the fourth dielectric layer 220 is interposed between the fifth dielectric layer 230 and the third dielectric layer 212. That is, the fourth dielectric layer 220 is removed from an upper surface of the mask layer 206, and the exposed portion of the fourth dielectric layer 220 located within each of trenches 210 is removed. This exposes the upper surface of the mask layer 206, the portions of the mask layer 206, the conductive layer 204, and the first dielectric layer 202 through which trenches 210 pass, and a portion of the third dielectric layer 212 lying between the upper surface of substrate 200 and the upper surface of the fifth dielectric layer. The remaining portions of the fourth dielectric layer 220 and the fifth dielectric layer 230 form a first dielectric plug 232 that fills a lower portion of trenches 210, as shown in Figure 2E, having an upper surface that is recessed below the upper surface of the substrate 200.

In Figure 2F, a sixth dielectric layer 240 is blanket deposited, e.g., using a physical sputtering process, over the structure of Figure 2E and fills an unfilled portion of each of trenches 210. Specifically, the sixth dielectric layer 240 is deposited on the exposed upper surface of the mask layer 206, on the exposed portions of the mask layer 206, the conductive layer 204, and the first dielectric layer 202 through which trenches 210 pass, on the portion of the third dielectric layer 212 lying between the upper surface of substrate 200 and the upper surface of the fifth dielectric layer, and on the first dielectric plug 232. For one embodiment, the sixth dielectric layer 240 is of a high-density-plasma (HDP) dielectric material, such as a high-density-plasma (HDP) oxide. Note that the first dielectric plugs 232 reduce the remaining depths of trenches 210 and thus their aspect ratios for the deposition of the sixth dielectric layer 240. The reduced aspect ratios of trenches 210 act to reduce the formation of voids when depositing the sixth dielectric layer 240 within the unfilled portions of trenches 210.

A portion of the sixth dielectric layer 240 is removed from the structure of Figure 2F in Figure 2G, e.g., using chemical mechanical polishing (CMP). That is, the sixth dielectric layer 240 is removed so that the upper surface of the mask layer 206 is exposed and so that an upper surface of the sixth dielectric layer 240 within each of trenches 210 is substantially flush with the upper surface of the mask layer 206. Note that the portion of the sixth dielectric layer 240 within each of the trenches 210 forms a second dielectric plug 242

that passes through the mask layer 206, the conductive layer 204, the first conductive layer 202, extends into the substrate 200, and terminates at the first conductive plug 232. The third dielectric layer 212 is interposed between the portion of the second dielectric plug 242 and the substrate 200 and the first dielectric plug 232 and the substrate 200.

Note that the fourth dielectric layer 220 is located in the lower portion of each of trenches 210 and thus away from the layers disposed on the upper surface of substrate 200 that can be used to form memory cells. This acts to reduce problems associated with the fourth dielectric layer 220 storing trapped charges, especially when the fourth dielectric layer 220 is of nitride, that can adversely affect the reliability of the memory cells and thus the memory device.

Mask 206 is subsequently removed to expose the conductive layer 204. An intergate dielectric layer 250, e.g., such as a layer of silicon oxide, a nitride, an oxynitride, an oxide-nitride-oxide (ONO) layer, etc., is then formed on the exposed conductive layer 204. A conductive layer 260, such as a doped polysilicon layer, a metal layer, e.g., refractory metal layer, a metal containing layer, e.g., a metal silicide layer, or the like, is formed on the intergate dielectric layer 250, as shown in Figure 2H. The conductive layer 260 may include one or more conductive materials or conductive layers, a metal or metal containing layer disposed on a polysilicon layer, etc. For another embodiment, conductive layers 204 and 260 respectively form a floating gate and a control gate (or word line) of memory cells of a memory array, such as memory array 104 of Figure 1. Source/drain regions are also formed in a portion of substrate 200 not shown in Figure 2G as a part of the memory array. For one embodiment, conductive layer 204 is extended to improve the coupling of the floating gate. The trenches 210 filled with dielectric materials, as described above, act to prevent extraneous current flow through the substrate between the memory cells.

The components located in the region peripheral to memory array 104 of Figure 1 are also formed on the substrate 200, and the trenches 210 filled with dielectric materials, as described above, may be formed between the region peripheral to memory array 104 and memory array 104 and act to prevent extraneous current flow through the substrate between components of the peripheral region and memory array 104.

CONCLUSION

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.

What is claimed is:

1. A method of forming a portion of a memory device, comprising the steps of forming in a portion of a trench disposed on a substrate a dielectric filling layer having a 1st dielectric layer and a 2nd dielectric layer formed on top of the 1st dielectric layer so that the upper side surface thereof is disposed below the upper side surface of the substrate;

forming so that a 2nd dielectric filling layer consisting of a 3rd dielectric makes contact with a portion of a 4th dielectric layer and a portion of a 1st conductive layer, extending along a remaining portion of the trench running through the 4th dielectric layer formed on the upper side surface of the 1st dielectric filling layer from the upper side surface of the 1st dielectric filling layer extending upward to the upper side surface of the substrate;

forming a 5th dielectric layer on top of the 1st conductive layer after the step of forming the 2nd dielectric filling layer; and

forming a 2nd conductive layer on top of the 5th dielectric layer,

wherein the upper side surface of the 5th dielectric layer is disposed below the upper side surface of the 2nd dielectric filling layer.

2. The method of Claim 1, wherein the step of forming the 1st dielectric filling layer further comprises a step of covering a portion of the trench and forming the 1st dielectric layer on top of a 6th dielectric layer disposed on top of the substrate.

3. The method of Claim 2, wherein the step of forming the 2nd dielectric filling layer comprises a step of forming a portion of the 2nd dielectric filling layer on top of the 6th dielectric layer.

4. The method of any of Claims 1 through 3, wherein the 1st dielectric material is a nitride, the 2nd dielectric is a spin-on dielectric, and the 3rd dielectric is a high-density plasma based oxide.

5. The method of any of Claims 1 through 4, wherein the step of forming the 1st dielectric filling layer further comprises a step of curing the 2nd dielectric layer.

6. The method of Claim 5, wherein the step of curing the 2nd dielectric layer comprises an oxidation process.

7. The method of any of Claims 1-6, wherein the 4th dielectric layer is a tunnel dielectric layer.

8. The method of any of Claims 1-7, wherein the trench is formed by patterning and etching a hard mask layer disposed on top of the 1st conductive layer.

9. The method of any of Claims 1-8, wherein the step of forming the 1st dielectric filling layer comprises steps of

forming the 2nd dielectric layer on top of the 1st dielectric layer and filling the trench up to a level above the upper surface of the substrate on the 2nd dielectric layer; and

removing a portion the 2nd dielectric layer and disposing the upper side surface of the 2nd dielectric layer below the upper side surface of the substrate.

10. The method of Claim 9, wherein the step of forming the 1st dielectric filling layer further comprises a step of selectively removing a portion of the 1st dielectric layer to a level of the upper side surface of the 2nd dielectric layer.

11. The method of either of Claim 9 or Claim 10, further comprising a step of annealing the 2nd dielectric layer before the step of removing a portion of the 2nd dielectric layer.

12. The method of any of Claims 1-7 or Claims 9-11, wherein the 5th dielectric layer is an inter-gate dielectric layer.

13. The method of Claim 12, wherein the 1st conductive layer is a floating gate layer and the 2nd conductive layer is a control gate layer.

14. An integrated circuit device, comprising

a 1st dielectric filling layer, comprising

a 1st dielectric filling layer having a 1st dielectric layer and a 2nd dielectric layer formed on top of [the 1st] layer and disposed inside a trench disposed inside a substrate such that the top side surface is disposed below the top side surface of the substrate;

a 2nd dielectric filling layer consisting of a 3rd dielectric material, disposed on top of the upper side surface of the 1st dielectric filling layer inside the trench, running through a 4th dielectric layer formed on top of the upper side surface of the substrate and a 1st conductive layer formed on top of [the 4th dielectric layer] so as to make contact with a portion of the 4th dielectric layer and a portion of the 1st conductive layer;

a 5th dielectric material formed on top of the 1st conductive layer; and

a 2nd conductive layer formed on top of the 5th dielectric layer;

wherein the upper side surface of the 5th dielectric layer is disposed below the upper side surface of the 2nd dielectric filling layer.

15. The integrated circuit device of Claim 14, further comprising a 6th dielectric material disposed between the substrate and the 1st dielectric material in the 1st dielectric filling layer and disposed between a portion of the 2nd dielectric filling layer and the substrate.

16. The integrated circuit device of either Claims 14 or 15, wherein the 1st dielectric material is a nitride and the 2nd dielectric material is an annealed spin-on dielectric material.

17. The integrated circuit device of any of Claims 14 through 16, wherein the 3rd dielectric material is a high-density plasma based oxide.

18. The integrated circuit device of any of Claims 14 through 17, wherein the 4th dielectric layer is a tunneled dielectric layer, the 1st conductive layer is a floating gate layer, the 5th dielectric layer is an inter-layer dielectric layer, and the 2nd conductive layer is a control gate layer.

19. The integrated circuit device of any of Claims 14 through 18, wherein the integrated circuit device is a memory device.