

PATENT SPECIFICATION

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(54) TRAFFIC SIGNAL CONTROL SYSTEM

(71) We, OMRON TATEISI ELECTRONICS Co., a Japanese Body Corporate, of 10, Tsuchido-cho, Hanazono, Ukyo-ku, Kyoto, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to a traffic signal control system, and more particularly to a centralized traffic signal control system for controlling traffic signals at a multiplicity of intersections from a central control station.

A centralized traffic signal control wherein traffic signals over a wide territory are centrally controlled at a central control station is well known. In such a traffic signal control, a central processing unit and an electronic computer, to which traffic information at certain locations in the territory is supplied, are provided at the central control station. At the locations where traffic signals are installed, ultrasonic, inductance or earth magnetism vehicle detectors for collecting traffic information are provided. Such vehicle detectors are well known. Information regarding vehicle movements obtained by such vehicle detectors is supplied to the electronic computer. The computer computes traffic volumes, time occupancy and speed of vehicles according to the vehicle detection signals.

The computer computes traffic patterns to suit the conditions of vehicular traffic flows, and makes decision of timings of traffic signals, such as times of respective phases of traffic signals. Such times of phases of traffic signals are counted by the computer. Each time the computer counts out the respective computed values, a signal for advancing the phase of traffic signals is transmitted to the traffic signals. The indication of the traffic signals is switched over in accordance with the signal

transmitted from the central control station.

In the traffic signal control as above described, since the information of traffic flows over a wide territory is continuously supplied to the computer, it is possible to systematically control traffic signals at a multiplicity of intersections.

However, if the computer fails, the systematic control of a multiplicity of traffic signals can no longer be performed. Therefore, a fail-safe apparatus, which continues, upon failure of the computer, to perform a systematic control of the traffic signals according to the traffic control pattern based on pre-set program therein, is provided at the central control station. This fail-safe apparatus, as well as the computer, counts indication times of traffic signals and transmits signals for advancing phases of traffic signals. When the computer fails, each traffic signal is switched according to the signals for advancing phases from the fail-safe device, instead of the signals from the computer. In the fail-safe apparatus, one traffic control pattern may be pre-set, or two or three traffic control patterns, for selection which are selected according to the time of day may be pre-set. The fail-safe apparatus counts the indication times independent of the computer during the normal operation of the computer. The phase advancing signals generated from the fail-safe apparatus are not supplied to the traffic signals during the normal operation of the computer.

When the computer fails, the phase advance signals generated by the fail-safe apparatus are supplied to the traffic signals. However, since the count of the indication times by the fail-safe apparatus is performed independent of the count by the computer, it takes a certain time for transferring the control of the traffic signals by the computer to the control by the fail-safe

apparatus. Namely, if the computer fails within a short time after right-of-way of a certain main street has been given and the count of time by the fail-safe apparatus is, at that time, approaching a value to finish the right-of-way of the main street, then the right-of-way of the main street initiated by the computer will be terminated within a very short time by the phase advance signal from the fail-safe apparatus. Accordingly, in the prior art, each traffic signal was disconnected from the central control station at the time of failure of the computer, and controlled independently for a certain time by a corresponding local controller installed at the corresponding intersection, and the control by the fail-safe apparatus was commenced at the time when the phase or indication of the fail-safe apparatus coincided with that of the local controller.

As can be understood from the above description, during the time when the traffic signals are disconnected from the central control station, the systematic control of the traffic signals cannot be performed. Thus the traffic flow over a wide territory may be very much confused for a certain time upon the failure of the computer.

The object of the present invention is to provide a traffic signal control system which can smoothly control traffic flows over a wide territory by immediately transferring the control of traffic signals by electronic computer to the control by fail-safe apparatus upon failure of computer.

According to the invention, therefore, there is provided a traffic signal control system for controlling traffic signals at a multiplicity of inter-sections, comprising,

a computer for counting times of phases of traffic signals and generating signals for advancing phases of the traffic signals upon each countout of the times of phases,

a fail-safe apparatus, in which required times of phases of the traffic signals are set, and to which said signals generated by said computer are supplied,

wherein, in operation said fail-safe apparatus commences the count of times in synchronism with said signals from said computer, and generates signals for advancing the phases of said traffic signals in synchronism with the countout of said times of phases,

and switch means for transmitting to said traffic signals said signals from said computer when said computer is normally operating, and transmitting said signals from said fail-safe apparatus when said computer has failed.

An embodiment of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a traffic signal control system in accordance with the invention;

Fig. 2 is a block diagram illustrating in greater detail the construction of the fail-safe apparatus in the system of Fig. 1;

Fig. 3 is an explanatory drawing showing a synchronous time counting operation of the computer and the fail-safe apparatus;

Fig. 4 is an explanatory drawing showing the manner of control before and after failure of the computer, and

Fig. 5 is an explanatory drawing showing the mutual relationship of phase advance signals for adjacent traffic signals.

In Fig. 1, a computer is shown as a block 100, and a fail-safe apparatus is shown as a block 200. A phase advance signal SC generated by the computer 100 is supplied to one input terminal of respective gate circuits 300, 301 and 302. A signal S1 is supplied to the other input terminal of the respective gate circuits 300, 301 and 302. The phase advance signal SC supplied to the input terminals of the gate circuits 300, 301 and 302 appears at the output terminals thereof according to presence of the signal S1. The output signals of the gate circuits 300, 301 and 302 are supplied to OR gates 400, 401 and 402. The signal S1 is present when the computer 100 is normally operating, and is not present when the computer 100 fails.

A phase advance signal SF generated by the fail-safe apparatus 200 is supplied to one input terminal of respective AND gates 500, 501 and 502. The signal S1 is supplied to the other input terminal of the respective AND gates 500, 501 and 502. The signal SF generated by the fail-safe apparatus 200 appears at the output terminals of the AND gates 500, 501 and 502 when the signal S1 is absent. The output signals of the gate circuits 500, 501 and 502 are supplied to the other input terminal of the respective OR gates 400, 401 and 402.

The output signals of the OR gates 400, 401 and 402 are transmitted to corresponding traffic signals 600, 601 and 602 through transmission lines 700, 701 and 702.

Accordingly, the indications of the traffic signals are switched, when the computer 100 is operating normally, in accordance with the phase advance signal SC generated by the computer 100, and are switched, when the computer 100 fails in accordance with the phase advance signal SF generated by the fail-safe apparatus 200.

In the embodiment shown in Fig. 1, the fail-safe apparatus 200 is connected to the computer 100 through a control line CL and a bus line BL. When the computer 100 is operating normally, control parameters computed by the computer 100 are supplied



to the fail-safe apparatus 200.

Fig. 2 shows the fail-safe apparatus 200. Registers 1, 2, 3, 4, 5 and 6 are provided in the fail-safe apparatus 200 for setting the respective times of phases of the traffic signals. The data to be stored in the registers 1, 2, 3, 4, 5 and 6 is transmitted via a first bus line BL1 from the computer 100. The computer 100 is connected to one input terminal of respective AND gates 21, 22, 23, 24, 25 and 26 through bus line BL1, and also is connected to the other input terminal of the respective AND gates 21 to 26 through the first control line CL1. The output terminals of the AND gates 21 to 26 are respectively connected to the input terminals of the registers 1 to 6. The data signals from the computer 100 are conveyed on the bus line BL1 and appear at the output terminals of the AND gates 21 to 26 when a signal is supplied to the respective other input terminals thereof from the computer 100 through the control line CL1. Therefore, respective values of phase times computed by the computer 100 are stored in the registers 1, 2, 3, 4, 5 and 6 every period of, for example, five minutes. In the present embodiment, the value of the time of first phase is stored in the register 1, the value of the time of second phase is stored in the register 2, and in sequence the value of the time of sixth phase is stored in the register 6.

A counter 7 is provided for counting the respective times of phases. The counter 7 advances in accordance with clock pulses generated by a clock pulse generator 8, and is reset each time a counter 9 advances. The clock pulses generated by the generator 8 are supplied to the input terminal of a frequency divider 10. A decoder 11 is provided for controlling the divider 10, and the divider 10 generates at its output terminal pulse signals by dividing the frequency of the clock pulses by the value instructed by the decoder 11. The decoder 11 is controlled by the computer 100 through a bus line BL2. The pulse signals appearing at the output terminal of the divider 10 are called "per-cent pulses." The output terminal of the divider 10 is connected to input terminals of gate circuits 12 and 13. The output terminals of the gate circuits 12 and 13 are connected to input terminal of OR gate 14, and the output terminal of the OR gate 14 is connected to the input terminal of the counter 7.

The signal S1 is supplied to the other terminals of the gate circuits 12, 13. The set output terminal of a flip-flop 15 is connected to the remaining input terminal of the gate circuit 13.

Accordingly, when the computer 100 is operating normally, the counter 7 advances stepwise in accordance with the per-cent

pulses with the flip-flop 15 being set. When the computer 100 fails, the counter 7 advances in accordance with the per-cent pulses regardless of the state of the flip-flop 15.

The flip-flop 15 is set by the signal SC transmitted from the computer 100. The signal SC is also supplied to the input terminal of OR gate 16. The output terminal of the OR gate 16 is connected to the reset terminal of the counter 7 and also to the counter 9. The output terminal of the counter 9 is connected to one input terminal of respective AND gates 31, 32, 33, 34, 35 and 36. The other input terminal of the respective AND gates 31, 32, 33, 34, 35 and 36 is connected to respective output terminals of the registers 1, 2, 3, 4, 5 and 6 respectively. The data signals stored in the registers 1, 2, 3, 4, 5 and 6 appear at the output terminals of the AND gates 31, 32, 33, 34, 35 and 36, respectively, in accordance with the supply of output signals from the counter 9 to the respective other input terminals of the AND gates 31 to 36. The output signals of the AND gates 31 to 36 are connected to one input terminal of a coincidence circuit 17. The output terminal of the counter 7 is connected to the other input terminal of the coincidence circuit 17. A signal appears at the output terminal of the coincidence circuit 17 upon coincidence of the count value of the counter 7 with the data signal from the AND gates 31, 32, 33, 34, 35 and 36. The output terminal of the coincidence circuit 17 is connected to the input terminal of a gate circuit 500 as well as to the reset input terminal of the flip-flop circuit 15.

The counter 9 advances stepwise in accordance with the output of the OR gate 16, and the output of the counter 9 in each stage opens a corresponding one of the AND gates 31 to 36 in sequence. Each time the counter 7 counts out the time stored in one of the registers 1 to 6, a signal appears at the terminal of the coincidence circuit 17. The signal thus appears each time one of the time values stored in the registers 1 to 6 has elapsed.

In the present embodiment, the time of each phase computed by the computer is set in the registers 1 to 6 respectively, and the times of the phases are counted successively in the computer 100. The computer 100 generates the signals SC as it counts out the times of respective phases. Since the counter 7 is reset by the signal SC, the signal at the output terminal of the coincidence circuit 17 appears simultaneously with the signal SC generated by the computer 100.

As shown in Fig. 3(A), if, for any reason, the signal SC from the computer 100 is generated, during a phase (n), at the time t_1 earlier than a time t_2 where the signal

appears from the coincidence circuit 17, then the counter 7 is cleared at the time t_1 , and at the same time the counter 9 is advanced. Accordingly, in the next phase (n+1), both the advance signal SC from the computer 100 and the output signal of the coincidence circuit 17 are generated at a same time t_2 . On the other hand, as shown in Fig. 3(B), if the output signal of the coincidence circuit 17 appears at a time t_1 , earlier than a time t_2 where the signal SC is generated by the computer 100, then the flip-flop is reset at the time t_1 thereby the percent pulses are no more supplied to the counter 7. And later on, the counter 7 is reset and at the same time the flip-flop 15 is set by the signal SC generated by the computer 100 at a time t_2 . Accordingly, at the next phase (n+1), both the advance signal SC by the computer 100 and the output signal of the coincidence circuit 17 appear at a same time t_3 .

As above described, when the computer 100 is operating normally, the counter 9 is advanced by the advance signal SC, and the count of time by counter 7 and the count of time by the computer 100 are commenced simultaneously, and accordingly, it will be understood that the time when the signal SC is generated by the computer 100 and the time when the output signal of the coincidence circuit 17 appears are in coincidence in every phase. Therefore, even if the computer 100 fails at a time t_0 , as shown in Fig. 4, since the phase of the counter 9 provided in the fail-safe apparatus 200 is the same as that of the traffic signal, and the value of time count of the counter 9 in that phase is equal to that of the computer 100 and, the control of the traffic signals 600, 601, 602 can be switched from control by the computer 100 to control by the fail-safe apparatus without any troubles.

In the above, the description has been made in connection with the traffic signal at one intersection. However, as is well known by those skilled in the art, the signal SC from the computer 100 is transmitted to the traffic signals at adjacent intersections with offset value OFV suited to the traffic flow. The mutual relationships between phase advance signals transmitted to those adjacent intersections are shown in Fig. 5. Namely, after the phase advance signal SCO has been transmitted to the traffic signal 500 shown in Fig. 1, the phase advance signal SC1 is transmitted to the adjacent traffic signal 501 with offset value OFV1 in that phase. Similarly, after the phase advance signal SC1 has been transmitted to the traffic signal 501, the phase advance signal SC2 is transmitted to the adjacent traffic signal 502 with offset value OFV2 in that phase. In this manner, the traffic signals are

systematically controlled.

Since the relationships between the phase advance signals generated by the computer 100 and those generated by the fail-safe apparatus 200 are as described above, the systematic control of the adjacent traffic signals can be realized immediately when the computer 100 fails.

Further, a third bus line BL3 is provided for the purpose of adjusting the phase of the counter 9, at a desired time, in coincidence with the phase of traffic signals instructed by the computer 100.

In the above described embodiment, the setting of the registers 1 to 6 is performed by the computer 100. However, it may be so constructed that the setting of the registers 1 to 6 is performed manually. The values to be set in the registers 1 to 6 are not necessarily in coincidence with the phase times computed by the computer 100. The only one condition necessary is that the sum of the data to be set in the registers 1 to 6 is equal with respect to the respective intersections to be systematically controlled.

WHAT WE CLAIM IS:

1. A traffic signal control system for controlling traffic signals at a multiplicity of inter-sections, comprising;

a computer for counting times of phases of traffic signals and generating signals for advancing phases of the traffic signals upon each countout of the times of phases,

a fail-safe apparatus, in which required times of phases of the traffic signals are set, and to which said signals generated by said computer are supplied,

wherein, in operation said fail-safe apparatus commences the count of times in synchronism with said signals from said computer, and generates signals for advancing the phases of said traffic signals in synchronism with the countout of said times of phases,

and switch means for transmitting to said traffic signals said signals from said computer when said computer is normally operating, and transmitting said signals from said fail-safe apparatus when said computer has failed.

2. A traffic signal control system according to claim 1, wherein said times of phases are set in said fail-safe apparatus by said computer.

3. A traffic signal control system according to claim 1, wherein said times of phases are set in said fail-safe apparatus manually.

4. A traffic signal control system according to claim 1, wherein said fail-safe apparatus comprises;

first means in which times of phases are set,

second means for counting clock pulses, and

appears from the coincidence circuit 17, then the counter 7 is cleared at the time t_1 , and at the same time the counter 9 is advanced. Accordingly, in the next phase (n+1), both the advance signal SC from the computer 100 and the output signal of the coincidence circuit 17 are generated at a same time t_2 . On the other hand, as shown in Fig. 3(B), if the output signal of the coincidence circuit 17 appears at a time t_1 earlier than a time t_2 where the signal SC is generated by the computer 100, then the flip-flop is reset at the time t_1 thereby the percent pulses are no more supplied to the counter 7. And later on, the counter 7 is reset and at the same time the flip-flop 15 is set by the signal SC generated by the computer 100 at a time t_2 . Accordingly, at the next phase (n+1), both the advance signal SC by the computer 100 and the output signal of the coincidence circuit 17 appear at a same time t_2 .

As above described, when the computer 100 is operating normally, the counter 9 is advanced by the advance signal SC, and the count of time by counter 7 and the count of time by the computer 100 are commenced simultaneously, and accordingly, it will be understood that the time when the signal SC is generated by the computer 100 and the time when the output signal of the coincidence circuit 17 appears are in coincidence in every phase. Therefore, even if the computer 100 fails at a time t_0 , as shown in Fig. 4, since the phase of the counter 9 provided in the fail-safe apparatus 200 is the same as that of the traffic signal, and the value of time count of the counter 9 in that phase is equal to that of the computer 100 and, the control of the traffic signals 600, 601, 602 can be switched from control by the computer 100 to control by the fail-safe apparatus without any troubles.

In the above, the description has been made in connection with the traffic signal at one intersection. However, as is well known by those skilled in the art, the signal SC from the computer 100 is transmitted to the traffic signals at adjacent intersections with offset value OFV suited to the traffic flow. The mutual relationships between phase advance signals transmitted to those adjacent intersections are shown in Fig. 5. Namely, after the phase advance signal SCO has been transmitted to the traffic signal 500 shown in Fig. 1, the phase advance signal SC1 is transmitted to the adjacent traffic signal 501 with offset value OFV1 in that phase. Similarly, after the phase advance signal SC1 has been transmitted to the traffic signal 501, the phase advance signal SC2 is transmitted to the adjacent traffic signal 502 with offset value OFV2 in that phase. In this manner, the traffic signals are

systematically controlled.

Since the relationships between the phase advance signals generated by the computer 100 and those generated by the fail-safe apparatus 200 are as described above, the systematic control of the adjacent traffic signals can be realized immediately when the computer 100 fails.

Further, a third bus line BL3 is provided for the purpose of adjusting the phase of the counter 9, at a desired time, in coincidence with the phase of traffic signals instructed by the computer 100.

In the above described embodiment, the setting of the registers 1 to 6 is performed by the computer 100. However, it may be so constructed that the setting of the registers 1 to 6 is performed manually. The values to be set in the registers 1 to 6 are not necessarily in coincidence with the phase times computed by the computer 100. The only one condition necessary is that the sum of the data to be set in the registers 1 to 6 is equal with respect to the respective intersections to be systematically controlled.

WHAT WE CLAIM IS:

1. A traffic signal control system for controlling traffic signals at a multiplicity of inter-sections, comprising,

a computer for counting times of phases of traffic signals and generating signals for advancing phases of the traffic signals upon each countout of the times of phases,

a fail-safe apparatus, in which required times of phases of the traffic signals are set, and to which said signals generated by said computer are supplied,

wherein, in operation said fail-safe apparatus commences the count of times in synchronism with said signals from said computer, and generates signals for advancing the phases of said traffic signals in synchronism with the countout of said times of phases,

and switch means for transmitting to said traffic signals said signals from said computer when said computer is normally operating, and transmitting said signals from said fail-safe apparatus when said computer has failed.

2. A traffic signal control system according to claim 1, wherein said times of phases are set in said fail-safe apparatus by said computer.

3. A traffic signal control system according to claim 1, wherein said times of phases are set in said fail-safe apparatus manually.

4. A traffic signal control system according to claim 1, wherein said fail-safe apparatus comprises;

first means in which times of phases are set,

second means for counting clock pulses, and



(14)

third means for generating phase advance signals upon coincidence of the count of said second means with said set value in said first means.

- 5 5. A traffic signal control system according to claim 4, further provided with means for interrupting the supply of said clock pulses to said second means until said phase advance signal by said computer is
10 generated after said phase advance signal

by said third means has been generated.

6. A traffic signal control system substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

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