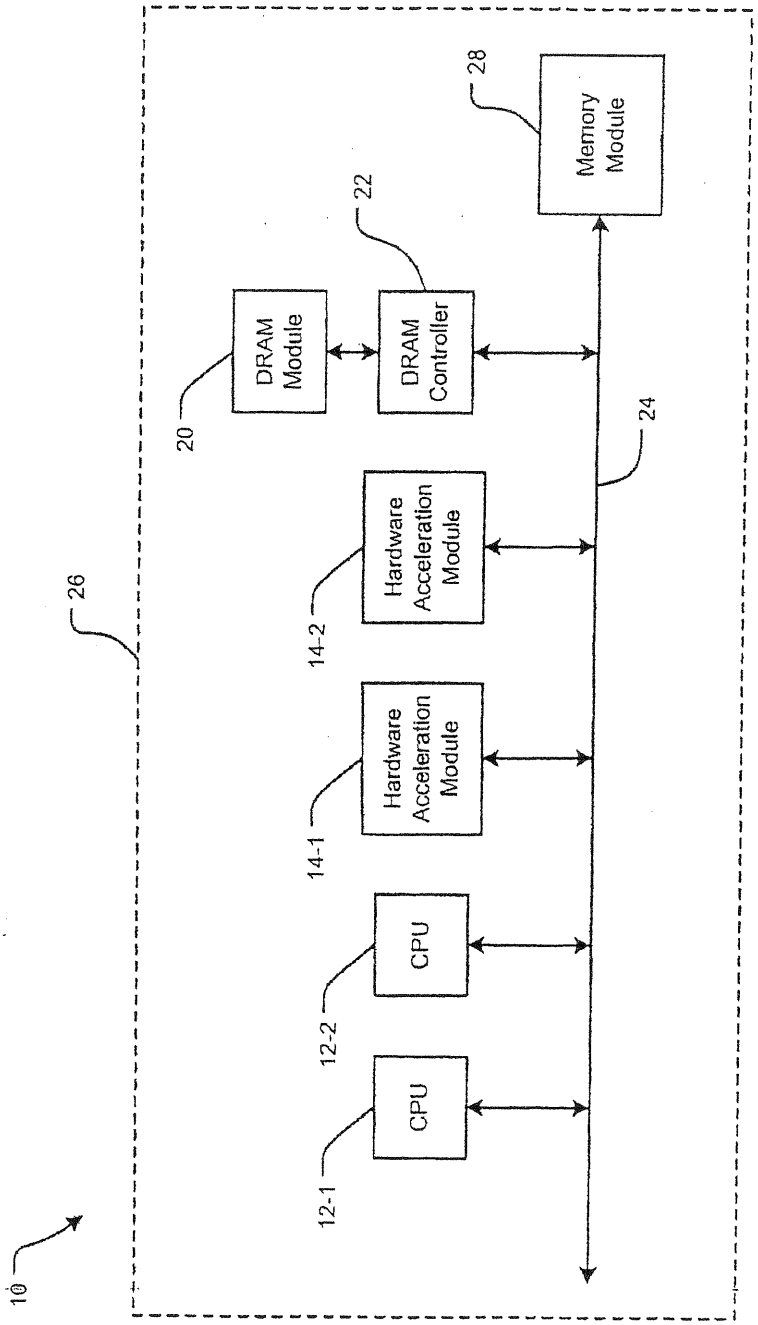


FIG. 1
(Prior Art)

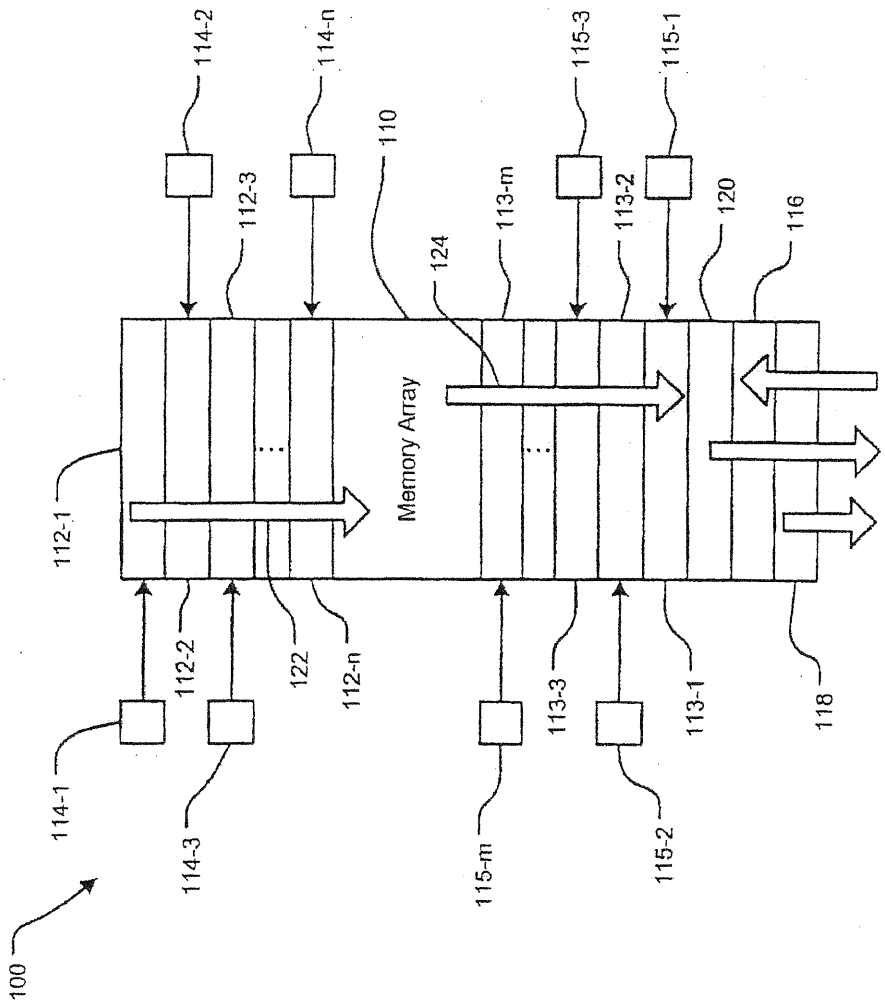

100
114-1
114-3
112-2
112-3
114-2
114-n
112-1
122
112-n
110
Memory Array
124
115-m
113-3
113-m
115-2
113-2
115-3
113-1
115-1
120
116
118

FIG. 2

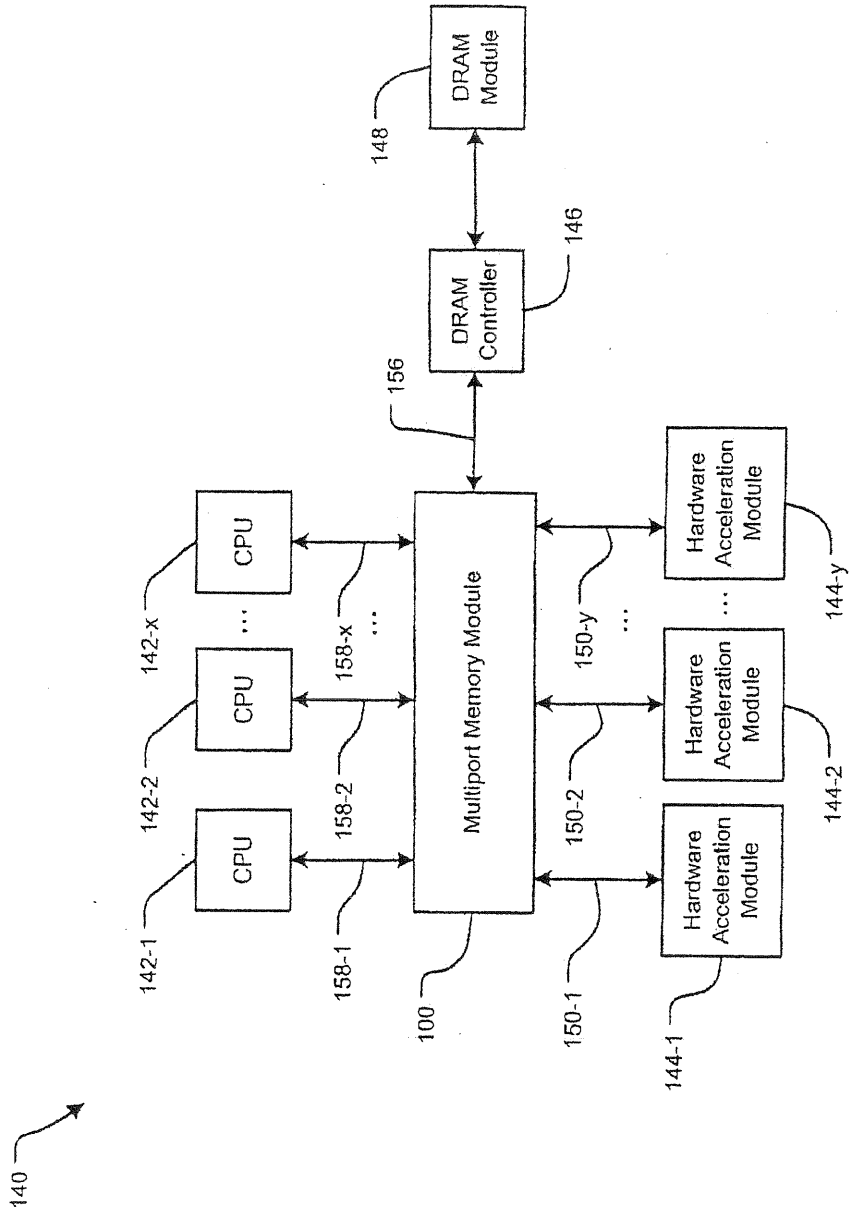

140
142-1
CPU
142-2
CPU
142-x
CPU
158-1
158-2
158-x
100
Multiport Memory Module
150-1
150-2
150-y
144-1
Hardware Acceleration Module
144-2
Hardware Acceleration Module
144-y
Hardware Acceleration Module
156
DRAM Controller
146
148
DRAM Module

FIG. 3

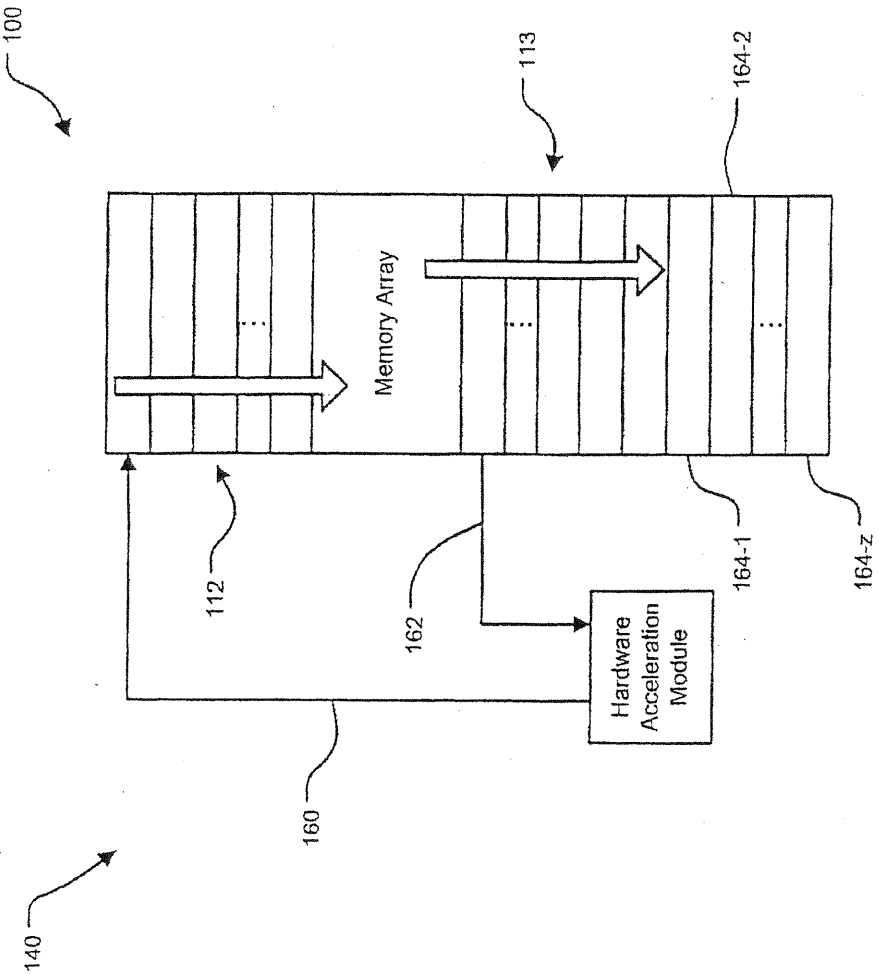

100
113
164-2
Memory Array
112
162
164-1
164-z
Hardware Acceleration Module
160
140

FIG. 4

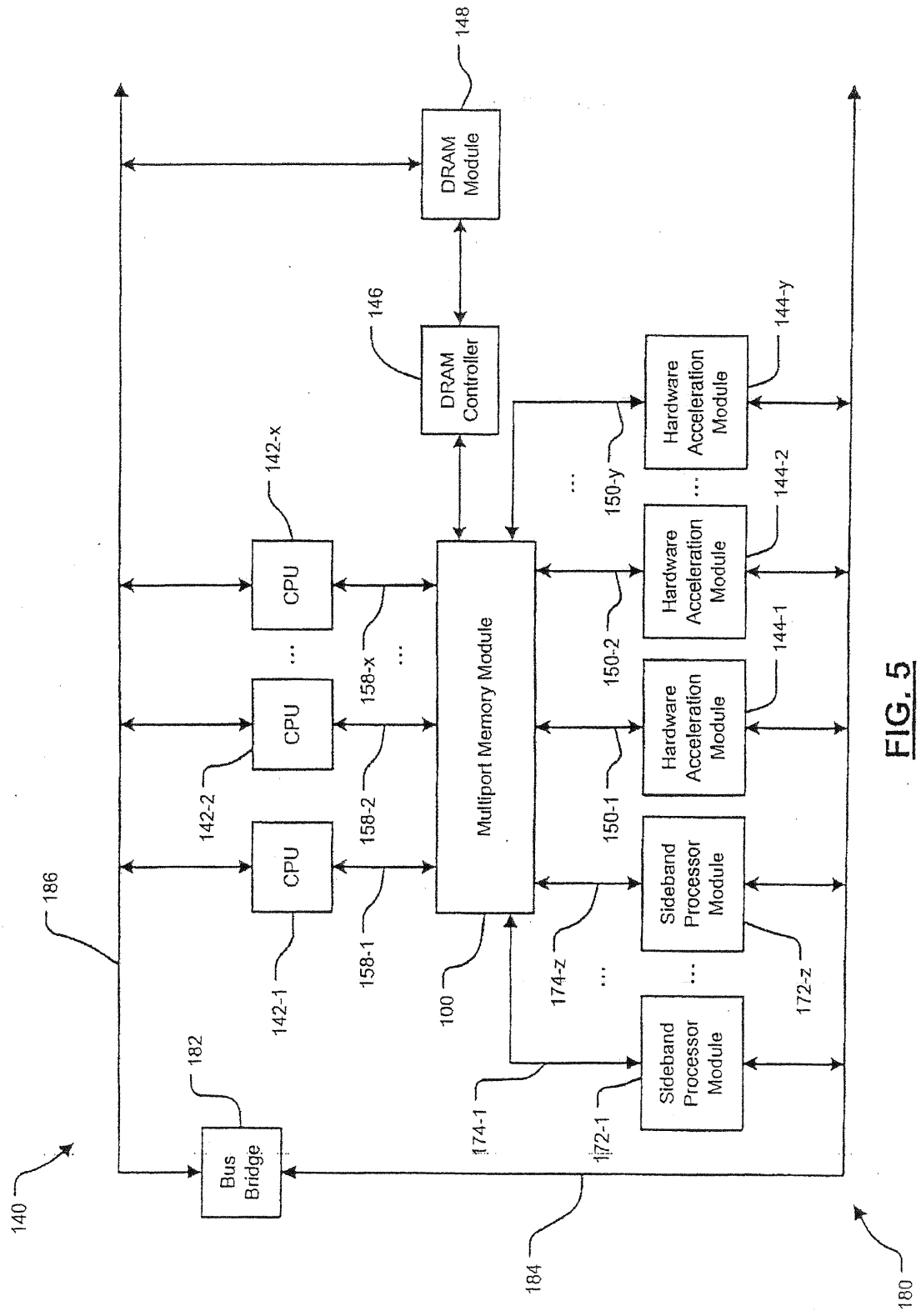

140
186
182
Bus Bridge
184
180
CPU
142-1
142-2
142-x
158-1
158-2
158-x
Multiport Memory Module
100
DRAM Controller
146
DRAM Module
148
Hardware Acceleration Module
144-1
144-2
144-y
150-1
150-2
150-y
Sideband Processor Module
172-1
172-z
174-1
174-z

FIG. 5

FIG. 6A

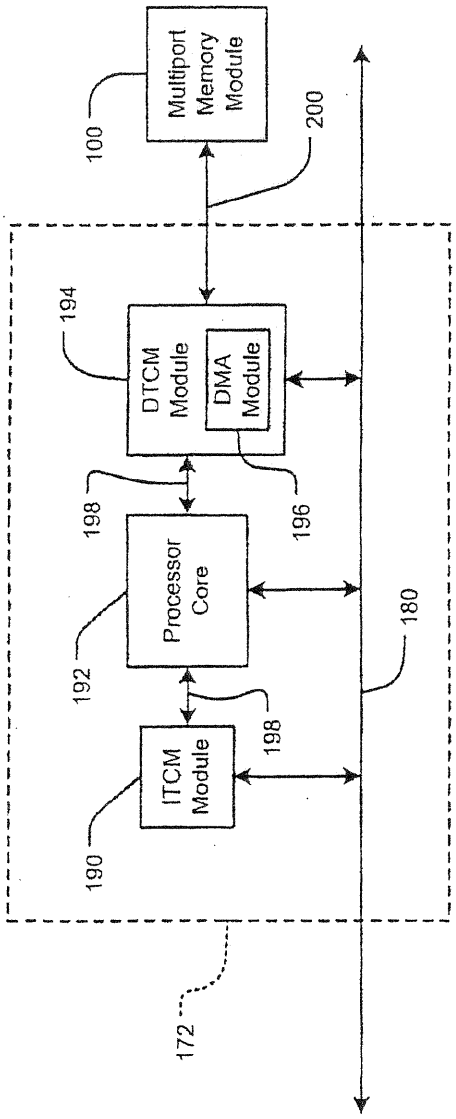
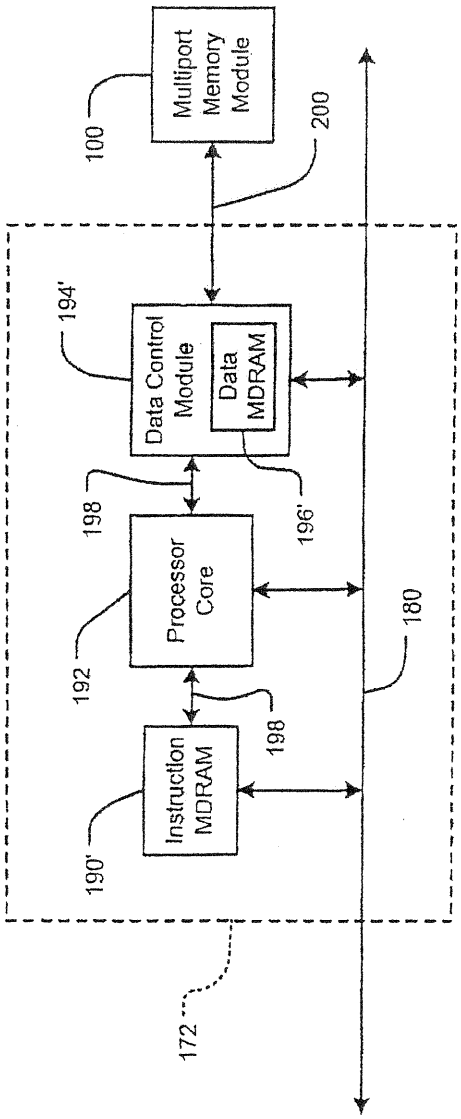

Multiport Memory Module
100
200
DTCM Module
DMA Module
194
196
198
Processor Core
192
ITCM Module
190
198
180
172

FIG. 6B


Multiport Memory Module
100
200
Data Control Module
Data MDRAM
194'
196'
198
Processor Core
192
Instruction MDRAM
190'
198
180
172

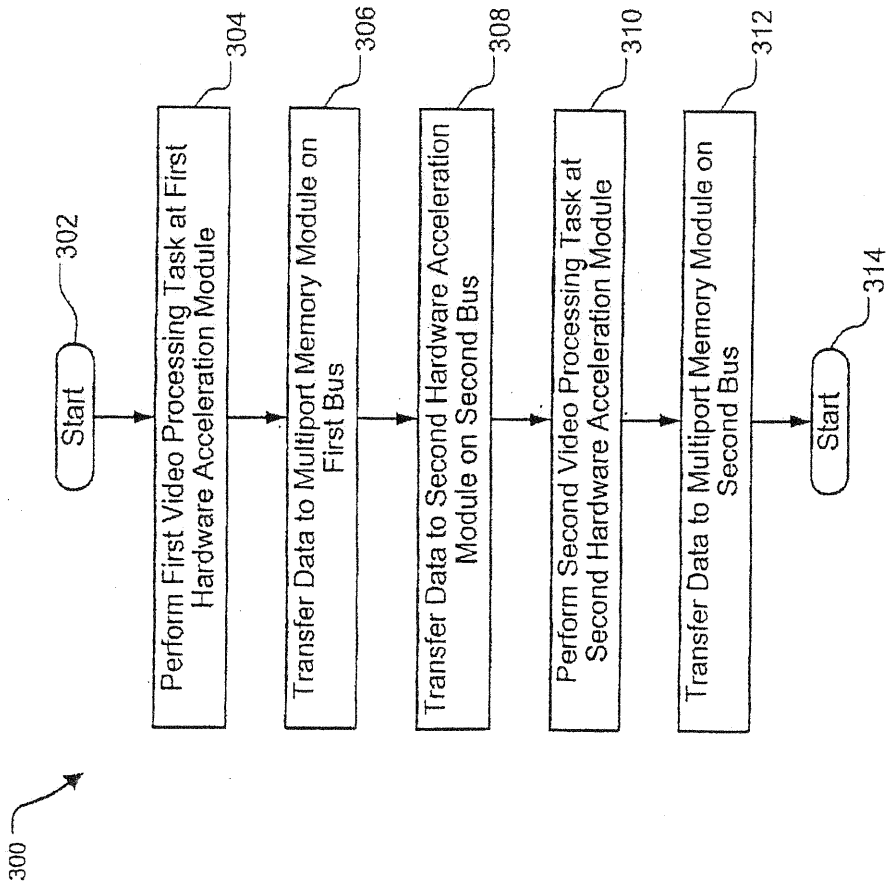

300
302
Start
304
Perform First Video Processing Task at First Hardware Acceleration Module
306
Transfer Data to Multiport Memory Module on First Bus
308
Transfer Data to Second Hardware Acceleration Module on Second Bus
310
Perform Second Video Processing Task at Second Hardware Acceleration Module
312
Transfer Data to Multiport Memory Module on Second Bus
314
Start

FIG. 7

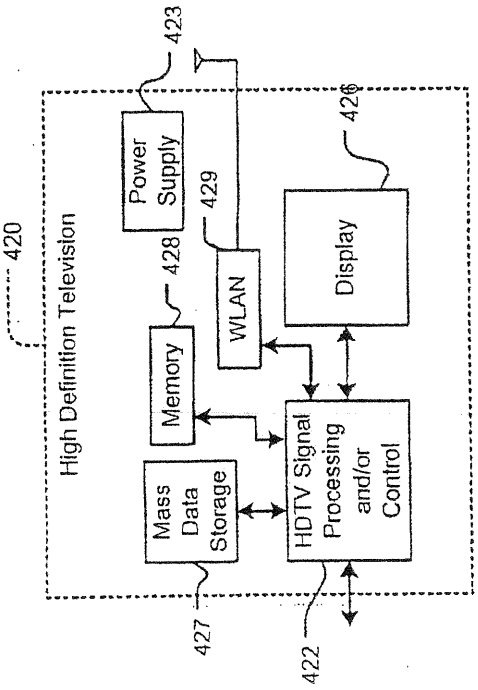

420
High Definition Television
Power Supply
423
429
428
Memory
WLAN
Display
426
Mass Data Storage
HDTV Signal Processing and/or Control
427
422

FIG. 8A

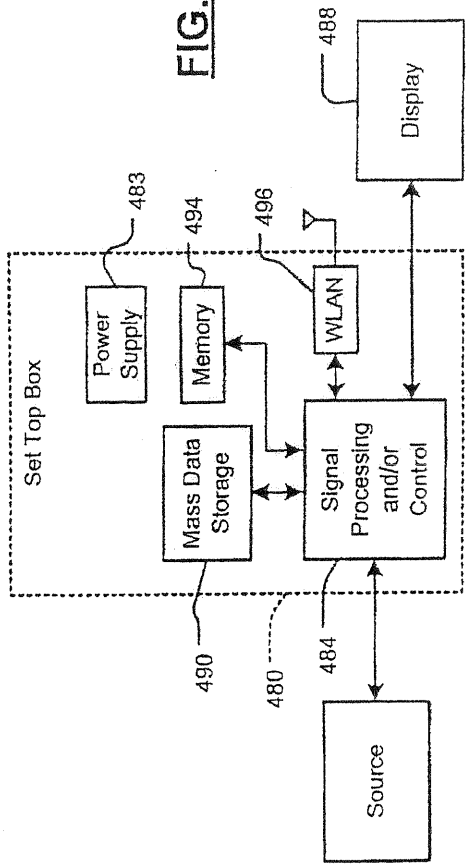

Set Top Box
Power Supply
483
Memory
494
WLAN
496
Mass Data Storage
Signal Processing and/or Control
Display
488
490
480
484
Source

FIG. 8B

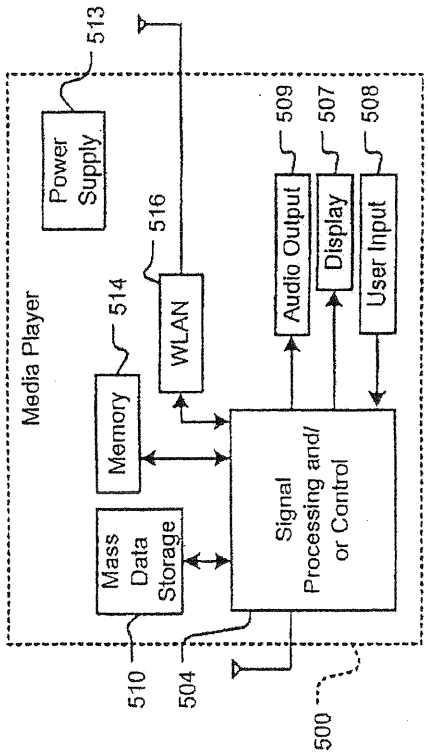

Media Player
513
Power Supply
516
WLAN
514
Memory
Mass Data Storage
Signal Processing and/or Control
509
Audio Output
507
Display
508
User Input
510
504
500

FIG. 8C