PITCH REDUCTION TECHNOLOGY USING ALTERNATING SPACER DEPOSITIONS DURING THE FORMATION OF A SEMICONDUCTOR DEVICE AND SYSTEMS INCLUDING SAME

Abstract

A method for patterning a layer increases the density of features formed over an initial patterning layer using a series of self-aligned spacers. A layer to be etched is provided, then an initial sacrificial patterning layer, for example formed using optical lithography, is formed over the layer to be etched. Depending on the embodiment, the patterning layer may be trimmed, then a series of spacer layers formed and etched. The number of spacer layers and their target dimensions depends on the desired increase in feature density. An in-process semiconductor device and electronic system is also described.

Figure 13