

ABSTRACT

An error correction circuit, including an error correction code (ECC) encoder configured to generate parity data corresponding to main data based on a parity generation matrix, and to output a codeword including the main data and the parity data to a plurality of memory devices; and an ECC decoder configured to: read the codeword from the plurality of memory devices, generate a syndrome corresponding to the codeword based on a parity check matrix, detect an error pattern based on the syndrome, generate a plurality of estimation syndromes corresponding to the error pattern using a plurality of partial sub-matrices included in the parity check matrix, and correct an error included in the read codeword based on a result of a comparison between the syndrome and the plurality of estimation syndromes.

FIG. 12