A DUAL SPACER PROCESS FOR NON-VOLATILE MEMORY DEVICES

BACKGROUND ART

This invention pertains to a spacer formation process for non-volatile memory devices. In particular, this invention is directed to a method for performing a two-step spacer deposition and etch resulting in the different appearance of a core and periphery of a non-volatile memory device. Additionally, this invention is related to a non-volatile memory device produced by the above method.

A semiconductor contains at least a core and periphery areas. Generally, memory information storage takes place in the core of a semiconductor. Additionally, storage of electronic charge also commonly occurs in the core. The core includes a plurality of core cells. The core cells are arranged in an ordered array known as a core cell array. Each core cell stores one or more bits of data for subsequent retrieval.

Commonly, adjacent the core is the periphery. One function of the periphery is to aid in correct circuitry selection for a certain memory location.

Charge is commonly stored in a separate polysilicon layer that is insulated both above and below the layer. Further, in an additional storage manner, charge is stored in a portion of the core generally known as the oxide-nitride-oxide (ONO) structure. Commonly, oxide functions as an insulator while nitride generally stores charge. The arrangement of the ONO structure facilitates the insulation of charge in the nitride layer by the nitride layer being sandwiched between two insulation oxide layers.

In one past method, the microchip formation process started with a silicon wafer substrate. On the silicon wafer, a bottom-most oxide layer is formed or deposited. This bottom-most oxide layer forms the bottom-most layer of the ONO structure of the core area.

The bottom and the top oxide layers of the ONO structure are formed generally in the same manner. In one manner, different gases, such as Silane, containing at least nitrogen dioxide, flow through a furnace. The silicon wafer and the oxygen from the nitrogen dioxide react to form an oxide layer. The oxide layer crystallizes on the wafer and/or the nitride layer.

The nitride layer, which is sandwiched between the two insulating oxide layers, is formed in a similar manner as the oxide layers. One way of nitride layer formation includes the use of different gases, such as Silane, containing at least silicon, hydrogen, and ammonia, flowing through a furnace. The silicon and the nitrogen from the ammonia react to form silicon nitride that crystallizes on the wafer.

While the core area typically has an ONO structure, the ONO structure is commonly etched away from the periphery area leaving only the bare silicon. A gate oxide is then commonly grown in a furnace on the bare silicon of the periphery area.

Once a gate oxide is grown on the bare periphery area, a doped polysilicon gate layer may be deposited on the gate oxide. The deposition of the polysilicon layer results in "seeds" of polysilicon formed on top of the gate oxide layer and the uppermost oxide layer of the ONO structure.

A prior method of spacer formation included blanket deposition of an oxide non-discriminately over the core and periphery of the wafer. Due to this blanket deposition, and particularly over the polysilicon line the spaces between and the area on top of the polysilicon line has a thinner deposition of oxide in comparison to the edges of the polysilicon lines. The edges of the polysilicon lines have a much thicker deposition of oxide. For

example, when a blanket deposition of an oxide is deposited over polysilicon lines, approximately 1000 Angstroms of oxide fills in the space between polysilicon lines while approximately 2000 Angstroms or more of oxide fills in about the edges of the polysilicon lines. When a spacer etch is performed of approximately 1000 Angstroms, the etch will remove about 1000 Angstroms from the space between the two polysilicon lines. The spacer created at the edges of the polysilicon lines will not be entirely removed and will remain at the edge of the polysilicon lines due to a topographical effect. The height of the spacer at the edge of the polysilicon lines is due to the height (to the first degree) of the polysilicon lines. Whereas, the width of the spacer, that is, the amount it extends from the polysilicon lines into the space between two polysilicon lines, will be about 2/3 the length of the original spacer deposition. In the example immediately above of a deposition of 1000 Angstroms of an oxide, a spacer of an oxide deposition of approximately a 600 to a 650 Angstrom width extending outward and into the space located between to polysilicon lines will be formed.

In some prior methods, vertical etching was performed to form a spacer between the polysilicon lines. The etch uniformly removed oxide between the polysilicon lines and above the polysilicon lines. Yet, due to a topographical effect, the vertical spacer etch still left a thicker oxide layer at the edge of the polysilicon lines. For example, if approximately 2000 Angstroms of oxide was deposited at the edge of a polysilicon line, the spacer vertical etch would remove only approximately 1000 Angstroms of oxide while leaving approximately 1000 Angstroms of oxide at the edge. Upon deposition and prior to etch, the deposition of the oxide in the area that will form the spacer at the edge of the polysilicon lines is substantially thicker than the deposition occurring between the polysilicon lines. Little if any oxide deposition may be left between the polysilicon lines, beyond that at the edge of the polysilicon lines, after the spacer etch is performed.

The oxide spacer acts as a mask for the polysilicon line prior to the implantation step. In non-volatile memory device manufacture, it is desirable to dope the area between the polysilicon lines. Doping the silicon between the polysilicon lines forms source and drain areas. Therefore, it is generally desirable to mask or "cover" certain areas of the wafer to prevent implantation at those areas. The oxide spacer blocks the implants from being too close to the polysilicon line. It does so by "spacing" the implants from the transistor area. The etch removes the mask so implantation may occur.

Using prior methods, the non-volatile memory device core may nearly completely fill with the oxide spacer. In prior methods, the manner in which the oxide is deposited results in the polysilicon lines appearing as if they had grown together. Then, when the spacer etch is performed, hardly any exposed silicon results in the area between polysilicon lines. The presence of the oxide covering the area between the two polysilicon lines makes implantation more difficult. Therefore, by some of the prior methods, implantation in the area between the polysilicon lines had to occur before core spacer formation.

DISCLOSURE OF INVENTION

The present invention relates to an improvement in semiconductor devices, and a method for making such semiconductor devices. The following description is presented to enable one of ordinary skill in the art to make and use the illustrative embodiment and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment will be readily apparent to those skilled in the art and the generic principles herein may be applied to other embodiments. Thus, the present invention is not

intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

In one aspect of the present invention, a first oxide layer is deposited over the polysilicon lines. The first oxide deposition covers tile area above the polysilicon lines as well as the area between polysilicon lines. This first oxide deposition does not fill up the space between the polysilicon lines. Following the first oxide deposition, the core and periphery areas may be etched removing a portion of the deposition. A spacer is formed adjacent the edge of the polysilicon lines. Subsequently, the area between polysilicon lines may be implanted or doped. The different structure of the core and periphery is provided by performing core specific implants, doping, or ONO/gate oxide removal in the gap between polysilicon lines defined by the first spacer. Next, a second oxide spacer may be deposited over the periphery and core. Unless either or both the periphery and core has been masked off with a resist, the second spacer is formed in both the periphery and the core. The second spacer width is defined by periphery circuit needs. Subsequent the second spacer deposition, a second spacer etch is performed over both the core and periphery but targeted to the particular needs of the periphery.

BRIEF DESCRIPTOIN OF DRAWINGS

FIG. 1 shows a side view of a prior art non-volatile memory device after poly-etching showing two polysilicon lines.

FIG. 2 shows a prior art side view of a non-volatile memory device after the first spacer deposition.

FIG. 3 shows a prior art non-volatile memory device after the first spacer etch.

FIG. 4 shows a side view of an oxide or nitride spacer between two polysilicon lines of an embodiment of the present invention.

FIG. 5 shows a side view of the core area after the second spacer etch one embodiment of the non-volatile memory device.

FIG. 6 shows a side view of the core area after the second spacer etch of an embodiment of the non-volatile memory device.

MODES FOR CARRYING OUT THE INVENTION

In FIG. 1 shows a prior art non-volatile memory device 1 after polysilicon etching. Two polysilicon lines 4 are deposited on the substrate 3. FIG. 2 shows a prior art non-volatile memory device 1 after a first oxide layer 12 is deposited over and in the area between 8 the two polysilicon lines 4. In FIG. 3, a prior art non-volatile memory device 1 is shown after performance of a first spacer etch showing the spacer 12′ (where prime in the figures represents a spacer formed from the oxide layer deposition). Implantation occurs in implantation area 8′. As shown in FIG. 4, in one aspect of the present invention, a first oxide layer 12 is deposited over the polysilicon lines 4. The oxide deposition covers the area above the polysilicon lines 4 as well as the area x between polysilicon lines 4. This first oxide deposition 12 does not completely fill up or level off the area x between the polysilicon lines 4. After the first oxide deposition 12, the area x between polysilicon lines 4 in both the core 24 and periphery 28 are etched. This forms the spacer 12′. Following spacer formation, a portion of the gate oxide may be removed. Subsequently, an implantation area 20 between the polysilicon lines 4 may be implanted or doped. Next, as shown in FIGS. 4 and 5, a second oxide spacer 13 may be deposited in the periphery 28 and core 24. Subsequent the second spacer 13 deposition, a second spacer etch is performed over the periphery 28 area and core 24. The doping of the periphery effects the appearance of the periphery 28. As shown in FIG. 6, this second

etch provides for a near absence of implant in the area between the polysilicon lines 4 in the periphery 28 of the non-volatile memory device 1.

This is in contrast to the core 24 of the non-volatile memory device 1 that, after the second spacer etch, still has dopants implanted into the silicon located between the spacers 12′ and under the spacer 13′.

The first oxide layer deposition 12 has an approximate thickness of less than one-half x (1/2x) where x represents the distance between the edges 16 of each polysilicon line 4. For example, if the distance between edges 16 of the two polysilicon lines 4 is approximately 1000 Angstroms, less than 500 Angstroms of a spacer deposition would be used to fill the gap between the two edge areas 16 of the polysilicon lines 4.

At some point after the oxide deposition 12, which is of a generally reduce thickness than commonly applied, a spacer etch forms a space between the polysilicon lines 4 by removing some of the oxide layer 12 which was deposited.

In the resulting space 20, implantation or removal of the ONO or gate oxide can occur. After implantation occurs, a second spacer deposition 13 is performed. The amount of the second spacer deposition 13 is dependent upon the overall spacer 12′ requirements. For example, if the deposition requirement overall of the spacer 12′ is approximately 1000 Angstroms, and in the first spacer deposition 12 less than 500 Angstroms was deposited, the second spacer deposition 13 is sufficient to produce a 1000 Angstrom deposition overall in the area between the two polysilicon lines 4.

FIG. 4 depicts the non-volatile memory device 1 after the second deposition 13 of the spacer oxide. FIG. 5 depicts one embodiment of the core 24 of the non-volatile memory device 1 after the second spacer etch. Implantation or doping occurs in the area formed after the first spacer etch located between the two polysilicon lines 20. FIG. 6 represents one embodiment of the periphery 28 of the non-volatile memory device 1 after the second spacer etch. As is apparent, the core area 24 after the second spacer etch is devoid or nearly devoid of oxide and has generally the appearance of FIG. 6. If the core 24 area is masked in the implantation area 20 of the silicon wafer or substrate, then oxide deposition may still be found between the first spacers 12′ and the core has generally the appearance of FIG. 5. Whereas, in contrast, the periphery 28 does not have oxide remaining in the area located between the first spacer 12′ as generally in FIG. 6. One embodiment of a nonvolatile memory device 1 made by the method of the present invention has a distinguishable core 24 and periphery 28 area.

In an alternative embodiment, the core 24 and the periphery 28 of the integrated circuit both have the appearance of the circuit as depicted in FIG. 6. In this embodiment, the implants located in the implantation area 20 in the core 24 and the periphery 28 differ. This difference in implant between the core 24 and the periphery 28 can be accomplished by masking the core 24 and/or periphery 28 during implantation.

In yet another embodiment, implantation of core 24 occurs after the performance of first spacer etch. Whereas, implantation occurs in the periphery 28 only after both the first and the second oxide deposition is preformed and the second spacer etch. In order not to etch the core 24 during the second spacer etch, the core 24 is covered with resist during the second spacer etch. In this manner, the core 24 receives neither the second deposition nor undergoes the second spacer etch. The resulting core 24 has the appearance depicted in FIG. 5. The periphery has the resulting appearance of FIG. 6.

In yet a further embodiment, implantation of periphery 28 occurs after the performance of first spacer etch. Whereas, implantation occurs in tile core 24 only after both the first and the second oxide deposition is preformed and the second spacer etch. In order not to etch the periphery 28 during the second spacer etch, the

periphery 28 is covered with resist during the second spacer etch. In this manner, the periphery 28 receives neither the second deposition nor undergoes the second spacer etch. The resulting core 24 has the appearance depleted in FIG. 6. The periphery 28 has the resulting appearance of FIG. 5.

The discussion above is descriptive, illustrated and exemplary and not to be taken as limiting the scope defined by the appended claims. Of course, it should be understood that a wide range of changes and modifications could be made to the embodiment described above. For example, the thickness of the spacer layers may vary. Thus, it is intended that the foregoing detailed description be regarded as illustrative rather than limiting and that it be understood that it is the following claims, including all equivalents, which are intended to define the scope of this invention.

CLAIMS:

1. A method for forming dual spacers, comprising:

forming a first oxide layer (12) over a core region (24) and a periphery region (28), the core and peripheral regions comprising one or more polysilicon lines (4);

etching the first oxide layer to form one or more first spacers (12') in the core region and in the peripheral region, thereby exposing an open space (20) between the one or more polysilicon lines and between the first spacers;

masking the peripheral region with a photoresist;

implanting the core region through the open space between the first spacers such that the peripheral region is not implanted;

forming a second oxide layer (13) over the core region and the peripheral region; and

etching the second oxide layer such that second oxide spacers (13') are formed adjacent to the first oxide spacers in the area between the polysilicon lines in at least the peripheral region.

2. The method of claim 1 wherein the first oxide layer has a thickness of less than one-half the distance between a periphery of the polysilicon lines.

3. A non volatile device made by the method of claim 1.

4. A non volatile memory device made by the method of claim 2.