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(54) Title: ROOM TEMPERATURE QUANTUM FIELD EFFECT TRANSISTOR COMPRISING A 2-DIMENSIONAL
QUANTUM WIRE ARRAY BASED ON IDEALLY CONDUCTING MOLECULES

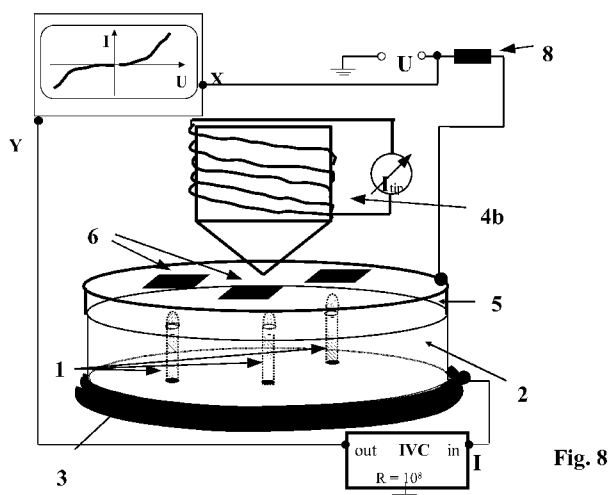


Fig. 8

(57) Abstract: One, several or very many parallel quantum wires, e.g. especially 1-dimensional quantum-conducting heavy ion tracks - "true" quantum wires at room temperature - see similarly EP1096569A1 [1] and [2], or also perhaps SWCNTs, vertically directed or also slightly tilted - up to about 45 degrees - arranged in a 2 dimensional plane, which as a 2-dimensional array interconnect the source and drain contacts of the here invented transistor, are modulated with respect to their quantum-mechanical conductivity via the strength of an applied electric or magnetic field [3], which is homogenous or variable in space locally across the 2 dimensional quantum wire array. The I-V curves of such quantum wires are measured via a double resonant tunnelling effect which allows identifying quantum effects at room temperature. A "true" quantum wire is characterized by quantized current steps and sharp current peaks in the I-V (I_{sd} versus U_{sd} , not just I_{sa} versus U_{gate}) curve. In the ideal case the quantum wires consist of straight polyacetylene-reminiscent molecules of the cumulene form ($\dots=C=C=C=C=C=\dots$) or of the form ($\dots-C\equiv C-C\equiv C-C\equiv C-\dots$) which are generated by the energy deposition during the single swift (heavy) ions' passage through the insulating DLC-layer. The switching time of the transistor is determined practically solely by the switching time of the magnetic field (time

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constant of the "magnetic gate"), the ohmic resistance of the source- drain connection via the quantum wire array is in the conducting state practically zero. The controlling "gate"-magnetic field having a component normal to the quantum wires can be generated by a small controlling current through some inductance (embodiment 1, Fig. 7, 8, 9, 10, 11) or also by a suitable (locally variable) direction of the magnetization in a ferromagnetic thin layer (e.g. Fe, Co, Ni, etc.) - embodiment 2, Fig. 8, 9, 10, 11 -, or also for example in a thin layer consisting of metallic (ferromagnetic) nanoparticles (e.g. Fe, Co, Ni, etc.) or also "current-less" through an electrostatically charged tip (embodiment 3a analogous to Fig. 7) or via a suitable polarization of a ferroelectric thin layer or liquid crystals /nanoparticles in an electric field - embodiment 3b, as in Fig. 8, 9, 10, 11. The quantum wire transistor can also be switched/controlled optically. Applications in the case of very large arrays ($>10^{10}/\text{cm}^2$ parallel QWs) would be a power transistor, in the case of very small arrays (single or a few parallel QWs) it would be non-volatile information storage, where due to the particular properties of 1-dimensional quantized conductivity a multi-level logic can be realized. In the case of optical switching/controlling of the quantum wire transistor, an extremely highly resolving 2-dimensional array of photodetectors is envisioned, where in that case the single QWs would have to be electrically connected one by one, e.g. reminiscent of the concept of a Nand- or Nor-Flash- Ram, whose size scale in turn is supposedly determining the limit of the achievable area density of the pixels. A feasible concept for a read-out matrix for possible applications of these quantum field effect transistors as a non-volatile memory chip or as a ultrahighly resolving light pixel detector array is reminiscent of the concept of a Nor-Flash-Ram. The concept is comprising a crossed comb structure of nanometric electrically conducting conventional leads on either side of the DLC-layer embedding the vertical quantum wires as shown in Fig. 23 each crossing on average being interconnected by one or a few ion track quantum wires. A feasible concept for a wiring matrix writing onto the quantum field effect transistors for a non-volatile memory chip is shown in Fig. 11 comprising a meander-shaped circuitry.