CLAIMS:

1. A method of forming a nanowire device comprising:

forming alternating layers of an epitaxial silicon material on epitaxial silicon germanium material on a substrate;

forming fin structures by etching the alternating layers and forming trenches adjacent to the fin structures;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate;

filling a gap in the spacers that is adjacent to the fin structures with a second spacer;

forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers;

removing one of the silicon and the epitaxial silicon germanium layers from the fin structures disposed between the spacers.

2. The method of claim 1 wherein the second spacer material comprises at least one of a spacer like material and a low-k material.

3. The method of claim 1 further comprising wherein the gap in the spacers is filled on a source/drain side of the spacer.

4. The method of claim 1 further comprising wherein the gap in the spacers is filled on a gate side of the spacer.

5. A method of forming a nanowire device comprising:

forming alternating layers of an epitaxial silicon material on epitaxial silicon germanium material on a (100) substrate comprising a <111> channel;

forming fin structures by etching the alternating layers and forming trenches adjacent to the fin structures;

forming spacers across and on the fin structures;

removing a portion of the fin structures from source/drain regions on the substrate, and then forming source/drain structures on the source/drain regions, wherein the source/drain regions are adjacent the spacers;

removing the epitaxial silicon layers from the fin structures disposed between the spacers by using a wet etch that is selective to silicon and not to silicon germanium.

6. The method of claim 5 wherein silicon germanium nanowires are partially etched after removing all of the silicon between the SiGe nanowires of the fin structure.

7. The method of claim 6 wherein the wet etch comprises an anisotropic etch to minimize lateral etching within the spacers.

8. A method of forming a nanowire device comprising:

patterning alternating layers of nitride and oxide disposed on a silicon substrate to expose a back region and a trench region;

forming one of a silicon material and a silicon germanium material in the trench and back regions;

forming a hard mask on one of the silicon germanium and silicon;

forming a fin structure by removing a portion of the alternating layers of nitride and oxide not covered by the hard mask; and

forming nanowire structures by oxidizing the fin structure and then removing the oxidized portions.

9. The method of claim 8 further comprising wherein the nanowire structures are disposed across substantially all of the device.

10. A method of forming a nanowire device comprising:

patterning alternating layers of nitride and oxide disposed on a silicon substrate to expose a back region and a trench region;

forming one of a silicon material and a silicon germanium material in the trench and back regions;

forming a hard mask on one of the silicon germanium and silicon;

forming a forming a fin structure by removing a portion of the alternating layers of nitride and oxide not covered by the hard mask;

forming a second hard mask around the fin structure;

forming a gate region adjacent the fin structure, wherein a portion of the fin structure may be exposed;

forming nanowire structures by oxidizing the fin structure and then removing the oxidized portions.

11. The method of claim 10 further comprising wherein the nanowire structures are disposed only in the gate area.

12. The method of claim 10 further comprising wherein the oxidized portions of the fin structure is removed by:

etching the oxide with a wet etch; and

etching one of the silicon and silicon germanium with an anisotropic etch.

13. A method of forming a semiconductor device, the method comprising:

forming an epitaxial silicon germanium (SiGe) layer on a bulk crystalline silicon substrate;

forming an epitaxial silicon layer on the epitaxial SiGe layer;

forming a fin structure from the epitaxial SiGe layer and the epitaxial silicon layer;

forming a sacrificial gate electrode over the fin structure, defining a pair of source/drain regions of the fin structure;

forming dielectric spacers adjacent to sidewalls of the sacrificial gate electrode and over the fin structure;

removing portions of both the epitaxial silicon layer and the epitaxial SiGe layer from the pair of source/drain regions;

forming epitaxial silicon source/drain regions for the fin structure, the epitaxial silicon source/drain regions adjacent to the dielectric spacers;

removing the sacrificial gate electrode from between the dielectric spacers to expose a portion of the fin structure between the dielectric spacers;

removing the epitaxial SiGe layer from the portion of the fin structure between the dielectric spacers to form an epitaxial silicon nanowire in the portion of the fin structure between the dielectric spacers;

forming a high-k gate dielectric layer on the epitaxial silicon nanowire; and

forming a metal gate electrode on the high-k gate dielectric layer, the metal gate electrode around the epitaxial silicon nanowire.