

Switched Capacitor Circuit

Introduction

5 This invention relates to switched capacitor circuits.

 A problem afflicting signal processing systems using switched capacitor circuits is the generation of offset voltage by charges supplied to, or drawn from, the various
10 capacitors when the switches are opened. The charges may have been associated with the switches in their closed state or may be transferred via parasitic capacitances by the switch control signals.

 A typical switched capacitor circuit has a chain of
15 charge transfer stages each consisting of a switch responsive to a control, or clock, signal, a capacitor and a buffer amplifier. Alternate switches in such a chain are made responsive respectively to first and second clock signals having overlapping periods in which all switches
20 are open. As each switch in the chain is opened some charge will be transferred to or from the following capacitor, causing the voltage thereon to change from that established while the switch was closed. These voltage changes, being normally in the same sense, will accumulate
25 along the chain. An input signal will thus be offset from its initial levels as it is passed along the chain.

 In many cases offsetting the signal leads to degradation of the system performance. One such case, for example, is that in which a long chain of charge transfer
30 stages are used to provide a series of progressively more delayed signals. Outputs from such a chain can be appropriately weighted and summed to obtain finite impulse response (FIR) filter characteristics. An accumulative voltage offset reduces the signal handling capacity of the
35 chain: ultimately to zero.

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Statement of the Invention

In accordance with the invention a switched capacitor circuit including at least one stage comprising:

an input node for receiving an input signal, an
10 output node for producing an output signal, a first
reference node for receiving a first reference voltage, a
capacitor having a first terminal coupled to the first
reference node and having a second terminal coupled to the
output node and coupled to the input node via first switch
15 means responsive to a control signal is characterized in
that said at least one stage further comprises:

a second reference node;

second switch means coupled between the first terminal of the capacitor and the first and second reference nodes and responsive to the control signal so as alternately to couple the first terminal of the capacitor to the first and second reference nodes; and

means for producing at the second reference node a voltage representative of the output signal from a stage of the circuit so as to compensate for offset voltages produced on the capacitor.

Brief Description of the Drawings

30 One TV video signal filter incorporating a switched capacitor circuit in accordance with the invention will now be described by way of reference to the accompanying drawings, in which:

Figures 1(a), (b) and (c) show part of the circuit
35 with switches in various positions; and

Figures 2 and 3 show alternative arrangements for producing a voltage for use in the part of the circuit shown in Figure 1.

Description of Specific
Embodiment of the Invention

Referring firstly to Figure 1, a TV video signal
5 filter includes a switched capacitor, sampled data circuit
2 having a chain of similar, serially-connected stages,
only three of which 4, 6, 8 are shown. Each stage 4, 6, 8
has a switch S1, S2, S3, a capacitor C1, C2, C3 and a
unity-gain buffer amplifier. In each stage, one terminal
10 of the switch S1, S2, S3 constitutes the input node of the
stage and the other terminal of the switch is connected to
one terminal B of the stage's capacitor C1, C2, C3 and to
the input of the stage's buffer amplifier; the buffer
amplifier output constitutes the output node of the stage.

15 The terminals A of the capacitors C1 and C3 are
connected to ground. However, as will be explained
hereafter, the terminal B of the capacitor C2 is connected
to a first terminal of a further switch S2A. Second and
third terminals of the switch S2A are connected
20 respectively to ground and to a controlled voltage V1.

The switches S1, S2, S2A and S3 are controlled by
overlapping clock signals of first and second phases so
that the switches of adjacent stages open and close
alternately (as illustrated in Figures 1(a) and (c)) and so
25 that during a clock overlap period all switches are open
(as illustrated in Figure 1(b)). Thus, during a first
phase of the clock signals the switch positions are as in
Figure 1(a) and a voltage V0 established on capacitor C1 is
transferred to capacitor C2.

30 During a 'clock overlap' period those switches
(e.g. S2) which were closed, open, while those (e.g. S1,
S3) open remain so : the switch positions are thus as in
Figure 1(b). Due to the charge drawn from capacitor C2
when switch S2 opens the voltage thereon is changed to
35 $V_0 - V$. It will be realised that the charge path through C2
is completed by stray capacitance, CS2.

In a conventional chain of switched capacitor stages (not shown) in which the terminal A of capacitor C2 is connected to ground, like the terminals A of capacitors C1 and C3, it would be the voltage $V_0 - \Delta V$ which would be established on capacitor C3 upon closure of switch S3. In the arrangement of Figure 1, however, during the second phase of the clock signals terminal A of capacitor C2 is connected to a voltage V_1 , the switch positions being as shown in Figure 1(c). The voltage established on capacitor C3 is thus $V_0 - \Delta V + V_1$.

It is evident that if V_1 is set to ΔV then the voltage established on C3 equals the voltage V_0 originally established on C1 : the offset voltage ΔV is then compensated. It is equally evident that the compensation may be applied to any number of capacitors, or that a few stages may be overcompensated and the rest uncompensated etc. according to the system constraints.

Referring now also to Figures 2 and 3, the voltage V_1 may be controlled by a feedback loop in which an output signal from the system is compared continuously, or periodically, with a reference level, the comparator output (after filtering and any other necessary processing) providing V_1 .

In Figure 2 there is shown a circuit for generating the voltage V_1 for use in the chain of Figure 1. It is a characteristic of TV video signals that they are periodically set to a 'black' reference level, and systems designed to process them are equipped to generate timing pulses coinciding with these periods.

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In the circuit of Figure 2 an output signal from the final switched capacitor stage of the filter shown in Figure 1 is applied to one input of a gated comparator circuit 20 arranged to be active, in response to a gating signal, at periods during which the output signal will be at a 'black' level. A second input of the comparator receives a reference level to which the 'black' level should be, desirably, adjusted. The comparator output feeds a storage capacitor C_s which via a buffer amplifier provides the controlled voltage V_1 . Assuming the phasing to be correct the feedback loop comprising the circuit of Figure 2 and the filter of Figure 1 will adjust the 'black' level of the filter output signal to close to the desired reference level. The stability of the loop may be assured, as is well understood, by controlling the gain/phase characteristic, specifically by controlling the gain or maximum output current of the comparator of Figure 2 and by choosing a large enough value for storage capacitor C_s .

In a long chain of delay stages it will be necessary to compensate a number of stages (e.g. every other stage) so that the offset voltages do not accumulate along the chain to too high a level before being compensated. In such cases the circuit of Figure 2 may be modified as shown in Figure 3 by the addition of clock-controlled switch 22 and a further buffer amplifier.

In Figure 3 the voltage appearing on the storage capacitor C_s is supplied via a first buffer amplifier to one input terminal of the changeover switch 22 operated by the filter clock signal. Another input terminal of the changeover switch 22 is connected to ground or to an appropriate reference voltage. The output terminal of the changeover switch 22 is connected via the further buffer amplifier to the signal ground side of all the filter storage capacitors (such as C_2) chosen to receive the compensation signal. The advantage of this structure is that a single changeover switch 22 is required rather than individual changeover switches such as S_{2a} being provided for each capacitor of the filter to which compensation is applied.

Claims

1. A switched capacitor circuit including at least one stage comprising:

5 an input node for receiving an input signal, an output node for producing an output signal, a first reference node for receiving a first reference voltage, a capacitor having a first terminal coupled to the first reference node and having a second terminal coupled to the
10 output node and coupled to the input node via first switch means responsive to a control signal,
characterized in that said at least one stage further comprises:

a second reference node;
15 second switch means coupled between the first terminal of the capacitor and the first and second reference nodes and responsive to the control signal so as alternately to couple the first terminal of the capacitor to the first and second reference nodes; and
20 means for producing at the second reference node a voltage representative of the output signal from a stage of the circuit so as to compensate for offset voltages produced on the capacitor.

25 2. A switched capacitor circuit according to claim 1 wherein the means for producing comprises:

a comparator having a first input coupled to receive the output signal from a stage of the circuit; a second input coupled to receive a second reference voltage and an
30 output coupled to the second reference node.

3. A switched capacitor circuit according to claim 2 wherein the means for producing further comprises a storage means coupled between the comparator output and the second
35 reference node.



4. A switched capacitor circuit according to any preceding claim including a plurality of serially connected stages each comprising:

an input node for receiving an input signal, an
5 output node for producing an output signal, a first reference node for receiving a first reference voltage, a capacitor having a first terminal coupled to the first reference node and having a second terminal coupled to the output node and coupled to the input node via first switch
10 means responsive to a control signal,

characterized in that the circuit further comprises:
a second reference node;

second switch means coupled between the first
terminals of the capacitors of at least two stages and the
15 first and second reference nodes and responsive to the control signal so as alternately to couple the first terminals of the capacitors of said at least two stages to the first and second reference nodes; and

means for producing at the second reference node a
20 voltage representative of the output signal from a stage of the circuit so as to compensate for offset voltages produced on the capacitors.

5. A switched capacitor circuit substantially as
25 hereinbefore described with reference to the accompanying drawings.

6. A TV video signal filter circuit comprising a
switched capacitor circuit according to any preceding
30 claim.

