

Description

Background of the Invention

The present invention relates to reactance circuits and, more particularly, to a circuit and method for producing a balanced, variable reactance across a pair of circuit terminals, the value of which is controllable.

There is a myriad of uses for a balance reactance circuit having a variable reactance that is controllable. One obvious use for such a circuit, to which the present invention is directed, is to provide a controllable reactance as a portion of an LC reactive tank circuit of an oscillator. By varying the reactance, the total reactance of the tank circuit can be varied to cause a change in the center operating frequency of the oscillator. The oscillator, in turn, may be utilized in the FM or video detector stages of a television receiver.

Contemporary technology is driving television receivers to be manufactured as single monolithic integrated circuitry. As such, the FM and video detector portion of the television receiver, to the extent possible, has to be integratable in order to produce a single monolithic chip circuit. The requirement also dictates that the detector oscillator of the video detection circuitry be as simple as possible; the less complex the circuitry the more room that is available on board the integrated chip for additional components of the television receiver. One method that has been proposed is the use of a LC oscillator operating at a center frequency that can be tuned within a predetermined range. The oscillator is tuned by electronically varying the reactance of the LC tank circuit of the oscillator. In particular, by varying the capacitance value of the LC tank, the oscillator's center frequency is changed. Therefore, a requirement for an integrated variable reactance circuit is established.

A prior art single ended variable capacitance circuit, U.S. Patent No. 4,109,214, produces a single-ended variable capacitance at an output terminal thereof. However, because of the balanced nature of the oscillator that is required for performance in television receivers, the single-ended capacitive circuit of the prior art is not useful. Additionally, the prior art circuit requires that signal components be dissipated to ground which is undesirable in quality television receivers due to the fact that such grounded signals could be picked up and reproduced within the receiver to cause distortion of the received television signal.

Therefore, a need exists for a balanced variable reactance circuit the value of reactance being made electronically variable.

SUMMARY OF THE INVENTION

In accordance with the invention there is provided a monolithic integrated, balanced variable reactance circuit for providing a controllable reactance between first and second terminals, comprising:

a first current steering circuit having first, second and third terminals, said first current steering circuit being responsive to an applied control signal for steering first and second proportional currents between said first and said third terminals and respectively between said second and said third terminals, said first and second terminals of said first current steering circuit being coupled to the first and second terminals of the balanced reactance circuit respectively;

a second current steering circuit having first, second and third terminals, said second current steering circuit being responsive to said applied control signal for steering first and second proportional currents between said first and said third terminals and respectively between said second and said third terminals, said first terminal being coupled to said first terminal of said first current steering circuit and said second terminal being coupled to said second terminal of said first current steering circuit, said latter first and second proportional currents being in antiphase relation with respect to said first and second proportional currents of said first current steering circuit;

first reactive means coupled between said third terminal and said second terminal of said second current steering circuit.

second reactive means coupled between said third terminal and said second terminal of said second current steering circuit.

According to Claim 8 there is also provided a method for producing a variable and controllable reactance across a pair of terminals.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic drawing illustrating a prior art, variable capacitive circuit;

FIG. 2 is a vector diagram useful for understanding the operation of FIG. 1;

FIG. 3 is a schematic diagram illustrating a balanced variable reactance circuit in accordance with the present invention;

FIG. 4 is a schematic diagram of a variable reactance circuit of another embodiment of the present invention;

FIG. 5 is a schematic diagram of still another embodiment of the present invention;

FIG. 6 is a schematic diagram of the preferred embodiment of the present invention; and

FIG. 7 is a vector diagram useful for understanding the operation of the circuit of FIG. 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to FIGS 1 and 2 the description of prior art variable capacitive circuit 10 is described. The operation of variable capacitive circuit 10 is useful for understanding the operation of the balanced, variable reactance circuits of the embodiments of the present invention. Capacitive circuit 10 comprises a pair of NPN transistors 12 and 14 the emitters of which are commonly connected in a differential manner at common circuit node 16. A current source 18 is coupled between node 16 and a power supply conductor at which is supplied ground reference potential 20. The base electrodes of transistors 12 and 14 are coupled respectively to a pair of terminals 22 and 24 across which a direct current (DC) control voltage, V_{CONT} is supplied for differentially controlling the conduction of the two transistors in order to steer proportional currents therebetween. The collectors of transistors 12 and 14 are coupled to first and second terminals 28 and 30 (with the collector of transistor 12 being at alternating current, AC, ground) to a source of operating potential accordingly. A capacitor having a capacitive value, C , is connected between the collector and emitter of transistor 14, between nodes 32 and 16. It is understood that circuit 10, including capacitor 26, can be manufactured in monolithic integrated circuit form.

In operation, variable capacitive circuit 10 functions as a current steering circuit whereby the effective capacitance value produced at node 32 is varied as the conductivity of transistor 14 is controlled by varying V_{CONT} . In response to an alternating voltage, V_i , applied at terminal 30, a reactive current, i_i , flows into and out of node 32 to produce current flow through capacitor 26 equal to i_c . As shown in the vector diagram of FIG. 2, i_c splits at common node 16 and is sourced through transistors 12 and 14 accordingly. With transistor 14 conducting, the current i_s (vector 38) that is fed back through transistor 14 appears at the collector thereof, at node 32, in antiphase to the collector current, i_c . Hence, the total current, i_i , can be shown to be equal to:

$$i_i = (i_c - i_s)$$

Therefore, with transistor 12 rendered fully conductive and transistor 14 fully nonconductive, all of the current i_c flows into common node 16 which is at alternating ground reference. Because transistor 14 is turned off, the current i_s equals zero and therefore the current i_i is equal to the current i_c (see the

above equation). Thus, the effective capacitance looking into node 32 is equal to the value of capacitor 26, or in other words;

$$C_{\text{eff}} = C,$$

where C is the capacitance value of capacitor 26.

At the balanced operating condition of circuit 10, where transistors 12 and 14 are equally conducting, the current i_c is equally split or steered therebetween. In this condition, i_s is equal to one half i_c . Since the current i_s is antiphase to the current i_c , it becomes equal to one-half the value i_c . This produces an effective capacitance at terminal 30 of;

$$C_{\text{eff}} = C/2$$

The value of capacitance 32 therefore appears to have been reduced by one-half its original value. Similarly, as the DC control voltage V_{CONT} is varied to fully turn on transistor 14 (while transistor 12 is turned off) the effective capacitance at node 32 becomes zero since the current i_s becomes equal to but opposite in phase to the current i_c .

Turning now to the remaining FIGS. the operation of the particular embodiments of the present invention will be described with reference to the operation of the variable capacitance circuit of FIG. 1. Referring first to FIG. 3, there is illustrated balanced variable reactance circuit 40 of one embodiment of the invention. Variable reactance circuit 40 includes a pair of current steering circuits 42 and 44 each of which individually operates in a similar manner described above for single ended variable reactance circuit 10 but which produce a balanced, variable reactance across first and second terminals thereof. Current steering circuits 42 and 44 each have a pair of outputs coupled to nodes 46 and 48, and via resistors 50 and 52, to power supply conductor 54 at which is received an operating potential, V_{CC} . Nodes 46 and 48 are connected to first and second terminals 56 and 58 across which the aforementioned balanced variable reactance is produced by variable reactance circuit 40 as will be hereinafter discussed. Terminals 56 and 58 may be coupled to an oscillator circuit (not shown) that is coupled at external terminals 60 and 62 to tuned LC tank circuit 65 as previously discussed. The tank circuit sets the center operating frequency of the oscillator; the oscillator and variable reactance circuit 40 being suited to be manufactured in monolithic integrated circuit form.

First current steering circuit 42 comprises NPN transistors 64 and 66 which are responsive to the control voltage V_{CONT} applied across the bases of the two pair of transistors for steering the capaci-

tive current sourced to common node 68 from capacitor 72 therethrough to nodes 46 and 48 accordingly. Common circuit node 68 is coupled to current source 70 the latter being returned to direct current (DC) reference potential 20. The currents steered through the individual transistors 64 and 66 are proportional to each other and appear at nodes 46 and 48 as two inphase current signals. Hence, in response to an alternating current (AC) driving voltage applied at terminal 60, a pair of proportional, inphase current signals are produced at nodes 46 and 48 the relative magnitudes of which are dependent on the relative conductivity of the two transistors 64 and 66. The portion of the capacitor current that is steered through transistor 64 to node 46 will be of opposite phase to the capacitive current flowing through capacitor 72 and tend, therefore, to cancel the latter at node 46.

Similarly, second current steering circuit 44 comprises a pair of NPN transistors 74 and 76 the emitters of which are connected at common circuit node 78 and, via current source 80, to DC reference potential 20. It is understood that during operation, common circuit nodes 68 and 78 are at AC ground. A driving voltage is applied at node 48 from terminal 62, which is of antiphase relation to the driving voltage applied at node 60, produces a capacitive current through capacitor 82 to node 78, that is steered between transistors 74 and 76 thereby establishing proportional and inphase current signals at the respective collectors thereof which are coupled to nodes 46 and 48. Again, the relative magnitudes of the two currents flowing through the collectors of transistors 74 and 76 vary as the relative conductivity thereof is varied by V_{CONT} . As understood, since the base of transistor 74 is coupled to the base of transistor 66 it operates in phase therewith and in antiphase with respect to transistor 64 such that the currents steered through transistors 74 and 76, which are sourced to nodes 46 and 48 respectively, are antiphased to the currents steered through transistors 64 and 66 and therefore tend to cancel each other.

In operation then, with a pair of equal but oppositely phased driving voltage signals applied at terminals 60 and 62, across tank circuit 65, a pair of antiphased capacitive currents are produced through capacitors 72 and 82 accordingly. These capacitive currents are summed with the current steered through the current steering circuits 42 and 44, at nodes 46 and 48, to produce an effective capacitance thereacross having a value that is electronically varied by varying the control voltage V_{CONT} . For example, at a balanced operating condition, where transistors 64 and 66 and 74, 76 are all conducting equally, the currents steered through transistors 64 and 74 cancel each other as do the currents steered through transistors 66 and 76.

Thus, only the direct capacitive currents flow through capacitors 72 and 74. This produces an effective capacitance across terminals 60 and 62 equal to the value, $C/2$; where C is the value of capacitors 72 and 82. It can be shown that the value of this effective capacitance which appears across tank circuit 65 varies from a value equal to zero to a maximum value of C as the control voltage, V_{CONT} , is varied over its full control range and transistors 64 and 76 go from a full conductive state to a nonconducting state. Hence, by varying the DC control voltage on the bases of these transistors, the effective capacitance of tank circuit 65 is varied which, in turn, would vary the center operating frequency of the LC oscillator coupled across terminals 56 and 58 as is understood.

Referring now to FIG. 4 there is illustrated variable reactance circuit 90 which operates as described above with reference to variable reactance circuit 40 but which in addition eliminates the direct capacitive currents from flowing through tank circuit 65 during the balanced operating state of the two current steering circuits 42 and 44. It is to be understood in the following description that components of the variable reactance circuit 90 which correspond to like components of variable reactance circuit 40 will be designated by the same referenced numbers.

In normal operation, the variable reactance circuits of the present invention described hereinafter are intended to be operated in balanced operating state whereby a predetermined value of capacitance is established across the first and second terminals 56 and 58. Therefore, it is desirable in some cases to eliminate the effect of the integrated capacitors of the variable reactance circuits from appearing directly across the tank circuit in order to prevent undesirable affects, such as any temperature coefficient associated with integrated capacitors 72 and 82 on the normal operating frequency. For example, if for some reason capacitors 72 and 74 have undesirable temperature coefficients associated therewith due to their being fabricated in monolithic circuit form, the center frequency and perhaps the Q of the tank circuit may be adversely affected. By eliminating the direct capacitive current at the center operating frequency from flowing through tank circuit 65, the effective capacitance across the tank at balance is zero. Thus, the normal operating frequency and Q of the tank circuit will be unaffected by the capacitors.

As illustrated in FIG. 4, differential amplifier 92 includes a pair of differentially connected NPN transistors 94 and 96 that are coupled to current source 98. The first and second inputs (bases of transistors 94 and 96) of amplifier 92 are coupled respectively to the common nodes 68 and 78 of the current steering circuits 42 and 44. The outputs

(collectors of transistors 94 and 96) of amplifier 92 are connected respectively to nodes 48 and 46. As shown, the value of current sourced through current source 98 is twice that of the current sourced through either current source 70 or 80.

At the balanced operating state, the bases of transistors 94 and 96 are modulated by the AC signals appearing across capacitors 72 and 82 to produce collector currents through the two transistors which are equal in amplitude but opposite in phase to the capacitive currents summed therewith. Hence, for example, the current flowing through capacitor 72, through transistor 66 to node 48, is cancelled by the collector current of transistor 94 and therefore does not appear across tank circuit 65 at terminal 62. In operation the value of reactance of variable reactance circuit 90 varies from a negative reactance value equal to $C/2$ to a positive reactance value equal to $C/2$ as the voltage V_{CONT} is varied over a predetermined range. The effective reactance value at the midrange value of V_{CONT} , i.e., the balance operating state of transistor 64, 66, 74 and 76 is, as aforementioned, equal to zero.

Variable reactance circuit 100 of FIG. 5 eliminates the effect of the dynamic emitter resistances, re, of each transistor of the current steering circuit 42 and 44 on the circuit performance. For example, at balance, the direct capacitive current flowing through capacitor 72 (FIG. 3) also flows through the emitter-collector path of transistor 66 to node 48. The value of the dynamic emitter resistance of transistor 66 will therefore cause the resultant reactive current to lag the ideal capacitive current by some factor. This action can effect the operating frequency of the tank circuit 65 as well as the Q thereof. The addition of transistors 102 and 104, having their collector-emitter paths coupled between common node 68 and 78 respectively and current sources 70 and 80, cancel the dynamic resistance effects of the transistors of the two current steering circuits. As illustrated, the bases of transistors 102 and 104 are cross connected to the common nodes 78 and 68 respectively. Capacitor 72 is connected between node 46 and the emitter of transistor 102. Likewise, capacitor 82 is connected between node 48 and the emitter of transistor 104. In this manner, the capacitors remain coupled between the common nodes and respective terminals of the variable reactance circuit 100. Transistors 102 and 104 establish virtual grounds at nodes 106 and 108 whereby the dynamic emitter resistances of the transistors cancel each other. Thus, the undesired effect of the transistors dynamic emitter resistances is eliminated. It is understood that the embodiments shown in FIGS. 4 and 5 can be combined into a single variable reactance circuit embodying the two concepts described separately.

Referring now to FIG. 6 and 7 there is shown variable reactance circuit 110 of the preferred embodiment of the invention which combines the features of variable reactance circuit circuits 90 and 100. Thus, at the center operating frequency no direct capacitive current flows through tank circuit 65 from terminals 60 and 62 thereby eliminating the temperature coefficient affects of the integrated capacitors 72 and 82. Additionally, the dynamic emitter resistances of transistors 64, 66, 74, 76, 112 and 114 are compensated for as well as any series resistance associated with capacitors 72 and 82 in order to prevent loading on tuned tank circuit 65 as will be hereinafter described.

As illustrated, a pair of emitter follower transistors 112 and 114 have their respective base-emitter paths connected between nodes 46 and 48 to one side of capacitor 72 and 78. The other side of capacitor 72 and 82 are returned at common nodes 68 and 78 as described above. The collectors of transistors 112 and 114 are coupled to positive power supply conductor 116 to a source of operating potential V_{CC} whereby capacitors 72 and 82 are isolated from but electronically coupled across tank circuit 65 at terminal 60 and 62. The conduction paths for transistors 112 and 114 are via respective resistors 118 and 120 to a second power supply conductor at which is supplied ground reference 20. Resistors 122 and 124 may correspond to current sources 70 and 80 previously described.

Again, a pair of antiphased AC voltage drive signals V and V' (FIG. 7) are applied at nodes 46 and 48, across tank circuit 65, to produce two antiphased capacitive currents through capacitors 72 and 82 respectively, which currents are sourced from the respective collector-emitter paths of transistor 112 and 114. Transistors 112 and 114 thus have the effect of removing the direct capacitive currents from flowing through tank circuit 65 during the balance operating condition of the circuit. As illustrated in FIG. 7, the AC driving voltage, V (vector 126), that is applied at terminal 60 will ideally produce a capacitive current i_c (vector 128) through transistor 112 that leads the voltage V by 90 degrees. However, among other things, the dynamic emitter resistance of the transistors will cause the actual capacitive current, i_c' (vector 130) to lag i_c by some angle depending on the value of i_r' , the resistive component of i_c' . It is understood that driving voltage V' (vector 136), will produce a similar antiphase capacitive current through capacitor 82.

In order to prevent loading of tuned tank circuit 65 due to the resistive component i_r' flowing through capacitor 72 and its counterpart that is associated with capacitor 82, resistors 138 and 140 are connected respectively between common circuits node 68 and 78 and junctions 58 and 56.

Thus, for example, the current flowing through transistor 114 produces direct capacitive current through capacitor 82 and a current through resistor 138. The current through resistor 138 will be in opposite phase to the resistive component of current flowing through capacitor 72 and therefore when this current is summed therewith, at node 68, the effect of these two resistive currents are cancelled. The resultant current becomes capacitive (vector 128) and equal to i_c . Similarly, the current flowing through resistor 140 is of opposite phase to the resistive component of current flowing through capacitor 82 and will therefore cancel each other at node 78 to produce a resultant capacitive current. Thus, at the center operating frequency of tank 65, with current steering circuits 42 and 44 being operated in a balanced operating state, variable reactance circuit 110 has no effect on the tune circuit 65. However, as V_{CONT} is varied above and below the value that establishes the balance operating condition, an effective capacitance is produced across the tank circuit which causes the center operating frequency thereof to vary in the same manner as discussed with reference to variable reactance circuit 90.

Hence, what has been described above are novel balanced variable reactance circuits suitable for being manufactured in monolithic integrated circuit form for providing a variable and controllable capacitance across a pair of terminals. In the preferred embodiment, the variable reactance value is substantially made equal to zero at the balanced operating condition of the circuit and therefore has no effect upon any load coupled thereto, such as a tuned LC tank circuit. Thus, the variable reactance circuit will not degrade performance of the tank circuit at the center operating frequency thereof.

Claims

1. A monolithic integrated, balanced variable reactance circuit for providing a controllable reactance between first (56) and second (58) terminals, comprising:

a first current steering circuit (42) having first (46), second (48) and third (68) terminals, said first current steering circuit being responsive to an applied control signal for steering first and second proportional currents between said first and said third terminals and respectively between said second and said third terminals, said first (46) and second (48) terminals of said first current steering circuit being coupled to the first (56) and second (58) terminals of the balanced reactance circuit respectively;

a second current steering circuit (44) having first (46), second (48) and third (78) terminals,

said second current steering circuit being responsive to said applied control signal for steering first and second proportional currents between said first (46) and said third (48) terminals and respectively between said second and said third terminals (78), said first terminal being coupled to said first terminal of said first current steering circuit and said second terminal being coupled to said second terminal of said first current steering circuit, said latter first and second proportional currents being in antiphase relation with respect to said first and second proportional currents of said first current steering circuit;

first reactive means (72) coupled between said third terminal (68) and said first terminal (46) of said first current steering circuit (42).

second reactive means (82) coupled between said third terminal (78) and said second terminal (48) of said second current steering circuit (42).

2. The circuit of claim 1 wherein said first and second reactive means are first and second capacitive means.

3. The circuit of claim 2 including:

first (116) and second power (20) supply conductors;

a first transistor (112) having a base coupled to said first terminal (46) of said first current steering circuit (42), a collector coupled to said first power supply conductor, and an emitter coupled to said first capacitive means (72) whereby said first capacitive means is indirectly coupled to the first terminal of the balanced reactance circuit;

a second transistor (114) having a base coupled to said second terminal (48) of said first current steering circuit, a collector coupled to said first power supply conductor (116), and an emitter coupled to said second capacitive means (82) whereby said second capacitive means is indirectly coupled to the second terminal of the balanced reactance circuit; and

said third terminals (68, 78) of said first and second current steering circuits being coupled to said second power supply conductor.

4. The circuit of claim 3 further including:

first resistive means (138) coupled between said third terminal (68) of said first current steering circuit and said emitter of said second transistor (114); and

second resistive means (140) coupled be-



Thus, for example, the current flowing through transistor 114 produces direct capacitive current through capacitor 82 and a current through resistor 138. The current through resistor 138 will be in opposite phase to the resistive component of current flowing through capacitor 72 and therefore when this current is summed therewith, at node 68, the effect of these two resistive currents are cancelled. The resultant current becomes capacitive (vector 128) and equal to i_c . Similarly, the current flowing through resistor 140 is of opposite phase to the resistive component of current flowing through capacitor 82 and will therefore cancel each other at node 78 to produce a resultant capacitive current. Thus, at the center operating frequency of tank 65, with current steering circuits 42 and 44 being operated in a balanced operating state, variable reactance circuit 110 has no effect on the tune circuit 65. However, as V_{CONT} is varied above and below the value that establishes the balance operating condition, an effective capacitance is produced across the tank circuit which causes the center operating frequency thereof to vary in the same manner as discussed with reference to variable reactance circuit 90.

Hence, what has been described above are novel balanced variable reactance circuits suitable for being manufactured in monolithic integrated circuit form for providing a variable and controllable capacitance across a pair of terminals. In the preferred embodiment, the variable reactance value is substantially made equal to zero at the balanced operating condition of the circuit and therefore has no effect upon any load coupled thereto, such as a tuned LC tank circuit. Thus, the variable reactance circuit will not degrade performance of the tank circuit at the center operating frequency thereof.

Claims

1. A monolithic integrated, balanced variable reactance circuit for providing a controllable reactance between first (56) and second (58) terminals, comprising:

a first current steering circuit (42) having first (46), second (48) and third (68) terminals, said first current steering circuit being responsive to an applied control signal for steering first and second proportional currents between said first and said third terminals and respectively between said second and said third terminals, said first (46) and second (48) terminals of said first current steering circuit being coupled to the first (56) and second (58) terminals of the balanced reactance circuit respectively;

a second current steering circuit (44) having first (46), second (48) and third (78) terminals,

said second current steering circuit being responsive to said applied control signal for steering first and second proportional currents between said first (46) and said third (48) terminals and respectively between said second and said third terminals (78), said first terminal being coupled to said first terminal of said first current steering circuit and said second terminal being coupled to said second terminal of said first current steering circuit, said latter first and second proportional currents being in antiphase relation with respect to said first and second proportional currents of said first current steering circuit;

first reactive means (72) coupled between said third terminal (68) and said first terminal (46) of said first current steering circuit (42).

second reactive means (82) coupled between said third terminal (78) and said second terminal (48) of said second current steering circuit (42).

2. The circuit of claim 1 wherein said first and second reactive means are first and second capacitive means.

3. The circuit of claim 2 including:

first (116) and second power (20) supply conductors;

a first transistor (112) having a base coupled to said first terminal (46) of said first current steering circuit (42), a collector coupled to said first power supply conductor, and an emitter coupled to said first capacitive means (72) whereby said first capacitive means is indirectly coupled to the first terminal of the balanced reactance circuit;

a second transistor (114) having a base coupled to said second terminal (48) of said first current steering circuit, a collector coupled to said first power supply conductor (116), and an emitter coupled to said second capacitive means (82) whereby said second capacitive means is indirectly coupled to the second terminal of the balanced reactance circuit; and

said third terminals (68, 78) of said first and second current steering circuits being coupled to said second power supply conductor.

4. The circuit of claim 3 further including:

first resistive means (138) coupled between said third terminal (68) of said first current steering circuit and said emitter of said second transistor (114); and

second resistive means (140) coupled be-

tween said third terminal (78) of said second current steering circuit and said emitter of said first transistor (112).

5. The circuit of claim 4 including:

third resistive means (118) coupled between said emitter of said first transistor (112) and said second power supply conductor (20); and

fourth resistive means (120) coupled between said emitter of said second transistor (114) and said second power supply conductor (20).

6. The circuit of claim 4 wherein said first current steering circuit includes:

third (64) and fourth (66) transistors each having a base, collector and an emitter, said emitters being connected to said third terminal (68), said bases receiving said applied control signal thereacross, said collector of said third transistor being connected to said first terminal (46) and said collector of said fourth transistor being connected to said second terminal (48); and

current source means (70 or 122) coupled between said third terminal and said second power supply conductor.

7. The circuit of claim 6 wherein said second current steering circuit includes:

fifth (74) and sixth (76) transistors each having a base, collector and an emitter said emitters being connected to said third terminal (78), said collector of fifth transistor being connected to said first terminal (46), said collector of said sixth transistor being coupled to said second terminal (48), said base of said fifth transistor being coupled to said base of said fourth transistor and said base of said sixth transistor being coupled to said base of said third transistor; and

current source means (80 or 124) coupled between said third terminal and said second power supply conductor.

8. A method for producing a variable and controllable reactance across a pair of terminals, comprising the steps of:

producing first and second antiphased reactive currents through first (72) and second (82) capacitors;

producing first and second proportional currents from said first reactive current;

producing third and fourth proportional currents from said second reactive current;

summing said first reactive current, said first and third currents at a first one of said pair

of terminals, said first and third currents being antiphased with respect to each other with said first current being in antiphase relation with said first reactive current; and

summing said second reactive current, said second and fourth currents at the second one of the pair of terminals.

9. The method of claim 8 further including varying the proportionality of said first and second currents with respect to each other while simultaneously varying the proportionality of said third current with respect to said fourth current.

Revendications

1. Circuit à réactance variable et intégré de façon monolithique pour fournir une réactance contrôlable entre des première (56) et seconde (58) bornes comprenant :

- un premier circuit (42) de pilotage en courant ayant des première (46), seconde (48) et troisième (68) bornes, ledit premier circuit de pilotage en courant étant sensible à un signal de contrôle appliqué pour piloter des premier et second courants proportionnels entre lesdites première et troisième bornes, et respectivement entre ladite seconde et ladite troisième borne, lesdites première (46) et seconde (48) bornes dudit premier circuit de pilotage en courant étant couplées aux première (56) et seconde (58) bornes du circuit à réactance équilibrée, respectivement ;

un second circuit (44) de pilotage en courant ayant des première (46), seconde (48) et troisième (78) bornes, ledit second circuit de pilotage en courant étant sensible audit signal de contrôle appliqué pour piloter les premier et second courants proportionnels entre ladite première (46) et ladite troisième (78) bornes et respectivement entre ladite seconde et ladite troisième (78) bornes, ladite première borne étant couplée à ladite première borne dudit premier circuit de pilotage en courant, et ladite seconde borne étant couplée à ladite seconde borne dudit premier circuit de pilotage en courant, lesdits premier et second courants proportionnels étant en opposition de phase par rapport aux premier et second courants proportionnels dudit premier circuit de pilotage en courant ;

des premiers moyens réactifs (72) couplés entre ladite troisième (68) borne et ladite première (46) borne dudit pre-



- mier circuit (42) de pilotage en courant ;
des seconds moyens réactifs (82) couplés entre ladite troisième (78) borne et ladite seconde (48) borne dudit second circuit (44) de pilotage en courant. 5
2. Circuit selon la revendication 1 dans lequel lesdits premiers et seconds moyens réactifs sont des premiers et seconds moyens capacitifs. 10
3. Circuit selon la revendication 2 comprenant :
des premier (116) et second (20) conducteurs d'alimentation électrique ;
un premier transistor (112) ayant une base couplée à ladite première borne (46) dudit premier circuit (42) de pilotage en courant, un collecteur couplé audit premier conducteur d'alimentation électrique, et un émetteur couplé auxdits premiers moyens capacitifs (72) de façon à ce que lesdits premiers moyens capacitifs soient indirectement couplés à la première borne du circuit réactif équilibré ; 15
un second transistor (114) ayant une base couplée à ladite seconde borne (48) dudit premier circuit de pilotage en courant, un collecteur couplé audit premier conducteur d'alimentation électrique (116), et un émetteur couplé auxdits seconds moyens capacitifs (82) de façon à ce que lesdits seconds moyens capacitifs soient indirectement couplés à la seconde borne du circuit réactif équilibré ; et 20
lesdites troisièmes bornes (68, 78) desdits premier et second circuits de pilotage en courant étant couplées audit second conducteur d'alimentation électrique. 25 30 35
4. Circuit selon la revendication 3 comprenant de plus :
des premiers moyens résistifs (138) couplés entre ladite troisième borne (68) dudit premier circuit de pilotage en courant et ledit émetteur dudit second transistor (114) ; et 40
des seconds moyens résistifs (140) couplés entre ladite troisième borne (78) dudit second circuit de pilotage en courant et ledit émetteur dudit premier transistor (112). 45
5. Circuit selon la revendication 4 comprenant :
des troisièmes moyens résistifs (118) couplés entre ledit émetteur dudit premier transistor (112) et ledit second conducteur (20) d'alimentation électrique ; et 50
des quatrième moyens résistifs (120) couplés entre ledit émetteur dudit second transistor (114) et ledit second conducteur (20) d'alimentation électrique. 55
6. Circuit selon la revendication 4, dans lequel ledit premier circuit de pilotage en courant comporte :
des troisième (64) et quatrième (66) transistors dont chacun comporte une base, un collecteur et un émetteur, lesdits émetteurs étant connectés à ladite troisième borne (68), lesdites bases recevant ledit signal de commande appliqué sur elles, ledit collecteur dudit troisième transistor étant connecté à ladite première borne (46) et ledit collecteur dudit quatrième transistor étant connecté à ladite seconde borne (48) ; et
des moyens servant de source de courant (70 ou 122) couplés entre ladite troisième borne et ledit second conducteur d'alimentation électrique.
7. Circuit selon la revendication 6, dans lequel ledit second circuit de pilotage en courant comporte :
des cinquième (74) et sixième (76) transistors, dont chacun comporte une base, un collecteur et un émetteur, lesdits émetteurs étant connectés à ladite troisième borne (78), ledit collecteur du cinquième transistor étant connecté à ladite première borne (46), ledit collecteur dudit sixième transistor étant couplé à ladite seconde borne (48), ladite base dudit cinquième transistor étant couplée à ladite base dudit quatrième transistor, ladite base dudit sixième transistor étant couplée à ladite base dudit troisième transistor ; et,
des moyens servant de sources de courant (80 ou 124) couplés entre ladite troisième borne et ledit second conducteur d'alimentation électrique.
8. Procédé pour produire une réactance variable et contrôlable sur une paire de bornes, comprenant les étapes de:
produire des premier et second courants réactifs en opposition de phase au moyen de premier (72) et second (82) condensateurs ;
produire des premier et second courants proportionnels à partir dudit premier courant réactif ;
produire des troisième et quatrième courants proportionnels à l'aide dudit second courant réactif ;
additionner ledit premier courant réactif, lesdits premier et troisième courants à une première borne de ladite paire de bornes, lesdits premier et troisième courants étant en opposition de phase l'un par rapport l'autre, ledit premier courant étant en opposition de phase avec ledit premier courant réactif ; et



additionner ledit second courant réactif, lesdits second et quatrième courants sur la seconde borne de la paire de bornes.

9. Procédé selon la revendication 8 comprenant de plus une étape de variation de la proportionnalité entre lesdits premier et second courants l'un par rapport l'autre, tandis que l'on fait varier simultanément la proportionnalité dudit troisième courant par rapport audit quatrième courant.

Patentansprüche

1. Integrierter Schaltungsblock mit einem abgeglichenen, veränderbaren Blindwiderstand zur Lieferung eines zwischen zwei Anschlüssen (56 und 58) regelbaren Blindwiderstandes, mit einem ersten drei Anschlüsse (46, 48 und 68) aufweisenden Stromeinstellkreis (42), der auf ein zugeführtes Regelsignal anspricht, um zwei proportionale Ströme zwischen dem ersten und dritten Anschluß bzw. dem zweiten und dritten Anschluß zu steuern, wobei der erste und zweite Anschluß (46 und 48) des ersten Stromeinstellkreises mit dem ersten bzw. zweiten Anschluß (56, 58) der Schaltung mit abgeglichenem Blindwiderstand verbunden ist, mit einem zweiten drei Anschlüsse (46, 48 und 78) aufweisenden Stromeinstellkreis (44), der auf ein zugeführtes Regelsignal anspricht, um zwei proportionale Ströme zwischen dem ersten und dritten Anschluß (46 und 78) bzw. dem zweiten und dritten Anschluß (48 und 78) zu steuern, wobei der erste Anschluß mit dem ersten Anschluß des ersten Stromeinstellkreises und der zweite Anschluß mit dem zweiten Anschluß des ersten Stromeinstellkreises verbunden ist, während die letzteren beiden proportionalen Ströme in Gegenphase zu den beiden proportionalen Strömen des ersten Stromeinstellkreises sind, mit einem ersten einen Blindwiderstand bewirkenden Hilfsmittel (72), das zwischen dem dritten und ersten Anschluß (68 und 46) des ersten Stromeinstellkreises (42) liegt, und mit einem zweiten einen Blindwiderstand bewirkenden Hilfsmittel (82), das zwischen dem dritten und zweiten Anschluß (78 und 48) des zweiten Stromeinstellkreises (44) liegt.
2. Schaltung des Anspruches 1, bei der die beiden einen Blindwiderstand bewirkenden Hilfsmittel zwei Kapazitäten sind.

3. Schaltung des Anspruches 2 mit zwei der Aufladung dienenden Stromleitern (116 und 20), mit einem ersten Transistor (112), dessen Basis mit dem ersten Anschluß (46) des ersten Stromeinstellkreises (42), dessen Kollektor mit dem ersten der Aufladung dienenden Stromleiter und dessen Emitter mit der ersten Kapazität (72) verbunden ist, wobei die erste Kapazität indirekt mit dem ersten Anschluß der Schaltung mit abgeglichenem Blindwiderstand gekoppelt ist, und mit einem zweiten Transistor (114), dessen Basis mit dem zweiten Anschluß (48) des ersten Stromeinstellkreises, dessen Kollektor mit dem ersten der Aufladung dienenden Stromleiter (116) und dessen Emitter mit der zweiten Kapazität (82) verbunden ist, die indirekt mit dem zweiten Anschluß der Schaltung mit abgeglichenem Blindwiderstand gekoppelt ist, wobei der dritte Anschluß (68, 78) der beiden Stromeinstellkreise mit dem zweiten der Aufladung dienenden Stromleiter verbunden ist.
4. Schaltung des Anspruches 3 ferner mit einem ersten Widerstand (138), der zwischen dem dritten Anschluß (68) des ersten Stromeinstellkreises und dem Emitter des zweiten Transistors (114) liegt, und mit einem zweiten Widerstand (140), der zwischen dem dritten Anschluß (78) des zweiten Stromeinstellkreises und dem Emitter des ersten Transistors (112) liegt.
5. Schaltung des Anspruches 4 mit einem dritten Widerstand (118), der zwischen dem Emitter des ersten Transistors (112) und dem zweiten der Aufladung dienenden Stromleiter (20) liegt, und mit einem vierten Widerstand (120), der zwischen dem Emitter des zweiten Transistors (114) und dem zweiten der Aufladung dienenden Stromleiter (20) liegt.
6. Schaltung des Anspruches 4, bei der der erste Stromeinstellkreis die folgenden Bestandteile enthält: einen dritten und vierten jeweils eine Basis, einen Kollektor und einen Emitter aufweisenden Transistor (64 und 66), wobei die Emitter mit dem dritten Anschluß (68) verbunden sind, die Basen das ihnen zugeführte Regelsignal empfangen, der Kollektor des dritten Transistors mit dem ersten Anschluß (46) verbunden ist und der Kollektor des vierten Transistors mit dem zweiten Anschluß (48) verbunden ist, und



eine Stromquelle (70 oder 122), die zwischen dem dritten Anschluß und dem zweiten der Aufladung dienenden Stromleiter liegt.

7. Schaltung des Anspruchs 6, bei der der zweite Stromereinstellkreis die folgenden Bestandteile enthält: 5
- einen fünften und sechsten jeweils eine Basis, einen Kollektor und einen Emitter aufweisenden Transistor (74 und 76), wobei die Emitter mit dem dritten Anschluß (78) verbunden sind, der Kollektor des fünften Transistors mit dem ersten Anschluß (46) und der Kollektor des sechsten Transistors mit dem zweiten Anschluß (48) verbunden ist, während die Basis des fünften Transistors mit der Basis des vierten Transistors und die Basis des sechsten Transistors mit der Basis des dritten Transistors verbunden ist, und 10 15
- eine Stromquelle (80 oder 124), die zwischen dem dritten Anschluß und dem zweiten der Aufladung dienenden Stromleiter liegt. 20
8. Verfahren zum Erzeugen eines veränderbaren und regelbaren Blindwiderstandes an zwei Anschlüssen mit den folgenden Schritten: 25
- zwei in Gegenphase auftretende, durch zwei Kondensatoren (72 und 82) hindurchgehende Blindströme zu erzeugen,
- zwei gegenüber dem ersten Blindstrom proportionale Ströme zu erzeugen, 30
- zwei weitere, gegenüber dem zweiten Blindstrom proportionale Ströme zu erzeugen,
- den ersten Blindstrom und den ersten und dritten Strom an dem einen Anschluß aufzusummieren, wobei der erste und dritte Strom zueinander in Gegenphase ist und der erste Strom in Gegenphase zu dem ersten Blindstrom auftritt, und 35
- den zweiten Blindstrom und den zweiten und vierten Strom an dem anderen Anschluß aufzusummieren. 40
9. Verfahren des Anspruchs 8, bei dem die Proportionalität der beiden Ströme zueinander geändert wird, während gleichzeitig die Proportionalität des dritten Stromes bezüglich des vierten Stromes geändert wird. 45

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* C L M S *

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