What is claimed is:

1. A memory device, comprising:

a memory cell array comprising a plurality of memory cells, each of the plurality of memory cells having a switch element, and a data storage element connected to the switch element and containing a phase-change material; and

a memory controller for obtaining first read voltages from the plurality of memory cells, inputting a first write current to the plurality of memory cells, and then, obtaining second read voltages from the plurality of memory cells, wherein the memory controller compares the first read voltage of a first memory cell of the plurality of memory cells to the second read voltage of the first memory cell to determine a state of the first memory cell, and

wherein the memory controller further comprises:

a first capacitor for charging electric charges corresponding to the first read voltage;

a second capacitor for charging electric charges corresponding to the second read voltage; and

a comparator for adding an offset value to a voltage of the first capacitor, and comparing the voltage of the first capacitor to a voltage of the second capacitor.

2. The memory device of claim 1, wherein the memory controller compares a difference between the first read voltage of the first memory cell and the second read voltage of the first memory cell to a reference value to determine if the first memory cell has a set state or a reset state.

3. The memory device of claim 2, wherein a size of the reference value is based on resistance properties of the data storage elements.

4. The memory device of claim 2 or claim 3, wherein, when the difference between

the first read voltage and the second read voltage is lower than the reference value, the memory controller determines the state of the first memory cell to be the reset state.

5. The memory device of claim 2 or claim 3, wherein, when the difference between the first read voltage and the second read voltage is higher than the reference value, the memory controller determines the state of the first memory cell to be the set state.

6. The memory device of any one of claims 1 to 5, wherein the memory controller sets the state of the first memory cell to a reset state by inputting the first write current to the first memory cell, after obtaining the first read voltage.

7. The memory device of claim 1, wherein, when a portion of the plurality of memory cells are determined to be in a set state, the memory controller inputs a second write current, different from the first write current, to keep the portion of the plurality of memory cells in the set state.

8. The memory device of any one of claims 1 to 7, wherein at least one of the switch elements comprises an ovonic threshold switch (OTS) element.

9. The memory device of any one of claims 1 to 8, wherein the memory controller further comprises:

a first sense amplifier configured to turn on a first switch for charging the first capacitor when a clamping voltage is applied to detect the first read voltage, and to turn on a second switch for charging the second capacitor when the clamping voltage is applied to detect the second read voltage.

10. A memory device, comprising:

a memory cell array comprising a plurality of memory cells, each of the plurality of memory cells having a switch element, and a data storage element connected to the switch element and containing a phase-change material; and

a memory controller for inputting a read current to the plurality of memory cells, sequentially detecting first read voltages and second read voltages from the plurality of memory cells, and comparing the first read voltage of a first memory cell of the plurality of memory cells to the second read voltage of the first memory cell to determine a state of the first memory cell,

wherein an interval between the detection of the first read voltages and the second read voltages is write current free.

11. The memory device of claim 10, wherein the memory controller adds an offset voltage to the first read voltage of the first memory cell, and compares the first read voltage with the offset voltage added thereto to the second read voltage to determine if the first memory cell is in a set state or a reset state.

12. The memory device of claim 11, wherein a magnitude of the offset voltage is determined by a read disturb property of the first memory cell.

13. The memory device of claim 11 or claim 12, wherein, when a sum of the first read voltage and the offset voltage is less than the second read voltage, the memory controller determines the state of the first memory cell to be the set state.

14. The memory device of any one of claims 11 to 13, wherein, when a sum of the first read voltage and the offset voltage is greater than the second read voltage, the memory controller determines the state of the first memory cell to be the reset state.

15. The memory device of any one of claims 10 to 14, wherein after the memory controller detects the second read voltage, the memory controller inputs a write current for setting the state of the first memory cell as a set state to the first memory cell when the first memory cell is determined to be in the set state.

16. The memory device of any one of claims 10 to 15, wherein the read current flows from the switch element to the data storage element in each of the plurality of memory cells.

17. A memory device, comprising:

a memory cell having a switch element, and a data storage element connected to the switch element and containing a phase-change material; and

a memory controller for sequentially detecting a first read voltage and a second read voltage from the memory cell, and comparing the first read voltage to the second read voltage to determine a state of the memory cell as a set state or a reset state,

wherein an interval between the detection of the first read voltages and the second read voltages is write current free, and

wherein, when the state of the memory cell is determined as the set state, the memory controller inputs, to the memory cell, a set write current for setting the state of the memory cell as the set state.

18. The memory device of claim 17, wherein after the memory controller detects the first read voltage from the memory cell, the memory controller inputs a reset write current for setting the state of the memory cell as the reset state to the memory cell, and then, detects the second read voltage.

19. The memory device of claim 17 or claim 18, wherein, when a difference

between the first read voltage and the second read voltage is higher than a reference value, the memory controller determines the state of the memory cell as the set state, and, when the difference between the first read voltage and the second read voltage is lower than the reference value, the memory controller determines the state of the memory cell as the reset state.

20. The memory device of claim 19, wherein the reference value is determined by a resistance property of the data storage element and a read disturb property of the memory cell.