

ABSTRACT OF THE DISCLOSURE

A memory device includes a first switch for switching a first power voltage and transmitting the first power voltage to a common node of a first power rail. A second switch switches a second power voltage and transmits the second power voltage to the common node. A control logic generates a first control signal for controlling the first switch during initial driving of the memory device. A masking circuit controls the first switch to maintain a turn on state in at least a partial period of the initial driving period of the memory device by providing a first masking control signal obtained by masking the first control signal to the first switch.

FIG. 1