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NANOCRYSTAL FLASH MEMORY DEVICE AND MANUFACTURING METHOD THEREFOR

BACKGROUND OF THE INVENTION

TECHNICAL FIELD

The present invention relates generally to Flash memory devices and more particularly to Flash memory devices using nanoncrystals.

BACKGROUND ART

The increasing use of portable electronics and embedded systems has resulted in a need for low-power high-density non-volatile memories that can be programmed at very high speeds. One type of memory, which has been developed, is Flash electrically erasable programmable read only memory (Flash EEPROM). It is used in many portable electronic products, such as personal computers, cell phones, portable computers, voice recorders, etc. as well as in many larger electronic systems, such as cars, planes, industrial control systems, etc.

A Flash EEPROM device is formed on a semiconductor substrate. In portions of the surface of the substrate, a doped source region and a doped drain region are formed with a channel region therebetween. A tunnel silicon oxide dielectric layer is formed on the semiconductor substrate over the channel region and between the source and drain regions. Above the tunnel silicon oxide dielectric layer, over the channel region, a stacked-gate structure is formed for a transistor having a floating gate layer, an inter-electrode dielectric layer, and a control gate layer. The source region is located on one side of the stacked gate structure with one edge of the source region overlapping the gate structure. The drain region is located on the other side of the stacked gate structure with one edge overlapping the gate structure. The device is programmed by hot electron injection and erased by Fowler-Nordheim tunnelling.

A silicon (Si) nanocrystal Flash EEPROM device has been proposed that can be programmed at fast speeds (hundreds of nanoseconds) using low voltages for direct tunneling and storage of electrons in the silicon nanocrystals. By using nanocrystal charge storage sites that are isolated electrically, charge leakage through localized defects in the gate oxide layer is presumably reduced.

A germanium (Ge) nanocrystal Flash EEPROM device has also been demonstrated that can be programmed at low voltages and high speeds. Such a device was fabricated by implanting germanium atoms into a silicon substrate. However, the implantation process can cause germanium to locate at the silicon-tunnel oxide interface, forming trap sites that can degrade the device performance. The presence of such trap sites places a lower limit to the thickness of the resulting tunnel oxide, because defect-induced leakage current in a very thin tunnel oxide can result in poor data retention performance.

Solutions to these problems have been long sought, but have long eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

The present invention provides a Flash memory having a trilayer structure of rapid thermal oxide (RTO)/germanium (Ge) nanocrystals in SiO_2/sputtered SiO_2 cap. This structure has been demonstrated with via capacitance versus voltage (C-V) measurements having memory hysteresis due to germanium nanocrystals in the middle layer of the trilayer structure. The Ge nanocrystals are synthesized by rapid thermal annealing (RTO) of co-sputtered Ge+SiO_2 films.

The present invention provides a method for obtaining a Flash memory structure of Ge nanocrystals synthesized by RTA technique and discloses that the Ge nanocrystal growth is critically dependent on the Ge concentration and the rapid thermal anneal RTA processing conditions.

Certain embodiments of the invention have other advantages in addition to or in place of those mentioned above. The advantages will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a chart of the capacitance versus voltage (C-V) characteristics of various multi-layer structure devices;

FIG. 2 is a diagram representative of a transmission electron microscope (TEM) micrograph of one of the devices of FIG. 1;

FIG. 3 is a diagram representative of a TEM micrograph of another of the devices of FIG. 1;

FIG. 4 is a schematic diagram of a nanocrystal Flash memory device according to the present invention;

FIG. 5 is a diagram representative of a transmission electron micrograph of a TEM micrograph of the nanocrystal Flash memory device according to the present invention;

FIG. 6 is a Flash EEPROM device according to the present invention; and

FIG. 7 is a simplified flow chart according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to FIG. 1, therein are shown capacitance versus voltage (C-V) curves of various experimental devices. The greater the hysteresis, or difference in capacitance upon application of a bias voltage and reversal of the bias voltage, the better the charge storage characteristics, or memory, of the device.

The capacitance versus voltage curves are shown for three devices: Devices 100, 200, 300. Each device includes a semiconductor substrate upon which a multi-layer insulator structure is formed where charges are to be stored. The Device 100 has a trilayer structure of RTO SiO_2 (5nm)/Ge+SiO_2(20nm)/sputtered SiO_2(50nm) cap, where the RTO is a rapid thermal oxide of silicon dioxide of 5nm thickness, the Ge+SiO_2 is a combination of germanium and silicon dioxide of 50nm thickness, and the sputtered silicon dioxide is of a 50nm thickness. The Device 200 has a trilayer structure of RTO SiO_2 (5nm)/sputtered SiO_2(20nm)/sputtered SiO_2(50nm) cap. And the Device 300 has a two-layered structure of RTO SiO_2 (5nm)/Ge+SiO_2(20nm).

The Device 100, which is a trilayer structure, exhibits a counter-clockwise hysteresis of about 6V in the C-V curve as shown in FIG. 1.

The Device 200, which is another trilayer structure with the middle insulator layer consisting of a 20-nm thick pure sputtered oxide, exhibits a counter-clockwise hysteresis about 0.73V. The width of this hysteresis is smaller than the width of the hysteresis of the Device 100.

Not shown is a similar trilayer structure as the Device 200, but omitting a rapid thermal anneal (RTA) step, which showed a hysteresis of 1.09V. This means that the RTA process improves the sputtered oxide quality and reduces the trapped charge density in the Device 200 from 3.62×10^{11} cm^{-2} (as-prepared) to 1.98×10^{11} cm^{-2} (after RTA). The

pronounced hysteresis exhibited by the Device 100 must therefore be due to charge storage in the Ge nanocrystals located at the middle insulator layer. The existence of Ge nanocrystals in the middle layer will be discussed further in the TEM results to be presented later.

The Device 300, which is a two layer device, exhibits a small hysteresis of less than 0.5 volt. The smaller normalized minimum capacitance of the Device 300 is due to a thinner total oxide thickness of 25nm. As there are fewer nanocrystals, it is reasonable to expect that the charge storage capacity will be less compared to the Device 100.

It has also been discovered that the sputtered SiO_2(50nm) cap is important in promoting the Ge nanocrystal growth.

Referring now to FIG. 2, therein is shown a diagram representative of a transmission electron microscope (TEM) micrograph of the Device 100. FIG. 2 is a diagram of the trilayer structure after rapid thermal anneal at 1000°C for 300 seconds. The trilayer structure of the Device 100 is formed on a semiconductor wafer such as a silicon substrate 102 and includes a first insulator layer 104 of 5 nm of RTO SiO_2, a nanocrystal-insulator layer 106 of 20 nm of co-sputtered Ge+SiO_2, and a second insulator layer 108 of 50 nm of pure sputtered SiO_2. The silicon substrate can be either n- or p- doped but is shown as being p-doped.

It can be seen from this diagram that the nanocrystal-insulator layer 106 consists of Ge nanocrystals 110 of different sizes. The trilayer structure of the Device 100 has been subjected to a rapid thermal anneal at 1000°C for 300 seconds.

It should be noted that larger Ge nanocrystals 112 of diameter (δ) ~20 nm were formed near the RTO SiO_2 to sputtered Ge+SiO_2 interface and smaller Ge nanocrystals 114 with δ ~6nm are formed at the RTO SiO_2 to sputtered Ge+SiO_2 and the sputtered Ge+SiO_2 to pure sputtered SiO_2 interfaces. There seems to be more Ge nanocrystals 110 near the RTO SiO_2 to sputtered Ge+SiO_2 interface than the sputtered Ge+SiO_2 to pure sputtered SiO_2 interface. The central region of the nanocrystal-insulator layer 106 contains much fewer Ge nanocrystals 110.

At 1000°C, Ge can diffuse significantly in SiO_2. It is believed that as the concentration of Ge dissolved in SiO_2 is lower than the solubility at the Si to SiO_2 interface and higher at the bulk of the SiO_2, the concentration gradient can lead to a diffusion flux, resulting in an accumulation of Ge at the interface.

It has been discovered that when the Device 100 was annealed at 1000°C, significant Ge diffusion towards the two interfaces took place. The process can account for the larger number of Ge nanocrystals 110 near the two interfaces and the smaller number of Ge

nanocrystals 110 in the central region of the nanocrystal-insulator layer 106. However, the reason is not known for the preferential formation of large Ge nanocrystals 112 and higher number of smaller Ge nanocrystals 114 at the RTO SiO_2 to sputtered Ge+SiO_2 interface.

It should be noted, referring back to FIG. 1, that the Device 100 also shows a significant positive shift of about 4V and a C-V curve with gentler slope as compared to the Device 200. As the hysteresis width is approximately 6V, this means that the Device 100 has a better charge storage capability than the Device 200. It has been suggested that in a system that contained Si-O-Si and Si-O-Ge bonds, the Ge-O bond is weaker and can be broken easily, leaving a Si-O- dangling bond structure. The 1000°C annealed sample contained a substantial amount of GeO_x bonds. This dangling bond structure can then trap an electron and become negatively charged. The significant positive shift of the C-V curve of the Device 100 may be due to the trapping of electrons by the dangling bonds. The gentler slope of the C-V curve of the Device 100 is a result of the large voltage shift induced by the charge stored in the nanocrystals. This was verified by C-V measurements at different delay times, i.e. to simulate different sweep rates.

Referring now to FIG. 3, therein is shown a diagram representative of a TEM micrograph of the Device 200. The three-layer structure of the Device 200 is formed on a silicon substrate 202, which is p-doped, and includes a first insulator layer 204 of 5nm of RTO SiO_2, a middle insulator layer of 20nm of sputtered SiO_2, and a second insulator layer of 50nm of sputtered SiO_2. This is a control device which has no Ge nanocrystals and which, as explained above, indicates that the high level of charge storage is due to the existence of Ge nanocrystals.

Referring now to FIG. 4, therein is shown a diagram representative of a TEM micrograph of the Device 300. The two-layer structure of the Device 300 is formed on a silicon substrate 302, which is p-doped, and includes a first insulator layer 304 of 5nm of RTO SiO_2 and a nanocrystal-insulator layer 306 of 20nm of co-sputtered Ge+SiO_2.

The Device 300 was subjected to a RTA at 1000°C for 300 seconds. It can be seen from FIG. 3 that Ge nanocrystals 310 are only located at the RTO SiO_2 to sputtered Ge+SiO_2 interface. As this device was fabricated without a capping oxide layer, it is reasonable to expect a significant out-diffusion of Ge to occur during RTA at 1000°C.

The C-V characteristic of the Device 300 as seen in FIG. 1 exhibits a small hysteresis of <0.5 V. The smaller normalized minimum capacitance of the Device 300 as compared to the other devices in FIG. 1 is due to a thinner total SiO_2 thickness (25 nm) in the Device 300.

As the Ge nanocrystals are much lesser in number in the Device 300, it is reasonable to expect the charge storage capacity of this device to be lower as compared to the Device 100.

Referring now to FIG. 5, therein is shown a diagram representative of a transmission electron micrograph of a Device 400 having a substrate 402 and including a first insulator 404 and a nanocrystal-insulator layer 406 with Ge nanocrystals 410 formed at the RTO oxide/co-sputtered silicon oxide + Ge interface achieved under optimized fabrication conditions.

An example of the C-V curve of the Device 100 (not fully optimized) containing the various layers described above is shown in FIG. 1. This figure shows the charge storage capability of the proposed structure. It is to be noted that the range of gate voltages at depletion for the two logic states of the device can be further optimized by changing the thickness of the various layers of the Device 100.

Referring now to FIG. 6, therein is shown an example of a Flash EEPROM device 500 according to the present invention, which has a metal-insulator-semiconductor (MIS) structure. A silicon substrate 502 has a source region 504 and a drain region 506 with a channel region 508 therebetween. In one embodiment, the silicon substrate 502 and channel region 508 are p-doped and the source and drain regions 504 and 506 are n-doped. A trilayer structure 512 consists of three insulator layers.

A thin (5 nm) SiO_2 layer 514 was grown on the p-type silicon substrate 502 in dry oxygen ambient using rapid thermal oxidation at about 1000°C.

A Ge+SiO_2 layer 516 of a thickness 20 nm was then deposited by the radio frequency (rf) co-sputtering technique. The sputtering target was a 4-inch SiO_2 (99.999% pure) disc with 6 pieces of undoped Ge (10mm × 10mm × 0.3mm) attached. The argon pressure and rf power were fixed at 3×10^{-3} mbar and 100 W, respectively.

A third pure SiO_2 layer 518 (50 nm) was then deposited by rf sputtering in argon at a rf power of 100W and sputtering pressure at 3×10^{-3} mbar.

The trilayer structure 512 was then rapid thermal annealed (RTA) in argon ambient at a temperature of 1000°C for 300s to form the nanocrystals 510. The RTA ramp-up and ramp-down rates were fixed at about 30°C/second.

The polysilicon control gate 520 was formed over the SiO_2 layer 518.

The present invention uses rf co-sputtering to form the germanium nanocrystal-insulator layer 106. Since a high-quality SiO_2 layer 514, which is a thin tunnel oxide, can be grown by rapid-thermal oxidation prior to the sputtering process, the silicon to oxide interface

of the first insulator layer 104 can be of a very good quality as ion-implantation damage is non-existent. The first insulator layer 104 also serves as a barrier to "line up" the Ge nanocrystals 510 at the oxide-sputtered layer interface during high-temperature rapid thermal annealing of the oxide-sputtered layer.

The structure consists of a rapid thermal oxide layer/SiO_2 layer with a Ge nanocrystals/sputtered silicon oxide cap layer. The Ge nanocrystals are responsible for the charge storage. In order for the proposed device to function well as a low-voltage high-speed Flash memory device (i.e., to have low write and erase voltages and short write and erase pulse duration), the Ge nanocrystals must lie as close to the Si substrate as possible (i.e., located at the RTO oxide/sputtered SiO_2+Ge layer interface).

The fabrication process steps of the proposed device are as follows:

(1) A good quality thin (about 2 – 5 nm) thermal oxide is grown on Si wafer by rapid thermal oxidation in a dry oxygen ambient.

(2) A layer of silicon oxide film that contains Ge nanocrystals is deposited. This layer is first deposited by co-sputtering silicon dioxide and Ge targets to obtain a germanium-silicon-oxide layer with a thickness of about 3 to 20 nm. The Ge concentration in the matrix can be varied from about 1 to 5 atomic percentage (at.%). The sputtering conditions are about: a sputtering pressure of 5 mTorr of argon (Ar) and a radio frequenty (rf) power of 100W. The nanocrystal formation will be carried out after step (5) is completed.

(3) A layer of silicon oxide of about 20 nm is deposited by rf sputtering of a pure silicon dioxide target at 5 mTorr at 100W.

(4) The structure, consisting of 3 layers, is rapid thermal annealed at about 800 - 1000°C for about 50 to 300 seconds in Ar.

It is to be noted that the distribution and size of the Ge nanocrystals are critically dependent on:

(1) The thickness of the rapid thermal oxide layer.

(2) The deposition of the Ge+SiO_2 layer.

(3) The Ge concentration, the RTA temperature and duration.

(4) The thickness of the third sputtered oxide layer or sputtered SiO_2 cap.

Referring now to FIG. 7, therein is shown a simplified flow chart 600 of the manufacturing method of the present invention. The method starts with Provide Silicon Wafer 602, which proceeds to Form First Insulator Layer 604, Form Nanocrystal-Insulator

Layer 606, and Form Second Insulator Layer 608. After the layers are formed, the method proceeds to Rapid Thermal Anneal 610. Subsequently, other steps are used to finish the Flash EEPROM device as well known to those having ordinary skill in the art.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations which fall within the spirit and scope of the included claims. All matters hither-to-fore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

THE INVENTION CLAIMED IS:

1. A method for manufacturing a Flash memory device [500] comprising:
providing a semiconductor wafer [502];
forming a first insulator layer [514] over the semiconductor wafer [502];
forming a nanocrystal-insulator layer [516] over the first insulator layer [514];
forming a second insulator layer [518] over the nanocrystal-insulator layer [516]; and
rapid thermal annealing the first insulator layer [514], the nanocrystal-insulator layer [516], and the second insulator layer [518].

2. The method as claimed in claim 1 wherein:
forming the nanocrystal-insulator layer [516] is performed by co-sputtering nanocrystal material and insulator material.

3. The method as claimed in claim 1 wherein:
forming the nanocrystal-insulator layer [516] uses from 1 to 5 atomic percentage of nanocrystal material.

4. The method as claimed in claim 1 wherein:
forming the second insulator layer [518] uses a sputtering process.

5. The method as claimed in claim 1 wherein:
forming the first insulator layer [514] uses a rapid thermal process.

6. The method as claimed in claim 1 wherein:
rapid thermal annealing the first insulator layer [514], the nanocrystal-insulator layer [516], and the second insulator layer [518] to provide more nanocrystals proximate the first insulator layer [514] to nanocrystal-insulator layer [516] than proximate the nanocrystal-insulator layer [516] to the second insulator layer [518].

7. A Flash memory device comprising:
a semiconductor substrate [502];
a first insulator layer [514] formed over the semiconductor substrate [502];
a nanocrystal-insulator layer [516] formed over the first insulator layer [514];
a second insulator layer [518] formed over the nanocrystal-insulator layer [516]; and
nanocrystals [510] proximate the first insulator layer [514] and the nanocrystal-insulator layer [516].

8. The device as claimed in claim 7 wherein:

the nanocrystal-insulator layer [516] contains from 1 to 5 atomic percentage of nanocrystal material.

9. The device as claimed in claim 7 wherein:

more nanocrystals [510] are proximate the first insulator layer [514] to nanocrystal-insulator layer [516] than proximate the nanocrystal-insulator layer [516] to the second insulator layer [518].

10. The device as claimed in claim 7 including:

sources [504] implanted in the semiconductor substrate [502];

drains [506] implanted in the semiconductor substrate [502] separated from the sources by channels [508]; and

gates [512] formed over the channels [508].