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(54) Title: METHOD AND APPARATUS FOR DYNAMICALLY GENERATING AND MAINTAINING FRAME BASED POLLING SCHEDULES FOR POLLING ISOCHRONOUS AND ASYNCHRONOUS FUNCTIONS THAT GUARANTEE LATENCIES AND BANDWIDTHS TO THE ISOCHRONOUS FUNCTIONS

(57) Abstract

Circuitry and complementary logic are provided to a bus controller (14), a number of 1:n bus signal distributors (18a-18b), and a number of bus interfaces (22a-22f) of an hierarchical serial bus assembly (26') for the bus controller (14) to dynamically generate and maintain a frame based polling schedule for polling the functions of the bus agents (16a-16f) connected to the serial bus assembly (26') and the serial bus elements themselves. The hierarchical serial bus assembly (26') is used to serially interface a number of isochronous (16a, 16d-16f) and asynchronous (16b-16c) peripherals to the system unit of a computer system. The circuitry and complementary logic of the serial bus elements support gathering of various critical operating characteristics by the bus controller (14). The circuitry and logic provided in accordance to these gathered critical operating characteristics guarantee latencies and bandwidths to the isochronous functions of the isochronous (16a, 16d-16f) peripherals. In certain embodiments, the circuitry and logic provided to the bus controller (14) further adapt in real time its frame based polling schedule in like manner, responsive to live attachment/detachment of serial bus elements.

