

PATENT SPECIFICATION

(11) 1 276 745

DRAWINGS ATTACHED

- (21) Application No. 30717/69 (22) Filed 17 June 1969
(31) Convention Application Nos. 41769 925 (32) Filed 17 June 1968
28 Dec. 1968 in
(33) Japan (JA)
(45) Complete Specification published 7 June 1972
(51) International Classification H01L 7/00 C23B 9/00
(52) Index at acceptance
H1K 217 223 22Y 312 353 368 415 416 417 418 41X 41Y 421
422 42X 441 471 474 482 486 490 497 507 511 51Y 520
52Y 530 54Y 55Y 563 581 59Y 611 615 616 618 61Y
63Y 650
C7B 13



(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR DEVICES

(71) We, NIPPON ELECTRIC COMPANY LIMITED, a Company duly organised and existing under the laws of Japan and having its executive office at 7-15 Shiba Gochome, Minato-ku, Tokyo-to, Japan, do hereby declare the invention for which we pray that a Patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and to methods of making such devices.

Semiconductor devices have been developed which afford high reliability and a high degree of integration. The highly integrated circuit device should have a multi-level interconnection structure on the surface of the semiconductor substrate to provide lead-out wirings to each of the semiconductor regions in the substrate.

The lead-out wirings for conventional semiconductor devices are formed by the selective photo-etching of a thin metal film formed by sputtering or vacuum evaporation of metal over the semiconductor substrate. Therefore on the surface of the substrate, a certain degree of unevenness is unavoidable in the lead-out wiring formed in this way. Furthermore, since the overlying wiring layer is formed on the uneven underlying wiring layer, the unevenness is further worsened as the layer is laminated to form the multi-level interconnections.

It is generally known that when the metal layer is deposited on such a structure, the thickness of the metal layer becomes insufficient at the end portions of the remaining uneven surface forming the wiring. Moreover, the end portions are particularly vulnerable to selective etching. As a result, the wirings often become defective to decrease the reliability.

Thus, the conventional technique of select-

ive etching of metal film to form the lead-out and other wirings over the semiconductor substrate, it is almost impossible to provide a highly reliable integrated circuit device, especially having multi-level interconnection structure. This is generally attributed to the unevenness and irregularities formed by the photo-etching process on the multi-layered metal films for wirings and even on the surface of the substrate.

The present invention includes a semiconductor substrate having at least one circuit component formed therein, and a layer comprising at least one metal portion adherent to a part of the surface of said substrate and an insulating portion adherent to a further part of the surface of said substrate, wherein said insulating portion is formed by anode oxidation of the metal of said metal portion.

The invention also includes a method of manufacturing a semiconductor device comprising the steps of depositing a metal film on a surface of a semiconductor substrate having at least one circuit component formed therein, and anode-oxidizing the entire thickness of a selected portion of said metal film, thereby forming a layer having an insulating portion adjacent to a non-selected metal portion.

The layer on the surface of the substrate serves as an electrical connection layer, including at least one electrode or lead-out portion and insulating portions.

A semiconductor device according to the present invention may comprise a first electrical connection layer including conductor portions formed on the semiconductor substrate, an insulating layer which covers the first layer and has a surface substantially parallel to that of the substrate and is substantially flat, and a second electrical connection layer including conductor portions formed on the surface of the insulating layer.

This structure may have further electrical connection layers and insulating layers.

Furthermore, in accordance with the invention, a semiconductor device may be provided in which the surface of each of the electrical connection layers is made substantially flat, by coating the semiconductor substrate with a film of a metal of uniform thickness, and subjecting to anodic oxidation those portions of the metal which do not correspond to the conductive portions to be formed in the finished device, while masking those portions of insulating material which correspond to the conductive portions.

A semiconductor according to this invention can thus be made without selective etching in the formation of metallic portions making it possible to flatten and smooth these portions and the semiconductor substrate.

Experiments have indicated that substances suitable for deposition on the semiconductor substrate include anodisable metals such as aluminium, tantalum, titanium, niobium and hafnium.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figures 1(A) to 1(D) show cross-sectional views of a conventional semiconductor device at various stages in the manufacturing process;

Figure 2(A) is a cross-sectional view of a first semiconductor device according to the invention;

Figure 2(B) is a cross-sectional view of a modification of the embodiment of Figure 2(A);

Figures 3(A) and 3(B) show a perspective and a cross-sectional view, respectively, of a further embodiment of the invention;

Figures 4(A) to 4(F) are cross-sectional views illustrating a method of manufacturing the semiconductor device according to the invention;

Figures 5(A) to 5(E') are cross-sectional views illustrating another method of manufacturing a semiconductor device according to the invention; and

Figure 6 is a perspective view of still another device according to this invention.

Referring to Figures 1(A) to 1(D), a conventional semiconductor device with multi-level interconnection structure is fabricated by forming metal channels 102 on a planar type semiconductor substrate 101 through the selective etching process (Figure 1(A)). An insulating film 103 is then applied uniformly over the substrate and the metal channels 102 (Figure 1(B)).

Although the plane of the semiconductor substrate shown in Figures 1(A) and 1(B) is not irregular, it is usually the case with this type of conventional semiconductor devices that the surface of the substrate (i.e.

the surface of the oxide and other insulative film formed on the semiconductor) is made uneven by the selective photo-etching process used in forming the metallic channels 102. Therefore, the subsequent processes to be described hereunder become extremely difficult. As a result the reliability of the metallic channels are not maintained high.

Referring further to Figures 1(A) and 1(D), it will be noted that a semiconductor device with a multilevel interconnection structure is obtained in the following steps. The surface of the above-mentioned metallic channels 102 is first covered with the insulator film 103. A second layer of metal is then deposited on the insulator film 103 and selectively etched away to provide the second-level metallic channels 104 (Figure 1(C)). In the same manner, another insulator film 105 and a metal film is deposited. Through the selective photo-etching of the last-mentioned metal film, a third-level metallic channel 106 is formed on the insulator film 105 as shown in Figure 1(D).

In this structure, the unevenness of the metal and insulator layer is accumulated towards the surface of the higher level layers.

Also, it has been the practice, in advance of each of the selective etching processes, to form the metal film by vacuum evaporation or sputtering metal particles. In either of these processes the metal particles are deposited on the surface of the substrate. For this reason the vertical portions of deposited metallic layer are thinner and less adherent than the portions parallel to the substrate surface. Furthermore, the photo-resist, when applied on this metallic layer by the roller coating for the selective etching, is subjected to a centrifugal force, and therefore the photo resist adherent to the outward sides of "hills" of the metallic layer becomes thin or less adherent than on the rest of the underlying layer. Accordingly, when metallic channels are provided on a substrate having an appreciably uneven surface, the portions parallel to the surface are more easily broken than the portions parallel to the surface of the basic semiconductor substrate. Experience has indicated that semiconductor devices with the multi-level interconnection structure manufactured by means of the foregoing process have disadvantages in practice. Rather, it has heretofore been found practically impossible to improve the reliability of multi-level connection layers of the type described above.

Referring to Figure 2 which shows an embodiment of the present invention, a semiconductor device 20 comprises a semiconductor substrate 101 which consists of a base substrate of silicon having necessary number of circuit elements and an insulating film of

silicon dioxide formed over the base substrate. The structure of the substrate 101 may be quite similar to the conventional semiconductor device illustrated in Figure 1. On the surface of the substrate 101, a first electrical connection layer is formed of aluminium channels 201 covered with a first insulator film 202 of alumina. The channels 201 are formed by selectively anodic oxidising an aluminium film to form alumina. The alumina film 202 formed in this way has a substantially flat surface parallel to the surface of the substrate 101. The channels 201 serve as electrodes for circuit elements or are mutually interconnected there between derived from the electrode region of the circuit elements. A second electrical connection layer having metal channels 203 formed in an alumina film 204 is formed on the first layer and a third layer having channels 205 in a film 206 is formed on the second layer. A step-by-step explanation of the process of forming the above-mentioned films and layers will be given later referring to Figure 4.

As will be apparent from the foregoing, each of the electrical connection layers is formed on an underlying layer which is so flat that the overlying layer is easily formed thereon and is maintained with high reliability. Moreover, since the underlying layers are formed by the selective anodisation of an aluminium film and not by a photo-etching process, the structure is capable of maintaining sufficient flatness of the underlying surface. It follows therefore that defects attributable to the unevenness involved in conventional structures, can be obviated.

This embodiment can also be realised as well by using other metals suitable for anodic oxidation in place of aluminium, such as titanium or tantalum.

Figure 2(B) shows a semiconductor device 20' in which silicon dioxide films 207 and 208 are interposed between two of the electrical connection layers, respectively. The silicon dioxide films 207 and 208 are formed by a vapour growth or sputtering process, with a view to reducing the capacitance between the aluminium channels 201 and 203 in each electrical connection layer.

In this embodiment, silicon dioxide films may be substituted by other insulating material such as ceramics, glass and metal oxide deposits by vapour evaporation or sputtering.

Referring to Figure 3(A), a further semiconductor device 30 according to the invention has, on a semiconductor substrate 101, first and second electrical connection layers formed in the above-described manner. The first electrical connection layer consists of aluminium channels 201 in an alumina film 202 and the second layer consists of aluminium channels 203 in another alumina film

204. On the upper layer of this embodiment, there are provided a plurality of protruding electrodes 301 which connect the desired portions of upper channels 203 through the openings formed in the alumina film 204. Also, the protruding electrodes 301 are formed through the technique well known in flip-chip semiconductor devices, in which solder balls, electroplated bumps or beam leads are employed as the bonding electrode to the outer circuit.

Figure 3(B) shows a semiconductor device having a flip-chip type semiconductor dice similar to that of Figure 3(A) attached to the leads 302 adherent to the surface of the ceramic substrate 303. At the bonding portion, the inside edges of the leads 302 have protrusions 304. These protrusions 304 are firmly attached to the exposed surfaces of the channels 201 of the semiconductor dice. The semiconductor dice of the embodiment has the structure illustrated in Figure 3. More particularly, the dice has a substantially flat surface coated with the insulated film formed through the anodic oxidation process. This semiconductor device of the face-bonded structure is easy to manufacture with the high reliability maintained.

Figures 4(A) to (F) show a preferred method of manufacturing a semiconductor device according to the present invention in the order of the steps of processing. The method involves a series of selective anodisation processes, as described hereunder.

In the first place, semiconductor substrate 101 with circuit elements yet to be processed for internal and external connections is uniformly covered with a 1-micron-thick aluminium film 401 deposited by a vacuum evaporation process (Figure 4(A)). The surface of this aluminium film 401 is covered with a photo resist layer 402 (Figure 4(B)), at those portions other than the portion which is to form an aluminium channel in the finished device. Using the photo resist 402 as a mask, the semiconductor substrate 101 with the aluminium film 401 on it is connected to a positive electrode and the anode forming solution is maintained at a negative potential and then anodic oxidation is carried out. Thus, the exposed surface of aluminium film 401 is selectively covered by non-porous alumina 403 (Figure 4(C)). This non-porous alumina is formed by the constant-voltage anodisation with an ammonium-borate solution saturated with ethylene glycol employed as the anodizing agent. In this process, the voltage applied is 40 to 45 volts and the processing time is about 3 minutes. If the voltage is too high or if the processing time is too long the photo resist loses its adherence to the aluminium surface, particularly at the peripheries of the photo resist film.

After the non-porous anode-oxidised layer is completed, the photo resist 402 is re-

70

75

80

85

90

95

100

105

110

115

120

125

130

5 moved from the aluminium surface by a suitable removing agent (Figure 4(D)). The selectively formed portion 403 of non-porous alumina serves as a mask during further anodisation which changes the unmasked aluminium film 401 to porous alumina (Figure 4(E)). Upon completion of this step, the insulating film is formed of non-porous alumina 403 and porous alumina 404 and an aluminium channel 201 covered with alumina forms the wiring layer. The solution for converting aluminium into porous alumina may be 2% sulphuric acid supplied to the aluminium at a temperature of 20°C. Constant voltage formation is performed at 20 volts. Finally, the first of the above-mentioned anodisation processes is repeated to form non-porous alumina 405 on both sides of the aluminium channel 201 for stabilising the chemical and electrical properties of the connection layer (Figure 4(F)).

25 The anodic oxidation in this final stage of processing begins with a constant-current formation using the semiconductor substrate as the anode. When the forming voltage reaches a certain level of 100 to 150 volts, the operation is switched over to constant-voltage formation. By this treatment non-porous alumina 405 is formed on the sides of the aluminium channel 201. The thickness of the non-porous alumina film 403 initially formed on the surface of the channel 201 is thus slightly increased to approx. 0.1 to 0.3 micron. In addition, the aluminium partially left in the course of forming the porous alumina can be almost completely changed to alumina.

35 As has been described above, the aluminium film deposited on the substrate by evaporation or sputtering can be selectively anodized with ease to form the alumina film, an insulating film. The surface of the alumina thus obtained is entirely flat and facilitates subsequent steps of processing. The formation of the multi-level interconnection is accomplished by providing openings in the portion of the non-porous alumina through which the channel can be electrically connected with the channel of the overlying layer, and then by repeating the above-described process illustrated in Figure 4. In order to form the openings in the non-porous alumina, an etching solution prepared by diluting a mixture of 35 g. chromic acid anhydride and 20 cc, phosphoric acid with one litre water is applied to the non-porous alumina at 70° to 75°C.

60 Since the non-porous alumina is proof against the processing agent for the porous alumina, the aluminium film is unfailingly changed to the porous alumina through this process. In addition, the forming process can be easily controlled by regulating the forming voltage of forming current.

65 Figures 5(A) to (E') show another pre-

ferred method of fabricating a semiconductor device in accordance with the present invention. This method comprises steps similar to those of Figure 4(A) in that a thin film of aluminium 401 is first deposited on the surface of a semiconductor substrate 101 (Figure 5(A)). A photo resist layer 501 is then applied to partially cover the aluminium film 401 where the aluminium channels are to be formed later (Figure 5(B)). The portion of the aluminium film 401 where the photo-resist is selectively removed is anodized to form porous alumina 404, using a photo-resist 501 as a mask against anodization (Figure 5(C)). The photo resist 501 is then removed. Then, a uniform, non-porous layer of alumina 502 is formed covering an aluminium channel 201 therein (Figure 5(D)). Thereafter, the non-porous alumina is selectively removed from above the desired portion 503 of channel 201. The portion 503 in an opening either for a connection with a metallic channel in the overlying layer or for an external lead-out electrode (Figure 5(E)).

Also, when it is desirable to expose a part of the channel 201 on the same plane as the surface of the alumina film, for facilitating to lead-out the external electrodes, the process of forming porous alumina 404 as indicated in Figure 5(C) may be followed by the provision of a mask 504 of photo resist adherent to the electrode lead-out portion on the surface of the aluminum film 401 (Figure 5(D')). Then, the non-porous alumina film 505 is formed. In this process, the mask 504 of photo resist may be substituted by acid-proof metal or alloy.

In the embodiment just described, the porous alumina 404 and non-porous alumina 502 are formed under the same conditions as in the formation of the porous alumina 404 and non-porous alumina 405 already explained in connection with the first manufacturing method.

As will be seen from the foregoing, an electrical connection layer consisting of metallic channels and an insulating film formed by the above-described process can be flat irrespective of how many such layers are laminated to form a multi-level interconnection structure. Admittedly there may be a change in volume at the time of conversion of aluminium in alumina. However, any unevenness attributable to this change in volume is almost negligible compared with that involved in the conventional device shown in Figure 1.

Even if the above-mentioned change in volume causes an appreciable unevenness over the surface of the anodic oxidation film it does not adversely affect the formation of a flat overlying electrical connection layer, because the boundary between the aluminium channels and alumina has an

70

75

80

85

90

95

100

105

110

115

120

125

130

extremely gradual gradient. Moreover, the resultant semiconductor device withstands scratching and deposition of foreign matters of the connection layer, because the conductive channels in the layer are protected by solid alumina.

In conventional semiconductor devices having aluminium channels, an alloying action which takes place in the course of heat treatment after the formation of the channel may lead to recrystallization of aluminium to form tiny protrusions on the surface of the aluminium channels or cracks in the insulator film deposited on the channels. According to the instant invention, almost entire parts of aluminium channels are buried in the alumina layer so that the channel shows no tendency of deterioration. Cracks are totally avoidable in the alumina film.

Referring to Figure 6, a field effect transistor 60, which is still another embodiment of the present invention, has a semiconductor substrate 101 so fabricated that drain and source regions 601 and 602 on n-type conductivity are formed in a p-type silicon substrate 603 in the same way as in conventional devices. An insulating film adherent to the surface, which has been used as a mask for the selective impurity diffusion, is completely removed to expose the whole surface of the semiconductor substrate 603. Then, a thin film of silicon dioxide 604, about 0.25 micron thick, is uniformly deposited on the substrate surface. The film 604 covers the entire surface of the same one major surface of the substrate 603 with the exception of the electrode openings for the drain and source regions, 601 and 602. The film portion 604' of the deposited film 604 between the drain and source of the field effect transistor serves as an insulated gate film. On the top surface of the semiconductor substrate 101 an aluminium film of uniform thickness of about one micron is deposited by vacuum evaporation. On each of the top portions where the gate, drain and source electrodes 605, 606 and 607 are to be formed, a photo resist film is applied. The aluminium film apart from these electrodes 605 to 607 is anodized in dilute sulphuric acid with a concentration of 2% at a temperature of 20°C. The forming voltage for this purpose is 20 volts, and forming is carried out at constant voltage. On completion of this anodizing step, the aluminium layer is converted into a first electrical connection layer composed of the gate electrode 605; drain electrode 606; and source electrode 607 which had been covered by the photo resist; and electrode 608 of another circuit element; and an alumina insulating film 609 which surrounds those electrodes. In this embodiment, channels 610, 611 and 612 for the second channel layer are subsequently formed

in the usual manner to provide interconnection for the respective circuit elements.

As will be seen from the description of the drawings, etching is not resorted to in forming the electrodes 605, 606, 607 and 608. The lowermost layer 604 of the insulating films is thin compared with those in the substrate formed by planar technique. The thickness of the layer 604 may be about one third of the aluminium film 605. The electrodes thus obtained are therefore highly reliable.

Also, the overlying channel layers 610, 611 and 612 can be readily formed with an adequately high reliability, because the surface of the first electrical connection layer is flat, smooth, and substantially parallel to the surface of the substrate 101.

This embodiment permits the use of different materials for the two groups of electrodes, i.e., the underlying layer electrodes 605, 606, 607 and 608 and the overlying layer electrodes 610, 611 and 612, with a view to facilitating the formation of the overlying interconnection. In addition, the overlying layer channels can be formed by anodic oxidation like those of the underlying layer.

By so doing, the reliability of the overlying layer against mechanical shock such as scratching of the upper layer channels can be improved.

While the description has been made in the foregoing in conjunction with semiconductor devices having at least one electrical connection layer in turn consisting of aluminium channels and an alumina layer formed through the selective anodic oxidation of the aluminium sheet it is to be understood that the objects of the present invention can be also attained by substituting aluminium with titanium, tantalum, niobium hafnium or other anodisable metal.

The principal advantage of the above devices are as follows. Since the electrical connection layers are formed through anodization, and not through the photo-etching, each of the layers is flat, irrespective of how many layers are laminated on the substrate. This is in sharp contrast to conventional devices wherein unevenness is unavoidable in a multi-layered interconnection structure. Semiconductor devices to which the above-described electrical connection layers are applicable are not restricted to plane semiconductor substrate coated with silicon dioxide. They may be mesa type devices coated with insulating films. The silicon dioxide film adherent to the semiconductor base substrate may be coated with other insulator films, such as silicon nitride, phosphosilicate glass, alumina-silicate glass, alumina formed by evaporation, sputtering or vapour growth process.

Moreover, it is possible to further improve

70

75

80

85

90

95

100

105

110

115

120

125

130

the stability of the characteristics of the semiconductor device through the thermal treatment in water vapour heated up to about 400°C. Also, it is possible to facilitate the process control and the quality checking of the completed device, by way of differentiating the electrical connection layers with colourants of insulative material, e.g., manganese oxide, cobalt oxide, copper oxide, iron oxide, and chromium oxide.

It would be apparent to those skilled in the art that further modifications of the embodiment one possible without departing from the scope of the invention. It is therefore to be understood that the foregoing description is made by way of example and not as a limitation to the scope of the invention as defined in the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor substrate having at least one circuit component formed therein, and a layer comprising at least one metal portion adherent to a part of the surface of said substrate and an insulating portion adherent to a further part of the surface of said substrate, wherein said insulating portion is formed by anode oxidation of the metal of said metal portion.

2. A semiconductor device as claimed in claim 1, wherein there is at least one layer of insulating material between said substrate and said layer.

3. A semiconductor device as claimed in claim 2, wherein at least one window is provided in said layer of insulating material, and said metal portion is electrically connected through said window to said circuit component formed in said substrate.

4. A semiconductor device as claimed in claim 1 or 2, wherein each of metal portion and said insulating portion has a surface substantially parallel to the surface of said substrate.

5. A method of manufacturing a semiconductor device comprising the steps of depositing a metal film on a surface of a semiconductor substrate having at least one circuit component formed therein, and anode-oxidizing the entire thickness of a selected portion of said metal film, thereby forming a layer having an insulating portion adjacent to a non-selected metal portion.

6. A method as claimed in claim 5, wherein the anode-oxidization is carried out in at least two stages so that a part of said insulating portion which is continuous with said non-selected metal portion of said layer differs in at least one physical property from the remainder of said insulating portion.

7. A method as claimed in claim 6, wherein said metal portion is aluminium, said part of said insulating portion is non-porous

alumina and the remainder of said insulating portion is porous alumina.

8. A method as claimed in any one of claims 5 to 6, wherein the metal deposited on said substrate is aluminium, and the anodic oxidation converts the selected portion of the aluminium to alumina.

9. A method as claimed in claim 5, wherein the metal deposited on said substrate is tantalum, titanium, niobium or hafnium.

10. A method of manufacturing a semiconductor device comprising the steps of preparing a semiconductor substrate including at least one circuit component therein and having an insulating film at one surface thereof, said insulating film having at least one opening formed therein, depositing a metal film on said semiconductor substrate, said metal film being electrically connected to said semiconductor substrate through said opening in said insulating film, and selectively anode-oxidizing said metal film thereby to convert said metal film into conductive channels isolated from one another by the resulting oxide of the metal of said metal film.

11. A method as claimed in claim 10, wherein said metal film deposited on said semiconductor substrate is comprised of a metal selected from the group consisting of aluminium, titanium, tantalum, niobium and hafnium.

12. A method as claimed in claim 10, wherein said selective anode-oxidizing step includes the steps of masking portions of said metal film at the locations of said intended conductive channels, at least one of said intended conductive channels being electrically connected to said semiconductor substrate through said opening in said insulative film and converting the entire thickness of the masked area of said metal film to anodized oxide.

13. A method as claimed in claim 12, wherein said metal film is comprised of aluminium or tantalum.

14. A method as claimed in claim 10, wherein said selective anode-oxidizing step includes the steps of masking a selected portion of said metal film at a location of an intended insulating area, converting a partial thickness of the unmasked area of said metal film to anodized non-porous oxide, unmasking the portion of said metal film previously covered, and converting the entire thickness of the previously masked portion of said metal film to anodized porous oxide.

15. A method as claimed in claim 14, further including the step of converting small peripheral portions of said conductive channels into anodised non-porous oxide.

16. A method as claimed in claim 14, wherein said metal film is comprised of aluminium.

17. A method as claimed in claim 10,

65

70

75

80

85

90

95

100

105

110

115

120

125

the stability of the characteristics of the semiconductor device through the thermal treatment in water vapour heated up to about 400°C. Also, it is possible to facilitate the process control and the quality checking of the completed device, by way of differentiating the electrical connection layers with colourants of insulative material, e.g., manganese oxide, cobalt oxide, copper oxide, iron oxide, and chromium oxide.

It would be apparent to those skilled in the art that further modifications of the embodiment one possible without departing from the scope of the invention. It is therefore to be understood that the foregoing description is made by way of example and not as a limitation to the scope of the invention as defined in the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor substrate having at least one circuit component formed therein, and a layer comprising at least one metal portion adherent to a part of the surface of said substrate and an insulating portion adherent to a further part of the surface of said substrate, wherein said insulating portion is formed by anode oxidation of the metal of said metal portion.

2. A semiconductor device as claimed in claim 1, wherein there is at least one layer of insulating material between said substrate and said layer.

3. A semiconductor device as claimed in claim 2, wherein at least one window is provided in said layer of insulating material, and said metal portion is electrically connected through said window to said circuit component formed in said substrate.

4. A semiconductor device as claimed in claim 1 or 2, wherein each of metal portion and said insulating portion has a surface substantially parallel to the surface of said substrate.

5. A method of manufacturing a semiconductor device comprising the steps of depositing a metal film on a surface of a semiconductor substrate having at least one circuit component formed therein, and anode-oxidizing the entire thickness of a selected portion of said metal film, thereby forming a layer having an insulating portion adjacent to a non-selected metal portion.

6. A method as claimed in claim 5, wherein the anode-oxidization is carried out in at least two stages so that a part of said insulating portion which is continuous with said non-selected metal portion of said layer differs in at least one physical property from the remainder of said insulating portion.

7. A method as claimed in claim 6, wherein said metal portion is aluminium, said part of said insulating portion is non-porous

alumina and the remainder of said insulating portion is porous alumina.

8. A method as claimed in any one of claims 5 to 6, wherein the metal deposited on said substrate is aluminium, and the anodic oxidation converts the selected portion of the aluminium to alumina.

9. A method as claimed in claim 5, wherein the metal deposited on said substrate is tantalum, titanium, niobium or hafnium.

10. A method of manufacturing a semiconductor device comprising the steps of preparing a semiconductor substrate including at least one circuit component therein and having an insulating film at one surface thereof, said insulating film having at least one opening formed therein, depositing a metal film on said semiconductor substrate, said metal film being electrically connected to said semiconductor substrate through said opening in said insulating film, and selectively anode-oxidizing said metal film thereby to convert said metal film into conductive channels isolated from one another by the resulting oxide of the metal of said metal film.

11. A method as claimed in claim 10, wherein said metal film deposited on said semiconductor substrate is comprised of a metal selected from the group consisting of aluminium, titanium, tantalum, niobium and hafnium.

12. A method as claimed in claim 10, wherein said selective anode-oxidizing step includes the steps of masking portions of said metal film at the locations of said intended conductive channels, at least one of said intended conductive channels being electrically connected to said semiconductor substrate through said opening in said insulative film and converting the entire thickness of the masked area of said metal film to anodized oxide.

13. A method as claimed in claim 12, wherein said metal film is comprised of aluminium or tantalum.

14. A method as claimed in claim 10, wherein said selective anode-oxidizing step includes the steps of masking a selected portion of said metal film at a location of an intended insulating area, converting a partial thickness of the unmasked area of said metal film to anodized non-porous oxide, unmasking the portion of said metal film previously covered, and converting the entire thickness of the previously masked portion of said metal film to anodized porous oxide.

15. A method as claimed in claim 14, further including the step of converting small peripheral portions of said conductive channels into anodized non-porous oxide.

16. A method as claimed in claim 14, wherein said metal film is comprised of aluminium.

17. A method as claimed in claim 10,



- wherein said selective anode-oxidizing step includes the steps of masking portions of said metal film at locations of the intended conductive channels, converting the entire thickness of the unmasked area of said metal film to anodized porous oxide, unmasking the portions of said metal film previously covered, and converting a partial thickness of at least a part of the surface of the previously masked portions of said metal film to anodized non-porous oxide.
18. A method as claimed in claim 17, wherein said metal film is comprised of aluminium.
19. A method as claimed in claim 18, wherein small peripheral portions of said conductive channels are converted to anodized non-porous oxide.
20. A method as claimed in claim 19, wherein the whole surface of said previously masked portions of said metal film is converted to anodized non-porous oxide film to a partial thickness and an opening is provided in each anodized non-porous oxide film covering each of said previously masked portions.
21. A semi-conductor device constructed and arranged substantially as hereinbefore described with reference to, and as illustrated in, any of Figures 2 to 6 of the accompanying drawings.
22. A method of making a semiconductor device substantially as hereinbefore described with reference to, and as illustrated in, any of Figures 2 to 6 of the accompanying drawings.
- MATHYS & SQUIRE,
Chartered Patent Agents,
10 Fleet Street,
London, EC4Y 1AY.

(9166)

Printed in Scotland by Her Majesty's Stationery Office
at HMSO Press, Edinburgh, 1972.

Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.



* C L M S *