

HIGH VOLTAGE CMOS OUTPUT DRIVER IN LOW VOLTAGE PROCESS

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Field of the Invention

The invention relates generally to semiconductor circuitry, and more specifically to a high voltage CMOS output driver in a low voltage semiconductor process.

Background of the Invention

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While semiconductor circuitry such as bipolar and CMOS circuitry has traditionally operated at a five volt potential difference between a high and a low signal level, the need for higher speed, lower power consumption, and lower heat dissipation has prompted a move to lower voltage circuitry. It is now common for such semiconductors to operate at voltage levels of 3.3 or 2.5 volts, allowing fabrication of

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such higher performance semiconductor devices. Although such devices are capable of a higher level of performance in many respects than older five volt semiconductors, they often must be integrated into designs or products utilizing the older five volt technology and so must be designed to interface with such circuitry. These lower voltage semiconductors are often designed to receive

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either a five volt signal or a lower voltage signal in the same device, making integration into older systems relatively easy where the newer low voltage semiconductors must receive signals.

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But, these lower voltage semiconductors cannot provide a five volt output signal as easily as they can receive one. Because the fabrication processes used in these lower voltage semiconductors comprise standard transistor geometries designed to conduct only lower voltages, they are not physically capable of reliably providing a full five volt output signal.

What is desired is a high voltage output driver capable of providing a high voltage output signal in a low voltage process semiconductor.

Summary of the Invention

The invention described here provides a high-voltage output buffer implemented in a low-voltage semiconductor process, enabling low-voltage semiconductors to interface with high-voltage circuitry. The buffer comprises a level translator circuit that in operation receives a signal varying between ground and a low voltage level, and outputs a corresponding signal varying between a reference voltage level and a high voltage level. The reference voltage level is an intermediate voltage level between half of the low voltage level and the high voltage level. The buffer also comprises an output circuit that in operation receives the output of the level translator circuit, and outputs a corresponding high voltage level when the input is a high voltage level or a zero voltage level when the input is at the reference voltage level. The low voltage supply in some embodiments of the invention is derived from the greater of an external low voltage supply or the reference voltage derived from the high voltage supply, so that the transistors of the buffer are protected from high voltages in the event of an external low voltage supply failure.

Brief Description of the Figures

Figure 1 shows a block diagram of an output buffer circuit, consistent with an embodiment of the present invention.

Figure 2 shows a five-volt output buffer circuit, consistent with an embodiment of the present invention.

Figure 3 shows an adaptation of the five-volt output buffer circuit of Figure 1 to a lower voltage output, consistent with an embodiment of the present invention.

Detailed Description

In the following detailed description of sample embodiments of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific sample embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other

embodiments may be utilized and that logical, mechanical, electrical, and other changes may be made without departing from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the invention is defined only by the appended claims.

5 The present invention provides a high voltage output driver capable of providing a high voltage output signal in a low voltage process semiconductor. The output buffer of one embodiment of the invention does this by use of a level translator circuit and an output circuit, examples of which are described in greater detail herein.

Figure 1 illustrates one such embodiment of an output buffer having a level
10 translator stage 101 and an output circuit 102. The level translator circuit receives an input signal 103 varying between a ground or zero volt level and the low voltage V_L that is the voltage level at which the semiconductor process used to fabricate the circuit is designed to operate. The level translator circuit 101 translates the received voltage signal 103 and outputs at 104 a signal varying between a reference voltage V_{ref} and a
15 high voltage level V_h . That is, when the level translator receives a ground or zero input voltage it outputs the voltage V_{ref} , and when the translator receives a low voltage level V_L it outputs a high voltage level V_h . The reference voltage V_{ref} is in some embodiments of the invention an intermediate voltage selected to be approximately half way between the low voltage level V_L and ground. In application, the V_{ref} voltage
20 signal output by the level translator may be somewhat higher than V_{ref} , such as V_{ref} plus the threshold voltage of a certain transistor. This will be explained in greater detail in other example embodiments of the invention.

Next, an output circuit 102 receives the signal 104 which varies between approximately V_{ref} to V_h , and translates it to an output signal 105 ranging between
25 ground or V_0 and V_h . When the output circuit receives a signal at level V_{ref} it outputs a signal at V_0 , and when the circuit receives a signal at V_h it outputs a signal at level V_h .

When the level translator and the output circuit are taken in combination to form a complete output buffer circuit, the output buffer circuit therefore will output a voltage
30 level V_0 at 105 when a V_0 voltage level is received at the input 103, and will output a high voltage level V_h at 105 when a low voltage level V_L is received at 103.

The invention is operable to output a voltage level at a single output 105 that ranges across a broader range of voltage (V_0 to V_h) than the semiconductor design process permits to be applied across any single transistor because of the unique structure of the output buffer circuit.

5 A detailed view of an embodiment of the output buffer circuit showing individual transistors is shown in Figure 2, demonstrating how the present invention may be constructed to avoid applying a greater voltage than V_I across any transistor of the buffer circuit. In this example, V_I is 3.3v, which indicates that the circuits are built using a 3.3v semiconductor fabrication process. The supply voltage V_{dd} is therefore
10 also 3.3 volts, supplying the circuit with the traditional operating voltage as a power source.

V_{ref} is defined for this example as $V_{dd}/2$, and so is therefore approximately 1.66 volts. V_{dd2} is the high voltage level, which in this example embodiment of the invention is a 5 volt power source.

15 The input is received at 201, which ranges from zero or ground (V_{ss}) to V_I , which is 3.3 volts in this example. The input signal is received by the gates of complementary n-channel transistors 202 and 203, where the signal provided to transistor 203 is first inverted by inverter 204. The voltage level V_{dd} , here 3.3 volts, is supplied to the gates of n-channel transistors 205 and 206, and the reference voltage of
20 $V_{dd2}/3$ or approximately 1.66 volts is applied to the gates of p-channel transistors 207 and 208. P-channel transistors 209 and 210 are connected to the voltage source V_{dd2} of 5 volts, and are coupled between the p-channel transistors of the complementary side of the transistor ladders that comprise the level translator as shown.

 In operation, either the transistor 202 or 203 will be switched on, and conduct.
25 For purposes of this example assume a low voltage level at the input, so that transistor 203 conducts and transistor 202 does not. This results in the connection between transistors 203 and 206 being brought to ground level. Transistors 206 conducts due to the voltage V_{dd} applied at the gate, and similarly brings the connection between the transistor 208 and 206 to the voltage level V_{ss} , or ground. Transistor 208 is connected
30 to V_{ref} at its gate, which causes it to conduct and to bring the connection between transistor 208 and 210 to approximately V_{ref} plus the threshold voltage of the PMOS

transistor. Because the threshold voltage in this example is approximately .85 volts and V_{ref} is approximately 1.65 volts, this connection is brought to a voltage level of approximately 2.5 volts.

5 The connection between transistors 208 and 210 is cross-linked to the gate of transistor 209, and is sufficient to turn transistor 209 on as its drain is connected to a five volt source. The connection between transistors 209 and 207 is therefore brought to five volts, and the connection 211 between the level translator and output stages of the circuit is at a five volt level.

10 The output stage receives the five volt input at transistor 212, which also has its drain connected to five volts, and so remains off. Transistor 213 receives a 3.3 volt signal from the inverter 204, and so is on. The connection between transistor 213 and 214 is therefore brought to ground, and the voltage V_{dd} applied to transistor 214. Transistor 214 similarly conducts the output 216 to ground. Because transistor 212 is off, it does not matter for purposes of determining the output signal whether transistor 215 conducts or
15 does not conduct in this particular example.

But, the junction between transistors 212 and 215 is intentionally controlled in the example circuit of the present invention, to ensure that neither transistor realizes a voltage drop of greater than 3.3 volts across its source and drain. Because transistor 212 is connected at the base to V_{ref} plus the PMOS threshold voltage V_p , the connection
20 between 212 and 215 is brought to $V_{ref} + V_p$. Transistor 215 is on because V_{ref} is applied to its base, but conducts current only from its own capacitance as transistor 212 is off. This controls the voltage drop across both transistors 212 and 215, ensuring that the drop from 5 volts at V_{dd2} to zero volts at the output 216 is shared between these two transistors.

25 If the input applied at 201 is high instead of low, transistors 202, 205, and 207 conduct, and the connection between transistors 207 and 209 is brought to V_{ref} plus the PMOS transistor threshold voltage. This signal is conducted to the level translator output 211, turning on output circuit transistor 212 because it is significantly lower than the drain voltage V_{dd2} . Transistor 213 is off because its input provided by inverter 204 is low, and transistor 215 is on because its gate is connected to V_{ref} , which is below the
30 five volt drain voltage it sees from conducting transistor 212. The output 216 is

therefore connected to Vdd2 via transistors 212 and 215, and provides an output signal of five volts. Transistor 214 is on, bringing the voltage between transistors 213 and 214 to Vdd minus the NMOS threshold voltage V_n , ensuring that the voltage drop between the 5v output at 216 and Vss is shared between transistors 213 and 214. Again, no
5 single transistor is subject to a drain-to-source voltage of greater than 3.3 volts, making fabrication of the circuit using a 3.3 volt semiconductor process viable.

In a further embodiment of the invention, the dual power Vdd and Vdd2 signals supplied to the circuit of Figure 2 may be both brought to 3.3 volts, in which case the same circuit may be used as a 3.3 volt output buffer. Figure 3 illustrates how tracing
10 through the same circuit as illustrated in Figure 2 but with the supply voltage Vdd2 changed to 3.3 volts and the reference voltage Vref changed to 0 volts yields a 3.3 volt buffer. This enables using the same circuit to provide either 3.3v or 5v output signals, changing only the supply voltage Vdd2.

In Figure 3, the numbering has been kept consistent with the numbering of
15 Figure 2 for easy reference. Because Vdd2 is reduced to 3.3 volts, Vref no longer needs to be derived as an intermediate voltage to limit the maximum voltage drop across a single transistor. It is therefore set to zero volts, and the circuit functions in the same way as the circuit of Figure 2 but with an output signal of 0 to 3.3 volts.

Because the invention will in many embodiments operate within an integrated
20 circuit fabricated in a low voltage process but having both low and high voltage power connections, it is desirable to ensure that the transistors of the circuit illustrated in Figure 2 do not fail if the low voltage power supply fails but the high voltage power supply is operational. In such a case, five volts may be applied at Vdd2, but Vdd will be zero volts, causing transistors such as 214 to potentially see a drain to source voltage of
25 nearly five volts in operation.

To address this, some embodiments of the invention implement a circuit or method that provides as Vdd inputs to transistors such as 214 the greater voltage level of either the low voltage supply or Vref, where Vref is derived from the high voltage supply. Such a system can be easily implemented onto the integrated circuit die, and
30 effectively allows the integrated circuit to function without suffering damage should the low voltage supply fail or be disconnected.

The invention described here provides a high-voltage output buffer implemented in a low-voltage semiconductor process, enabling low-voltage semiconductors to interface with high-voltage circuitry. The buffer comprises a level translator circuit that in operation receives a signal varying between ground and a low voltage level, and
5 outputs a corresponding signal varying between a reference voltage level and a high voltage level. The reference voltage level is an intermediate voltage level between half of the low voltage level and the high voltage level. The buffer also comprises an output circuit that in operation receives the output of the level translator circuit, and outputs a corresponding high voltage level when the input is a high voltage level or a zero voltage level when the input is at the reference voltage level. The low voltage supply in some embodiments of the invention is derived from the greater of an external low voltage supply or the reference voltage derived from the high voltage supply, so that the transistors of the buffer are protected from high voltages in the event of an external low voltage supply failure.

15 Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the invention. It is intended that this invention be limited only by the claims, and the full
20 scope of equivalents thereof.

Claims

We claim:

1. A high-voltage output buffer implemented in a low-voltage semiconductor process,
5 comprising:
a level translator circuit, the level translator operable to receive a signal varying between ground and a low voltage level, and to output a corresponding signal varying between a reference voltage level and a high voltage level, where the reference voltage level is an intermediate voltage level between half of the low voltage level and the high
10 voltage level; and
an output circuit, the output circuit operable to receive via an input the output of the level translator circuit, and to output a high voltage level when the input is a high voltage level or a zero voltage level when the input is at the reference voltage level.
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2. The high-voltage output buffer of claim 1, wherein the high voltage level is five volts and the low voltage level is 3.3 volts.
3. The high-voltage output buffer of claim 1, wherein the low-voltage semiconductor
20 process is a 3.3 volt semiconductor process.
4. The high-voltage output buffer of claim 1, wherein the buffer is further operable as a low-voltage buffer when the high voltage level is changed to the low voltage level.
- 25 5. A high-voltage output buffer implemented in a low-voltage semiconductor process, comprising:
a level translator circuit, the level translator operable to receive a circuit input signal varying between ground and a low voltage level, and to output a corresponding signal varying between a reference voltage level and a high voltage level, where the
30 reference voltage level is an intermediate voltage level between half of the low voltage level and the high voltage level; and

(Claim 5 continued)

an output circuit comprising:

5 a first PMOS transistor coupled between a high voltage and a second PMOS transistor, the gate of the first PMOS transistor coupled to the output of the level translator circuit;

a second PMOS transistor coupled between the first PMOS transistor and a first NMOS transistor, the gate of the second PMOS transistor coupled to receive the reference voltage;

10 a first NMOS transistor coupled between the second PMOS transistor and the second NMOS transistor, the gate of the first NMOS transistor coupled to receive the low voltage;

a second NMOS transistor coupled between the first NMOS transistor and ground, the gate of the second NMOS transistor connected to receive the level translator circuit input.

15 an output coupled to the connection between the second PMOS transistor and the first NMOS transistor.

20 6. The high voltage output buffer of claim 5, wherein the high voltage level is five volts and the low voltage level is 3.3 volts.

7. The high voltage output buffer of claim 5, wherein the low-voltage semiconductor process is a 3.3 volt process.

25 8. The high voltage output buffer of claim 5, wherein the buffer is further operable as a low-voltage buffer when the high voltage level is changed to the low voltage level.

9. A high-voltage output buffer implemented in a low-voltage semiconductor process, comprising:

30 a first PMOS transistor connected between a high voltage source and second PMOS transistor, the gate of the first PMOS transistor connected to a connection

(Claim 9 continued)

between a third PMOS transistor and a fourth PMOS transistor,

5 a second PMOS transistor connected between the first PMOS transistor and a first NMOS transistor, the gate of the second PMOS transistor coupled to a reference voltage that is approximately half of a low voltage level;

a first NMOS transistor coupled between the second PMOS transistor and a second NMOS transistor, the gate of the first NMOS transistor coupled to the low voltage level;

10 a second NMOS transistor coupled between the first NMOS transistor and ground; the gate of the second NMOS transistor coupled to receive an input;

a third PMOS transistor coupled between a high voltage source and a fourth PMOS transistor, the gate of the third PMOS transistor coupled to the connection between the first PMOS transistor and the second PMOS transistor;

15 a fourth PMOS transistor coupled between the third PMOS transistor and a third NMOS transistor, the gate of the fourth PMOS transistor coupled to the reference voltage;

a third NMOS transistor coupled between the fourth PMOS transistor and a fourth NMOS transistor, the gate of the third NMOS transistor coupled to the low voltage level;

20 a fourth NMOS transistor coupled between the third NMOS transistor and ground, the gate of the fourth NMOS transistor coupled to receive an inverted input signal;

a fifth PMOS transistor coupled between a high voltage and a sixth PMOS transistor, the gate of the fifth PMOS transistor coupled to the connection between the first PMOS transistor and the second PMOS transistor;

25 a sixth PMOS transistor coupled between the fifth PMOS transistor and a fifth NMOS transistor, the gate of the sixth PMOS transistor coupled to receive the reference voltage;

30 a fifth NMOS transistor coupled between the sixth PMOS transistor and the sixth NMOS transistor, the gate of the fifth NMOS transistor coupled to receive the low

(Claim 9 continued)

voltage;

5 a sixth NMOS transistor coupled between the fifth NMOS transistor and ground,
the gate of the sixth NMOS transistor connected to receive the input.

an output coupled to the connection between the sixth PMOS transistor and the
fifth NMOS transistor.

10 10. The output buffer of claim 9, wherein the semiconductor process is a 3.3 volt
semiconductor process.

11. The high-voltage output buffer of claim 9, wherein the high voltage level is five
volts and the low voltage level is 3.3 volts.

15 12. The high-voltage output buffer of claim 9, wherein the buffer is further operable as
a low-voltage buffer when the high voltage level is changed to the low voltage level.

13. A method of providing a high-voltage output from a circuit implemented in a low-
voltage semiconductor process, comprising:

20 receiving in a level translator circuit a signal varying between ground and a low
voltage level;

outputting from the level translator circuit a corresponding signal varying
between a reference voltage level and a high voltage level, where the reference voltage
level is an intermediate voltage level between half of the low voltage level and the high
25 voltage level;

receiving in an output circuit the output of the level translator circuit; and

outputting from the output circuit a high voltage level when the output circuit
input is a high voltage level or a zero voltage level when the input is at the reference
voltage level.

14. The method of claim 13, wherein the high voltage level is five volts and the low voltage level is 3.3 volts.

5 15. The method of claim 13, wherein the low-voltage semiconductor process is a 3.3 volt semiconductor process.

16. The method of claim 13, wherein the method is further operable as a low-voltage buffer when the high voltage level is changed to the low voltage level.

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