ABSTRACT

A METHOD TO FABRICATE DUAL-METAL GATE FOR N- AND P-FETS

A new method for forming a dual-metal gate CMOS transistors is described. An NMOS and a PMOS active area of a semiconductor substrate are separated by isolation regions. A nitride layer is deposited overlying a gate dielectric layer and patterned to form a first dummy gate in each of the active areas. First ions are implanted to form source/drain regions in each of the active areas not covered by the first dummy gates. The first dummy gates are isotropically etched to form second dummy gates thinner than the first dummy gates. Second ions are implanted to form lightly doped source/drain regions in each of the active areas not covered by the second dummy gates. Dielectric spacers are formed on sidewalls of the second dummy gates and the source/drain regions are silicided. The second dummy gates and spacers are removed. A first metal layer is deposited overlying the substrate and patterned to form a first metal gate in one of the NMOS and PMOS active areas. An oxide layer is deposited overlying the substrate and the first metal gate. The oxide layer is polished back to the metal gate. A via is opened through the oxide layer to the substrate in the other one of said NMOS and PMOS areas. A second metal layer is deposited within the via opening and polished back to the oxide layer to form a second metal gate in the other one of the NMOS and PMOS area to complete formation of dual-metal CMOS gates.

FIGURE 16