

ABSTRACT

An IC tester is provided which is capable of automatically testing the memory sections and the logic sections successively of a composite IC. A memory testing test head 104A and a logic testing test head 104B are disposed in the path of movement of a test tray TST, the arrangement being such that both the memory section and the logic section of each of ICs to be tested loaded on the test tray are successively tested by bringing each IC into electrical contact with sockets mounted on the respective test heads while the ICs are placed on the same test tray. Preferably, the memory section of each IC is first tested by the memory testing test head and thereafter the logic section thereof is tested by the logic testing test head.

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This Sheet Has Been Replaced

