Referring now to FIG. 12, therein is shown the structure of FIG. 11 after removal of the leadframe tape 800 of FIG. 11 and singulation into the integrated circuit package system 100.

Referring now to FIG. 13, therein is shown a cross-sectional view of an integrated circuit package system 1300 in a second embodiment of the present invention. The integrated circuit package system 1300 includes the semiconductor chip 102 over the leadfingers 108.

The semiconductor chip 102 has the stress-relieving layer 104 and adhesion layer portions 1302 of the adhesion layer 106, which are adjacent the diced sides 1306 of the semiconductor chip 102. The adhesion layer portions 1302 are selectively formed on the stress-relieving layer 104 just over the leadfingers 108 in such a manner as to avoid wafer warping by providing minimal material for CTE mismatch to occur.

The semiconductor chip 102 is connected to the leadfingers 108 by bond wires 110 and is encapsulated in an encapsulant 1304.

Referring now to FIG. 14, therein is shown a cross-sectional view of an integrated circuit package system 1400 in a third embodiment of the present invention. The integrated circuit package system 1400 includes the semiconductor chip 102 and the stress-relieving layer 104.

Under the stress-relieving layer 104 is an extra thick adhesion layer 1402. The adhesion layer 1402 is thick enough to form over the sides of the leadfingers 108. The adhesion layer 1402, in addition to bonding to the top of the leadfingers 108, also bonds on the sides of the leadfingers 108 to effectively cover the leadfingers 108. This provides a lead-locking function for the leadfingers and eliminates the problem of bouncing leadfingers during wire bonding.

The semiconductor chip 102 is wire bonded by bond wires 110 to the leadfingers 108 and the structure is encapsulated in an encapsulant 1404.

Referring now to FIG. 15, therein is shown a cross-sectional view of an integrated circuit package system 1500 in a fourth embodiment of the present invention. The integrated circuit package system 1500 includes the semiconductor chip 102, the stress-relieving layer 104, and the adhesion layer 106.

Under the adhesion layer 106 is an additional stress-relieving layer 1502. The additional stress-relieving layer 1502 is between and in direct contact with the leadfingers 108. The additional stress-relieving layer 1502 helps to further eliminate wafer warping.

What is claimed is:

1. An integrated circuit package system comprising:

a semiconductor chip;

a stress-relieving layer on the semiconductor chip;

an adhesion layer on the stress relieving layer; ~~and~~

electrical interconnects bonded to the adhesion layer; and~~layer.~~

an additional stress-relieving layer on the adhesion layer and attached between the electrical interconnects.

2. The system as claimed in claim 1 wherein:

the adhesion layer is on selected regions of the stress-relieving layer adjacent the diced sides of the semiconductor chip; and

the semiconductor chip is mounted by the adhesion layer on the electrical interconnects.

3. The system as claimed in claim 1 wherein:

the adhesion layer is thicker than the stress-relieving layer; and

the adhesion layer on the electrical interconnects and over the sides thereof.

4. The system as claimed in claim 1 wherein:~~further comprising:~~

~~an additional stress-relieving layer on the adhesion layer and~~ the additional stress-relieving layer holds the semiconductor chip ~~on~~over the electrical interconnects.

5. The system as claimed in claim 1 further comprising:

bond wires electrically connecting the semiconductor chip to the electrical interconnects; and

an encapsulant encapsulating the semiconductor chip, the bond wires, and the electrical interconnects.

6. The system as claimed in claim 1 wherein:

the stress-relieving layer is a low modulus stress-relieving layer;

the adhesion layer is a high modulus adhesion layer;

the low modulus stress-relieving layer and the high modulus adhesion layer are fully cured; and

the electrical interconnects are leadfingers.

7. The system as claimed in claim 6 wherein:

the high modulus adhesion layer is on selected regions of the low modulus stress-relieving layer adjacent the diced sides of the semiconductor chip; and

the semiconductor chip is mounted by the high modulus adhesion layer on the leadfingers.

8. The system as claimed in claim 6 wherein:

the high modulus adhesion layer is thicker than the low modulus stress-relieving layer; and

the high modulus adhesion layer on the leadfingers and over the sides thereof.

9. The system as claimed in claim 6 wherein:~~further comprising:~~

~~an additional low modulus stress-relieving layer on the high modulus adhesion layer and~~ the additional ~~low modulus~~ stress-relieving layer holds the semiconductor chip on the leadfingers.

10. The system as claimed in claim 6 further comprising:

bond wires electrically connecting the semiconductor chip to the leadfingers; and

an encapsulant encapsulating the semiconductor chip, the bond wires, and the leadfingers.