IMPROVED FUSE PROCESS USING LASER EXPOSURE OF FUSE RESIST

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention pertains to manufacturing integrated circuits and more particularly to isolating defective portions of integrated circuits to increase output of integrated circuit wafers.

Related Prior Art

Integrated circuit wafers are manufactured with extra or spare memory circuits to allow for a small percentage of manufacturing defects. The circuits are tested to determine whether any of the "first choice" circuits are defective. Defective circuits are then replaced by functioning "back up" circuits, which would have been extra if all "first choice" circuits were non-defective.

Once testing was complete, defective circuits would be cut out, and then logic associated with this part of the circuit will replace the failed memory cells with the "back up" cells.

Using standard techniques, a polycrystalline silicon line is exploded with a laser beam. The appropriate wavelength is used to heat the silicon and cause an explosion, or semi-explosion which melts or vaporizes the silicon and opens up the line.

Prior art uses polysilicon. To remove a defective memory cell the poly line lead is heated and gets so hot it will vaporize. Any remainder silicon reacts with the ambient and becomes silicon dioxide. Silicon dioxide in this process is non-conductive. If this same kind of process

is performed using a laser to heat aluminum, an aluminum oxide is formed and this is semi-conductive. It is a conductive ceramic which can never really be etched out by being burnt by a laser. Conductive ceramic does not make for a perfect high resistance path, as there is always a little bit of current leakage or potential leakage.

If laser burning is not used, the use of poly fuses with multilevel metalization requires a great deal of oxide etch in order to clear the required oxide off of the polysilicon fuses. The oxide can be on the order of four or five microns thick for a four level metal device. This requires very complex etch processes in order to overcome this problem, including the addition of patterning steps. This also requires increased area due to the pattern and etch bias required to perform such an etch.

The process just described is sufficient if the thickness of the oxide is less than one to two microns. The problem with this process is when multiple level metalization is patterned from putting four or more layers of metal on the circuit. Such patterning results in a large amount of oxide over the poly fuses. The design process would utilize the top level of metalization to make the fuse.

Referring to Figure 1, a simplified side view of an integrated circuit 10 done by a prior art process is illustrated. For the prior art process, a polysilicon line is a fuse link 12 and is near the crystal silicon surface 14, fairly deep below wafer surface 16. The process flow results in the line being covered by thick insulation oxide layers 18. For every level of metal that is put on, another 10,000 angstroms or 1 micron of oxide buildup is added. In this process, a mask is provided and a hole 20 (Figure 2) is created over every fuse. A timed etch is performed and a

significant amount of oxide layer 18 is etched out. Normally a wet etch or a plasma etch is used. All fuse links are uncovered because this pattern is put on before all the circuits are tested. As the process flow proceeds, the metal bond pads are opened up during this particular etch, as illustrated. The circuit can be electrically tested and which fuse needs to be blown can be determined.

Figure 2 illustrates a side view of integrated circuit 10 after a timed etch is done and oxide layer 18 is etched until every polysilicon fuse link 12 is almost exposed at 20. Oxide layer 18 over every fuse link 12 on the whole wafer is etched. A problem may occur when there are four or more levels of metal. The thickness of oxide layer 18 is on the order of five to ten microns, so this etch is actually very hard, if not impossible, to control.

In producing an integrated circuit, pattern definition and circuit etching is done at several levels, some levels containing metal as circuit components. When a repair is to be done, a laser beam is used to open up the particular fuses that are desired. However, when a metal link is used, the laser beam may leave a metal slag associated with typical high energy laser ablation-type fuses that is semi-conductive.

SUMMARY OF THE INVENTION

In the process of the present invention, there are formed holes only over the fuses that need to be cut. Fuses that do not need to be cut do not have a hole created over them.

The present invention combines the use of metal fuses and the laser repair system to pattern the needed fuse openings. This eliminates the conventional style patterning of all of the fuses and the ensuing difficulty

in control of the resulting fuse oxide etch over only the required areas for fuse opening. This also will allow a tighter packing density of the fuses on an integrated circuit since there is no slag produced during the laser exposure, and the laser spot size can be easily controlled to at least a two micron spot size.

The present invention provides a method for isolating defective circuits on an integrated circuit having a base layer with a covered conductor, preferably SiO_2, connecting link to the defective circuit, all covered with a photoresist. This method includes selectively exposing the photoresist covering the conduction link to light and dissolving the exposed photoresist with a developer solution which dissolves the exposed photoresist. The covered conductor in dissolved or etched with a second predetermined solution. The dissolved covered conductor is flushed away to remove the conduction path to the defective circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a sectional view illustrating a circuit manufactured by a process of prior art.

Figure 2 is a sectional view illustrating a circuit isolation process by fuse interrupt of prior art.

Figures 3A-3E are sectional views illustrating the circuit isolation process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides a solution to the problem of defective circuit isolation that allows the combination of the laser repair process and the fuse patterning into one step. In producing an integrated

circuit, pattern definition and circuit etching are done at several levels, some levels containing metal as circuit components. After pattern definition and etching of the top level metal, the typical suppression oxide is deposited. A pattern and etch is used to expose the bonding pads of the chip for testing. After testing, the wafers are coated with a photosensitive resist. A laser is used to expose photoresist in order to expose a fuse. Depending on where a defect is in the circuit, various fuses are etched to disconnect certain parts of the circuit and to connect other parts. An etching process is used to cut the metal fuses which eliminates any metal slag associated with typical high energy laser ablation-type fuses. In reality, an integrated circuit is being repaired by this process.

As stated previously, in producing an integrated circuit, pattern definition and circuit etching are done at several levels, some levels containing metal as circuit components. The process of the present invention is described as a one level device for simplicity and includes the following steps.

Referring now to Figures 3A-3E, the process of the present invention is illustrated. Step one, illustrated in Figure 3A, in the making of a wafer, an aluminum lead 30 is placed on an insulating layer or base 32. A metal line on the order of one to two microns wide is placed on the insulating base (one micron equals 10^{-8}cm.).

In step two, as illustrated in Figure 3B, a silicon dioxide or similar insulating layer 34 is added over lead 30. Insulating layer 34 is typically plasma enhanced chemical vapor deposition. In the preferred embodiment insulating layer 34 is silicon dioxide, however, any similar insulating material currently in use in the art is acceptable. Additional insulating layers 34 may be deposited over metal lead 30 which are also, preferably, a silicon dioxide based layer.

Step three is illustrated in Figure 3C where an organic polymer called a photoresist 36 is uniformly spun on aluminum lead 30 covered with insulating layer 34 with plasma enhanced chemical vapor deposition. In the present invention, the resist is a photosensitive polymer material that is spun on wafer. Photoresist 36 is spun on over the entire face of wafer so that the entire surface is covered. A centralized quantity of the photoresist material is put on wafer, wafer is spun at high speed, and photoresist 36 is thinly coated over the entire wafer. When wafer is coated, a laser system 40 is used to expose the photosensitive resist over the fuses that need to be cut.

In step four, illustrated in Figure 3D, laser system 40 exposes photoresist 36 to make it solvent soluble which then creates a pattern. The photosensitive polymer is comprised of an organic resin with a photoactive compound. Exposure to the laser beam causes a chemical reaction in the exposed area to promote its solubility to a developer. After the exposure, the resist is developed.

With photoresist 36, which is actually light sensitive, the area over lead 30 to be removed is exposed with a laser beam of the appropriate wavelength. In the preferred embodiment, photoresist 36 is typically 436 nanometers sensitive or 365 nanometers sensitive. Laser system 40 is not required to have its peak energy at either of these two wavelengths but a laser that produces enough energy in either one of these wavelengths is sufficient. Any type of laser that is currently in use in the art may be used as long as it is sufficient to promote the reaction of the photoactive compound within the resist material.

Through this process, photoresist 36 is exposed and developed. The

result of this process is leaving an opening 42 over metal lead 30. Basically, a square is exposed, leaving an area in photoresist 36 to be developed out. The light actually breaks the bonds in photoresist 36 and makes a portion of photoresist 36 soluble to a predetermined solvent. Then the portion that has been exposed to the proper wavelength light can be rinsed away. After this process, oxide insulating layer 34 over metal lead 30 remains, leaving a mask with opening 42.

In step five, as illustrated in Figure 3E, the pattern is etched with either a chemical or a plasma etch. A conventional etch is then used to etch both oxide insulating layer 34 and metal lead 30. When the etching is done, the etch does not etch the polymer material of photoresist 36. The polymer blocks are etch everywhere except at the exposed and developed locations. This produces a very high resistance open circuit with no slag produced that could still cause shorting or deposit in unwanted areas on the chip. This results in a hole that, with everything etched away, leaves an open circuit to the defective memory or other circuit. In the preferred embodiment a plasma etch is performed to etch both oxide insulating layer 34 and metal lead 30. This etch can be a plasma etch or a wet etch. Any etching type chemistry may be used as long as it etches both oxide insulating layer 34 and metal lead 30. The end product includes photoresist 36 on an oxide or insulating layer 34 with metal lead 30 cut out in an opening 42. Either a wet etch or a reactive ion etch has been done to remove this material. Typically, removing metal lead 30 connecting a memory circuit removes the conduction path to the memory circuit. A nice clean cut of metal lead 30 has been made using the process of the present invention.

While there has been illustrated and described a particular embodiment of the present invention, it will be appreciated that numerous

changes and modifications will occur to those skilled in the art, and it is intended in the appended claims to cover all those changes and modifications which fall within the true spirit and scope of the present invention.

CLAIMS

1. A method for isolating defective circuits on an integrated circuit comprising the steps of:

providing a base layer having an insulating layer covered conductor connection to a defective circuit, said base layer, conductor and insulating layer being covered with a photoresist material;

directing a laser beam over a predetermined portion of the photoresist to selectively expose a portion of said photoresist material covering said conductor to high energy light while simultaneously avoiding generation of slag at the conductor;

developing said exposed photoresist material with a predetermined solution to wash away said exposed photoresist material; and

dissolving said insulating layer covered conductor with a predetermined chemical reaction to remove a conduction path to said defective circuit and provide an opening in said photoresist that is substantially free of metal slag.

2. The method according to claim 1 wherein said dissolving step includes a wet etch process.

3. The method according to claim 1 wherein said dissolving step includes a dry etch process.

4. The method according to claim 1 wherein said laser light has a wavelength of about 436 nanometers.

5. The method according to claim 1 wherein said laser light has a wavelength of about 365 nanometers.

6. A method for isolating defective circuits on an integrated circuit having a base layer with an insulating layer covered conductor connection to the defective circuit, all covered with a photoresist material, said method comprising the steps of:

selectively exposing said photoresist material covering said conductor to light by subjecting said photoresist material covering to laser light with a wavelength of 436 nanometers;

developing said exposed photoresist material with a predetermined solution to wash away said exposed photoresist material;

dissolving said insulating layer covered conductor with a wet etch process to remove a conduction path to said defective circuit.

7. The method according to claim 1, wherein said laser beam is focused to a maximum width of about 2μm.

8. The method according to claim 6, wherein said laser beam is operable to expose the predetermined portion of the photoresist without generating an appreciable amount of metal slag at the conductor.