METRIC CIRCUIT AND METHOD FOR USE IN A VITERBI DETECTOR

ABSTRACT OF THE DISCLOSURE

A metric circuit (53) and method for use in a viterbi detector (54) are provided. The metric circuit (53) provides a transition signal (56) to a trellis block (55) during a first period and a second period. The transition signal (56) includes a negative transition signal and a positive transition signal. The metric circuit (53) includes a first adder circuit (70), a second adder circuit (72), a first comparator (74), a second comparator (76), an odd sample/hold circuit (80), and an even sample/hold circuit (82). The metric circuit (53) receives a discrete signal and a threshold value at the first adder circuit (70) and the second adder circuit (72). The first adder circuit (70) generates a first sum and the second adder circuit (72) generates a second sum. The first comparator (74) compares the first sum to an odd metric value, stored in the odd sample/hold circuit (80), during the first period, and compares the first sum to an even metric value, stored in the even sample/hold circuit (82), during the second period. The second comparator (76) compares the second sum to the odd metric value during the first period, and compares the second sum to the even metric value during the second period. The value of the odd metric value and the even metric value are replaced with either the first sum or the second sum only when specified conditions are met.

Figure 2