

"IMPROVEMENT TO DYNAMIC MOS-LOGIC IN INTERLACE-TECHNIQUE"

The invention relates to an integrated digital circuit arrangement with MOS field-effect transistors.

5 A known circuit arrangement comprises a combinatorial circuit for applying a logic operation to a plurality of input signals, which combinatorial circuit comprises a plurality of "sticks", each stick comprising a pre-charging transistor, a sampling transistor and at least one logic function transistor, there being provided means for applying said input signals as well as an output, which is coupled to a first node of the arrangement, whose potential at a specific instant
10 is representative of the result of the logic operation and depends on whether the capacitance of the first node is charged or not.

Such a circuit arrangement is known and is employed in the integrated Philips circuits SAB 3022B, SAB 3032D. These devices employ an N-MOS circuit in dynamic two-phase technique, which
15 operates as follows:

A buffer circuit, which is clocked by non-overlapping clock signals, transfers the logic information from a node of the combinatorial circuit to an output with a delay of one clock period. For a reliable transfer of information it is important that this node
20 is already at a specific potential when it receives said information. In other words, the node should be charged at the instant that the information arrives there. If a logic "1" is to be transferred via the node, this node is isolated after being pre-charged until the potential (which in this case remains high) is sampled for further
25 information transfer. If a logic "0" is to be transferred the node is discharged to a low potential via one or more sticks of the combinatorial circuit, after which this potential is sampled.

It is found that when such a circuit arrangement is used the frequency of the clock signals is limited because pre-charging
30 and especially discharging of the node takes too much time. This

is because numerous sticks of the combinatorial circuit are connected to the node, so that the capacitance of this node is substantial, whilst for example under specific circumstances discharging via only one stick should be possible. It should be borne in mind that one
5 such stick when conducting still represents a significant resistance, which has an adverse effect on the discharge time. Said resistance can only be reduced by use of larger transistors, which is not desirable in view of the required substrate area.

It is the object of the invention to provide an integrated digital
10 circuit arrangement which enables a higher information processing speed and in consequence means that faster clock signals can be used.

According to the present invention there is provided an integrated digital circuit arrangement with MOS field-effect transistors of the same conductivity type, which arrangement comprises a combinatorial
15 circuit for applying a logic operation to a plurality of input signals, which combinatorial circuit comprises a plurality of "sticks", each stick comprising a pre-charging transistor, whose gate is coupled to a source of pre-charging clock signals, a sampling transistor whose gate is coupled to a source of sampling clock signals of the same frequency
20 as, but different phase relative to, the pre-charging clock signals, and at least one logic function transistor to the gate of which one of the input signals is applied in use, each stick having an output on which at a specific instant determined by the sampling clock signal an output signal is produced representative of the logic operation of that
25 stick, and each stick having a transfer-gate transistor whose gate is connected to the output of its associated stick, the source-drain paths of the transfer-gate transistors being connected in series between a node and a voltage reference point, the output of the combinatorial circuit being dependent on whether the capacitance of the node is
30 charged or not.

An advantage of the circuit arrangement in accordance with the invention is that instead of the customary clock frequencies of about 50 kHz it is now possible to employ clock frequencies of approximately 500 kHz, which means that the circuit operates ten times as fast.
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The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows an embodiment of the invention, and

5 Figure 2 represents the clock signals required for a correct operation of the circuit arrangement of Figure 1.

The circuit arrangement of Figure 1 comprises enhancement-type insulated-gate field-effect transistors, such as the transistors TA, TB, TC, T₂, T₄, T₆, T₇ and T₉ to T₁₅ and similar transistors of the depletion type, such as the transistors
10 T₁, T₃, T₅ and T₈.

The supply voltage is designated UB and is for example +5 V. There is a common reference potential, which is represented in the drawing by the customary earth symbol.

Two clock signals, shown in Figures 2a and 2b, control
15 the circuit. These two clock signals are designated Ø1 and Ø2. The clock signals vary between the logic "0" level and the logic "1" level, the logic "1" level for example corresponding to a voltage of +4 V and the logic "0" level to a voltage of 0 V.

The circuit arrangement mainly comprises three sections:
20 one section is the customary buffer circuit, comprising transistors T₂ to T₉. In the prior-art versions problems occurred at the first node D of the circuit, because for taking over information from the combinatorial circuit said node had to be pre-charged and, as the case may be, discharged rapidly, while in the same
25 way as in the embodiment in accordance with the invention the clock signal Ø2 was the pre-charging clock signal and the clock signal Ø1 the sampling clock signal.

The second section is the combinatorial circuit, which in this case comprises 3 sticks. The sticks include the sampling
30 transistors TA, TB and TC, which are clocked by the clock signal Ø1. The sticks further comprise other enhancement transistors whose gate electrodes are connected to the input terminals A1, A2, A3, B1, B2, B3, C1, C2 and C3, via which the input information is applied. The result of the logic operation realized by the combinatorial
35 circuit is available on the respective outputs Q and QN of the buffer circuit.

In order to enable a rapid pre-charging and discharging of the node D of the circuit arrangement and thus the use of a higher clock frequency, seven additional transistors are included in the combinatorial circuit of the embodiment of the invention shown in Figure 1, which additional transistors constitute the third section of the circuit arrangement.

These additional transistors include the pre-charging transistors T10, T11 and T12, whose gate electrodes are connected to the clock line $\phi 2$, so that when $\phi 2$ is at logic "1" level, nodes DA, DB, DC of the circuit are charged, and further the transfer-gate transistors T13, T14 and T15, which provide an isolation between the individual sticks, transistor T₁ being arranged as a load transistor. If, for example, a logic "0" from stick A has to be transferred, node DA of the circuit arrangement should be discharged rapidly. If the sticks A, B and C were all connected directly to node D of the circuit, not only node A but also the nodes DB and DC, would have to be discharged, which obviously takes time. The inclusion of transistors T1, T13, T14 and T15 enables the nodes DA, DB and DC to be discharged individually. This can be done much faster, because in this case only the capacitance of one node is to be discharged via the associated stick.

The operation of such an N-MOS circuit, using the so-called dynamic two-phase technique, is as follows:

A buffer circuit, which is clocked by clock signals $\phi 1$ and $\phi 2$, which do not overlap each other in time, transfers the potential of the node D (logic level "1" or "0") to the output Q or the inverted output QN via transistors T2 and T7 with a delay of one clock period T. The potential of the node D in the circuit arrangement in accordance with the invention is determined by the potentials of the nodes DA, DB and DC of the individual sticks. Since the sticks are isolated from each other, nodes DA, DB and DC are each charged separately via the associated pre-charging transistor during the time that $\phi 2$ is "high".

Depending on the information applied to the input terminals

A1, A2, A3, B1, B2, B3, C1, C2 and C3 one or more of the sticks A, B and C can be turned on, so that during the time that ϕ_1 is high and transistors TA, TB, and TC conduct the charge of the node(s) associated with the conductive stick(s) is drained.

5 The embodiment for the sticks A, B and C of the combinatorial circuit shown in the drawing is merely an example. It can be adapted to suit the function to be realized.

By discharging one or more of the nodes DA, DB or DC via the associated stick(s) the connected gate electrode of the
10 relevant transistor(s), namely T13, T14 and T15 respectively, assumes the logic "0" level, so that the relevant transistor(s) T13, T14 and/or T15 is (are) turned off and transistor T1 can consequently charge the node D rapidly to logic "1" potential. Since transistor T2 conducts during the sampling phase, that is
15 when the clock signal ϕ_1 is at logic "1" level, the level on the node D of the arrangement also appears on the gate of the transistor T4, where it is also maintained if at the end of the sampling phase transistor T2 is turned off again.

The other transistors T3, T5, T6, T9 and T7 are included
20 in a circuit which is commonly used and known as a buffer circuit. Furthermore, it is to be noted that by the inclusion of the transistors T13, T14, T15 and the load transistor T1 the signal on the node D is inverted in comparison with logic circuits known so far, so that in this way a signal inversion is obtained.

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CLAIMS:

1. An integrated digital circuit arrangement with MOS field-effect transistors of the same conductivity type, which arrangement comprises a combinatorial circuit for applying a logic operation to a plurality of input signals, which combinatorial circuit comprises
5 a plurality of "sticks", each stick comprising a pre-charging transistor, whose gate is coupled to a source of pre-charging clock signals, a sampling transistor whose gate is coupled to a source of sampling clock signals of the same frequency as, but different phase relative to, the pre-charging clock signals, and at least one logic
10 function transistor to the gate of which one of the input signals is applied in use, each stick having an output on which at a specific instant determined by the sampling clock signal an output signal is produced representative of the logic operation of that stick, and each stick having a transfer-gate transistor whose gate is
15 connected to the output of its associated stick, the source-drain paths of the transfer-gate transistors being connected in series between a node and a voltage reference point, the output of the combinatorial circuit being dependent on whether the capacitance of the node is charged or not.
- 20 2. A circuit arrangement as claimed in claim 1, wherein the node is coupled to a supply voltage source by a depletion load transistor.
3. A circuit arrangement as claimed in claim 1 or 2, wherein the transistors of each stick and the transfer-gate transistors are enhancement transistors.
- 25 4. An integrated digital circuit arrangement with MOS field-effect transistors, constructed and arranged to operate substantially as hereinbefore described with reference to the accompanying drawings.

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