

**FEFET STRUCTURES USING AMORPHOUS OXIDE SEMICONDUCTOR
CHANNELS ON INTEGRATED CIRCUITS****CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/518,988, filed on August 11, 2023, entitled "INTEGRATED CIRCUIT HAVING MEMORIES AND A SHARED WRITE PORT", identified by Docket Number P23-133-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0002] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/602,733, filed on November 27, 2023, entitled "METHOD AND SYSTEM FOR KNOWN-GOOD-DIE TESTABILITY OF FACE-TO-FACE BONDED CHIPLETS", the entire contents of which is incorporated herein by reference in its entirety.

[0003] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/602,737, filed on November 27, 2023, entitled "SYSTEM AND METHOD FOR HAVING CORRECT-BY-CONSTRUCTION TIMING CLOSURE", the entire contents of which is incorporated herein by reference in its entirety.

[0004] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/567,649, filed on March 20, 2024, entitled "ASSEMBLY HAVING A FACE-TO-FACE BONDED CHIPLET", identified by Docket Number P24-052-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0005] The present application claims the benefit and priority to U.S. Provisional Patent Application No. 63/637,742, filed on April 23, 2024, entitled "INTEGRATED CIRCUIT HAVING MICROVAULT MEMORIES", identified by Docket Number P24-081-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0006] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/637,764, filed on April 23, 2024, entitled "FEFET STRUCTURES ON INTEGRATED CIRCUITS", identified by Docket Number P24-082-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0007] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/674,471, filed on July 23, 2024, entitled "SYSTEM, METHOD, AND APPARATUS FOR WAFER-SCALE MEMORY", identified by Docket Number P24-135-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

BACKGROUND*Relevant Field*

[0008] The present disclosure relates to integrated circuits. More particularly, the present disclosure relates to integrated circuits having FeFETs for storing memory.

Description of Related Art

[0009] Chiplets refer to miniature chips that are designed to work as a single entity while using advanced packaging technology. These miniaturized chips are created by dividing the larger chip into several smaller chips, each with its own function or capability. The concept originated from the semiconductor industry's need to overcome the physical restrictions of traditional monolithic chip designs and achieve higher levels of integration. The idea behind chiplets is to create a modular system of interconnected and interchangeable chips that can be combined in different configurations to create advanced computing systems with improved performance, power efficiency, and functionality.

[0010] Chiplets can be based on different architectures, such as CPU, GPU, memory, or IO, and can be assembled and stacked in a variety of ways, depending on the specific application requirements. One of the advantages of the chiplet approach is the ability to mix and match different chiplets from different manufacturers to create custom solutions that meet specific computing needs. This approach also allows for faster time to market, reduced development costs, and increased flexibility, as chiplets can be upgraded or replaced without the need for a complete system redesign.

[0011] The use of chiplets may be used in various industries, including consumer electronics, cloud computing, and data centers, where the demand for high-performance computing and energy efficiency is high. Chiplets are expected to play a significant role in the future of computing and are likely to unlock new possibilities for creating more powerful and/or sophisticated electronic devices.

[0012] SUMMARY

[0013] An integrated circuit is disclosed herein that may be part of a semiconductor device. A method of manufacturing or a method of writing and reading data to modules are disclosed herein and can be used with all examples, embodiments, and aspects as described herein.

[0014] The integrated circuit may comprise a plurality of microvaults, with each of the microvaults disposed in a spaced relation relative to one another and adjacent to a first surface. The plurality of microvaults includes a first microvault. Additionally, the integrated circuit may comprise a plurality of bonding areas, with each bonding area disposed on the first surface and

adjacent to a respective one of the plurality of microvaults. The plurality of bonding areas includes a first bonding area in operative communication with the first microvault.

[0015] In some embodiments, the integrated circuit may comprise a first bonding area disposed on the first surface and adjacent to the first microvault. This first bonding area can optionally include a plurality of bonds, with each bond in operative communication with the first microvault.

[0016] In some embodiments, the first bonding area may include a plurality of bonds each in operative communication with the first microvault. Optionally, these plurality of bonds may be bumpless bonds.

[0017] In some embodiments, the integrated circuit may have a first microvault with a capacity between 4 kilobytes and 1 megabyte.

[0018] In some embodiments, the first microvault has a capacity between 4 kilobytes and 128 kilobytes.

[0019] In some embodiments, the microvaults may have a storage capacity ranging from 4 kilobytes to 16 kilobytes.

[0020] In some embodiments, the first microvault may have dimensions of less than 256 micrometers by less than 256 micrometers and extend in a vertical dimension a predetermined distance.

[0021] In some embodiments, the first microvault has dimensions of 32 micrometers by 32 micrometers and extends vertically a predetermined distance.

[0022] In some embodiments, the integrated circuit may involve the first microvault having a vertical dimension that corresponds to at least 8 memory layers. Specifically, in one embodiment, the first microvault as having dimensions of 32 micrometers by 32 micrometers, and extending in a vertical dimension a predetermined distance. This vertical dimension corresponds to at least 8 memory layers in some embodiments.

[0023] In some embodiments, the bit density of the first microvault may be greater than 0.2 Gigabits per square millimeter for each layer of the microvault.

[0024] In some embodiments, the plurality of microvaults, including the first microvault, may be disposed on a Back-End-Of-the-Line portion of a die.

[0025] Optionally, the integrated circuit embodiment can include an SRAM vault that is disposed adjacent to the first microvault.

[0026] The integrated circuit may comprise an SRAM vault disposed adjacent to the first microvault, wherein the first bonding area is in operative communication with the SRAM

vault. In some embodiments, the integrated circuit may include a second bonding area disposed on the first surface that is in operative communication with the SRAM vault.

[0027] In some embodiments, the integrated circuit may further comprise a second bonding area disposed on the first surface and in operative communication with the SRAM vault. The second bonding area enables connection and data transfer between the SRAM vault component and other components in the system.

[0028] In some embodiments, the integrated circuit may involve the plurality of microvaults being formed on a first die and the SRAM vault being formed on a second die, where the first and second dies are bonded together.

[0029] In some embodiments, the integrated circuit may further comprise a DRAM (dynamic random access memory) vault disposed adjacent to the microvault. The DRAM vault provides an additional memory storage area that can be utilized along with the microvault memory.

[0030] In some embodiments, the integrated circuit may involve a DRAM vault disposed adjacent to the plurality of microvaults. The first bonding area may be in operative communication with this DRAM vault to facilitate data transfers between the first microvault and the DRAM vault.

[0031] In some embodiments, the integrated circuit further comprises a second bonding area disposed on the first surface mentioned previously. This second bonding area is in operative communication with the DRAM vault also mentioned previously. Operative communication allows data and signals to be exchanged between the second bonding area and the DRAM vault.

[0032] In some embodiments, the integrated circuit may comprise a plurality of microvaults formed on a first die and a DRAM vault formed on a third die. The first and third dies may be rigidly fixed together.

[0033] In some embodiments, the integrated circuit further comprises a read address register operatively coupled to the first bonding area. The read address register may be configured to hold and communicate a read address to the first microvault.

[0034] In some embodiments, the integrated circuit further comprises a read data register. The read data register may be operatively coupled to the first microvault to receive and hold read data from the first microvault.

[0035] In some embodiments, the integrated circuit further comprises a read data register operatively coupled to the first microvault to receive and hold read data from the first

microvault. The read data register may be operatively coupled to the first bonding area to communicate the held read data thereto.

[0036] The integrated circuit may include a read data register that is operatively coupled to a second bonding area of the plurality of bonding areas to communicate read data thereto. In some embodiments, the read data register receives and holds read data from the first microvault and then communicates this read data to the second bonding area.

[0037] In some embodiments, the integrated circuit may further comprise a second read data register in operative communication with the first read data register. The second read data register may be configured to receive and hold read data from the first read data register.

[0038] The integrated circuit may involve a second read data register disposed on a die having a second face, wherein the second face includes a read data bonding area operatively coupled to the first bonding area of the first surface.

[0039] In some embodiments, the integrated circuit may further comprise a second read data register disposed on a die having a second face. This second read data register is configured to receive and hold read data from the first read data register. Optionally, this second face of the die includes a read data bonding area that is operatively coupled to the second bonding area of the first surface, in order to facilitate communication of data between the dies. Through this bonding, data can be transferred from the first read data register on the first die to the second read data register on the second die.

[0040] In some embodiments, the integrated circuit may further comprise a second read data register disposed on a different die than the die that has the plurality of microvaults.

[0041] In some embodiments, the integrated circuit further comprises a second read address register disposed on a different die than the die containing the plurality of microvaults. This additional read address register located on a separate die may be utilized for various purposes such as increasing storage capacity or bandwidth for reading data from the microvaults. By having multiple read address registers distributed across discrete dies, flexible architectures can be enabled to meet performance requirements while minimizing device footprint and power consumption.

[0042] In some embodiments, the integrated circuit further comprises a second read address register. The second read address register is configured to receive and hold a read address. Optionally, the second read address register communicates the read address to the first microvault.

[0043] The integrated circuit may further comprise a second bonding area disposed on a second surface, in addition to the read address register and second read address register. The

second bonding area provides an interface on the second surface to facilitate communication and data transfers related to the read addressing functions. By having this second bonding area, the integrated circuit enables interfacing the read addressing architecture across multiple surfaces and dies.

[0044] In some embodiments, the integrated circuit may further comprise a second read address register. The second read address register can be disposed on a second die having a second surface. The second read address register may be configured to receive and hold the read address. Additionally, the second read address register can communicate the read address to the read address register of the first die via the second surface, wherein the second surface of the second die and the first surface of the first die may be bonded together.

[0045] In some embodiments, the integrated circuit further comprises a second surface with a second read address register disposed on it. The second read address register is configured to receive and hold the read address and communicate the read address to the read address register of the first surface. Optionally, the second surface and the first surface may be bonded together to facilitate communication of the read address between the two surfaces.

[0046] In some embodiments, the integrated circuit further comprises a Through-Silicon Via operatively coupled to a third surface on a first end of the Through-Silicon Via, where the third surface is on an opposite side of the first surface.

[0047] In some embodiments, the integrated circuit further comprises an interconnect coupled to the first surface where the plurality of microvaults are disposed. This interconnect is also coupled to a second end of a Through-Silicon Via that facilitates communication between dies. The Through-Silicon Via has a first end coupled to a third surface on the opposite side of the first surface.

[0048] In some embodiments, the integrated circuit further comprises a second microvault that is in operative communication with the first bonding area.

[0049] In some embodiments, the integrated circuit may further comprise a multiplexer operatively coupled to the first microvault to receive a first read data therefrom. The multiplexer may also be operatively coupled to the second microvault to receive a second read data therefrom. The multiplexer can be configured to select between the first read data from the first microvault and the second read data from the second microvault for output.

[0050] In some embodiments, the integrated circuit further comprises a counter operatively coupled to the multiplexer. The counter is configured to control the multiplexer to serially read out the first read data from the first microvault and the second read data from the second microvault.

[0051] In some embodiments, the integrated circuit further comprises a read data register configured to receive the first read data from the first microvault or the second read data from the second microvault selected by the multiplexer. The read data register holds the received first read data or second read data therein.

[0052] In some embodiments, the integrated circuit further comprises a second bonding area on the first surface. The read data register is coupled to this second bonding area to communicate the held first read data or second read data from the multiplexer to the second bonding area.

[0053] In some embodiments, the integrated circuit further comprises an assembly including a first die having the plurality of microvaults.

[0054] In some embodiments, the integrated circuit further comprises an assembly including a first die that has the plurality of microvaults. This plurality of microvaults on the first die includes the first microvault and a second microvault.

[0055] In some embodiments, the integrated circuit further comprises an assembly including a first die having the plurality of microvaults including a first microvault and a second microvault, as well as a second die comprising a read address register and a read data register. The first die may be bonded to the second die in this assembly.

[0056] In some embodiments, the integrated circuit may involve an assembly with a first die and a second die bonded together. The first die may have a plurality of microvaults including a first microvault and a second microvault, while the second die may have a read address register and a read data register. The first die may include a second bonding area on the first surface, in addition to the first bonding area described previously. Furthermore, the second die may include a third bonding area and a fourth bonding area. The various bonding areas may be connected such that the first bonding area of the first die is coupled to the third bonding area of the second die, while the second bonding area of the first die is coupled to the fourth bonding area of the second die.

[0057] In some embodiments, the integrated circuit further comprises a read address register operatively coupled to the third bonding area of the second die to communicate read addresses there. The read address register is configured to hold and communicate read addresses to the first microvault on the first die via the third bonding area, which is coupled to the first bonding area of the first die.

[0058] In some embodiments, the integrated circuit further comprises a read data register operatively coupled to a fourth bonding area of the second die to receive read data therefrom. The read data register is configured to receive and hold read data communicated

from the fourth bonding area of the second die which is bonded to the first die having the plurality of microvaults.

[0059] In some embodiments, the integrated circuit may involve an assembly including a first die with a plurality of microvaults such as a first microvault and a second microvault. The first die may also include a second read address register configured to receive and hold a read address. This second read address register can be configured to communicate a read address to the first microvault and the second microvault.

[0060] In some embodiments, the assembly may include a first die with a plurality of microvaults including a first microvault and a second microvault. The first die can further comprise a multiplexer configured to select between an output of the first microvault and an output of the second microvault.

[0061] In some embodiments, the integrated circuit may further comprise a second bonding area on a second surface of the first die having the plurality of microvaults. An interconnect may connect this second bonding area to an input of a multiplexer, which is configured to select among the output of the first microvault, the output of the second microvault, and communication received from the second bonding area.

[0062] In some embodiments, the integrated circuit may further comprise a phase counter configured to control the multiplexer that selects between outputs from the first microvault and second microvault. The phase counter facilitates sequentially reading out data from the multiple microvaults through the use of the multiplexer.

[0063] In some embodiments, the integrated circuit may further comprise a third address register configured to receive and hold an output of the multiplexer. The multiplexer may be configured to select between one of the plurality of microvaults, and a phase counter may be configured to control the selection of the multiplexer. The third address register could receive and hold the output that is selected by the multiplexer.

[0064] The integrated circuit may involve an assembly including a first die having a plurality of microvaults including a first microvault and a second microvault, as well as a second die with a read address register and a read data register, where the first die is bonded to the second die. In some embodiments, the first die may further comprise a multiplexer configured to select among an output of the first microvault and an output of the second microvault, as well as a third address register configured to receive and hold an output of the multiplexer. Optionally, the third address register could be operatively coupled to a second bonding area of the first die.

[0065] The integrated circuit may further comprise a Through-Silicon Via (TSV) coupled to the read address register and a second surface of the die on which the read address register is disposed. In some embodiments, the TSV facilitates communication of data such as a read address between the read address register and components located on the opposite side of the die.

[0066] In some embodiments, the integrated circuit further comprises a second Through-Silicon Via (TSV) coupled to a second bonding area of the first die on the second surface and to a second read data register. The second TSV facilitates communication of data between the second bonding area on the second surface of the first die and the second read data register on another die. This configuration enables efficient transfer of read data between multiple dies that are stacked and bonded together.

[0067] In some embodiments, the integrated circuit may comprise a multiplexer configured to select between one of the plurality of microvaults. The multiplexer enables accessing data from different microvaults in a selective manner.

[0068] In some embodiments, the integrated circuit may further comprise a phase counter configured to control the selection operation of the multiplexer that selects between one of the plurality of microvaults. The phase counter provides control signals to the multiplexer to facilitate sequentially accessing data from multiple microvaults.

[0069] In some embodiments, the integrated circuit further comprises a Through-Silicon Via (TSV) that is operatively coupled to the first surface and a second surface of a die that has the plurality of microvaults. The TSV facilitates communication between the first surface having the plurality of microvaults and bonding areas and the opposite second surface of the die.

[0070] In some embodiments, the integrated circuit further comprises a Through-Silicon Via configured to facilitate communication between a second die coupled to a first die having the plurality of microvaults. The Through-Silicon Via enables inter-die communication and integration between the microvault die and additional dies in a multi-die assembly.

[0071] In some embodiments, the integrated circuit may involve the first microvault comprising at least one column of 3D-NORs formed from a plurality of transistors. Each transistor in these 3D-NOR columns may include a gate coupled to a read-write enable line, a source coupled to a bit line, and a drain coupled to a select line.

[0072] In some embodiments, the integrated circuit may comprise a first microvault that includes a column of 3D-NANDs formed from multiple transistors. Each transistor in the column can have a gate terminal coupled to a read/write enable line, a source terminal coupled

to a bit line, and a drain terminal coupled to a source terminal of an adjacent second transistor in the column. The 3D-NAND column configuration in the first microvault can facilitate dense vertical stacking of the transistors while allowing for separate control of read and write operations through the independent enable line.

[0073] In some embodiments, the integrated circuit may comprise a first microvault that includes a column of 3D-NANDs with a pass gate formed from a plurality of transistors. Each transistor in the column of 3D-NANDs may have a gate coupled to a read/write enable line, a source coupled to a bit line, and a drain coupled to a source of a second transistor. Additionally, a pass gate may be coupled to all of the plurality of transistors in the column of 3D-NANDs.

[0074] In some embodiments, the integrated circuit may comprise a first microvault that includes a column of 3D-NORs (three-dimensional NOR gates) with independent read and write enables formed from multiple transistors. Each transistor within the 3D-NOR gates can have a source terminal coupled to a bit line, a drain terminal coupled to a read enable line, and a gate terminal coupled to a write enable line. The independent read and write enable lines allow separate control over reading from and writing to the microvault.

[0075] In some embodiments, the plurality of microvaults may include a thermal management layer configured to dissipate heat generated by the microvaults during operation. This thermal management layer could optionally involve a material with high thermal conductivity selected from a group consisting of copper, aluminum, diamond, and graphene to facilitate heat dissipation.

[0076] In some embodiments, the integrated circuit further comprises a thermal management layer configured to dissipate heat generated by the microvaults during operation. This thermal management layer may optionally comprise a material with high thermal conductivity selected from a group consisting of copper, aluminum, diamond, and graphene.

[0077] In some embodiments, the integrated circuit further comprises a hardware-based encryption module operatively coupled to at least one microvault. The encryption module functions to secure data that is written to or read from the microvault. By incorporating hardware-based encryption into the integrated circuit, data stored in the microvaults can be protected.

[0078] In some embodiments, the integrated circuit further comprises a power management circuit configured to adjust the voltage and current supplied to the plurality of microvaults. The adjustment of voltage and current by the power management circuit may be based on the operational status of the microvaults. For example, the power management circuit

may include a low-power mode that reduces power supply to the microvaults during periods of inactivity.

[0079] The integrated circuit may include a power management circuit configured to adjust voltage and current supplied to the plurality of microvaults based on their operational status. In some embodiments, the power management circuit includes a low-power mode that reduces power supply to the microvaults during periods of inactivity.

[0080] In some embodiments, the integrated circuit may further comprise a signal conditioning circuit operatively coupled to the plurality of microvaults. The signal conditioning circuit may be configured to enhance signal integrity of data transfers to and from the microvaults. Optional components of the signal conditioning circuit may include filters, amplifiers, or error-correction coders.

[0081] In some embodiments, the integrated circuit further comprises a signal conditioning circuit operatively coupled to the plurality of microvaults to enhance signal integrity of data transfers. The signal conditioning circuit may involve filters, amplifiers, or error-correction coders to enhance the signal integrity.

[0082] In some embodiments, the integrated circuit further comprises a diagnostic module configured to monitor the health and performance of the microvaults and report metrics to an external controller. The diagnostic module may be capable of performing self-tests on the microvaults and generating alerts if malfunctions are detected.

[0083] In some embodiments, the integrated circuit further comprises a diagnostic module configured to monitor the health and performance of the microvaults and report metrics to an external controller. Optionally, this diagnostic module is capable of performing self-tests on the microvaults and generating alerts if malfunctions are detected.

[0084] In some embodiments, each microvault may include a built-in self-repair mechanism that is capable of isolating and bypassing faulty memory cells. The self-repair mechanism can optionally utilize redundancy in the form of spare memory cells that can be dynamically allocated to replace the faulty cells.

[0085] In some embodiments, each microvault may include a built-in self-repair mechanism capable of isolating and bypassing faulty memory cells. This self-repair mechanism may utilize redundancy in the form of spare memory cells that can be dynamically allocated to replace any faulty cells that are detected.

[0086] In some embodiments, the microvaults may be arranged in a matrix configuration to enable parallel processing and data retrieval.

[0087] In some embodiments, the microvaults may be arranged in a matrix configuration to enable parallel processing and data retrieval. The matrix configuration may optionally include row and column decoders to facilitate access to individual microvaults.

[0088] In some embodiments, the integrated circuit further comprises a flexible substrate. The flexible substrate enables the integrated circuit to conform to non-planar surfaces.

[0089] In some embodiments, the integrated circuit further comprises a flexible substrate that enables the circuit to conform to non-planar surfaces. The flexible substrate may be comprised of materials such as polyimide, PEEK (polyether ether ketone), liquid crystal polymer, flexible glass, or combinations thereof. By using a flexible substrate, the embodiment can be applied to and function properly on curved or irregular surfaces.

[0090] In some embodiments, the integrated circuit may involve the first microvault being configured to operate as a cache memory for a processor. The cache memory can function in one or more modes such as write-through, write-back, write-around, or a combination thereof.

[0091] In some embodiments, the first microvault may be configured to operate as a cache memory for a processor. The cache memory may operate in one or more cache modes such as write-through, write-back, write-around, or a combination thereof.

[0092] In some embodiments, the plurality of microvaults may form a redundant array of independent memory elements. The redundant array of independent memory elements enables error correction and facilitates data recovery in the event of memory failures. Specifically, the first microvault can be configured as one element in an array of redundant, independent memory blocks, allowing data errors or failures in one block to be reconstructed from the other independent blocks. The redundant array architecture provides fault tolerance and reliability to help ensure operational continuity.

[0093] In some embodiments, the first microvault may include a crossbar switch architecture to facilitate data routing between memory cells. This crossbar switch architecture can enable non-blocking data transfer within the integrated circuit.

[0094] The integrated circuit may involve a crossbar switch architecture associated with the first microvault to facilitate data routing between memory cells. In some embodiments, this crossbar switch architecture is configured to enable non-blocking data transfer within the integrated circuit.

[0095] In some embodiments, the integrated circuit may involve the first microvault including a dedicated read peripheral. Specifically, the first microvault can optionally have its

own read peripheral, separate from other components, to facilitate data reads. This dedicated read peripheral for the first microvault enables optimized readout performance.

[0096] In some embodiments, the integrated circuit may include a dedicated read port operatively coupled to the first microvault. This allows read operations to be performed on the first microvault independently of write operations, enabling concurrent read and write access. The dedicated read port improves overall data throughput by eliminating contention between reading and writing data.

[0097] In some embodiments, the integrated circuit may include a dedicated write peripheral associated with the first microvault. This allows write operations to the first microvault to be handled by specialized write circuitry tailored for efficient writing. The dedicated write peripheral facilitates quick and reliable data storage within the microvault by optimizing the write path.

[0098] In some embodiments, the integrated circuit may include a dedicated write port operatively coupled to the first microvault. This dedicated write port facilitates writing data to the first microvault independently of read operations, enabling concurrent read and write access. The dedicated write port can improve overall data throughput to and from the microvault.

[0099] The integrated circuit may comprise a first transistor with a channel layer formed using a semiconductor material and a ferroelectric layer rigidly coupled to the channel layer. The first transistor may further comprise a source terminal fixed to the channel layer, a drain terminal fixed to the channel layer, and a gate terminal fixed to the ferroelectric layer.

[00100] In some embodiments, the channel layer of the first transistor may be formed from a polycrystalline silicon. The use of polycrystalline silicon for the channel layer provides known electrical properties that allow proper functioning of the transistor.

[00101] In some embodiments, the channel layer of the transistor may be formed from an Amorphous Oxide Semiconductor. This amorphous oxide semiconductor material can provide desirable properties such as high carrier mobilities and low off-state currents when used as the channel layer, while also being compatible with deposition on top of standard CMOS materials during back-end-of-line processing. Examples of amorphous oxide semiconductors that could be utilized include Indium Oxide, Indium Gallium Zinc Oxide (IGZO), Zinc Tin Oxide (ZTO), Indium Zinc Oxide (IZO), Gallium Zinc Oxide (GZO), Aluminum Zinc Oxide (AZO), Cadmium Oxide, Hafnium Indium Zinc Oxide (HIZO), Tin Oxide, and Indium-Tin-Zinc Oxide (ITZO), among others. The amorphous oxide

semiconductor channel layer may also be doped with elements such as Gallium, Indium, Zinc, Tin, Hafnium, Silicon, Aluminum, and others to optimize carrier concentration and mobility.

[00102] In some embodiments, the amorphous oxide semiconductor forming the channel layer of the first transistor may include at least one of indium oxide, indium gallium zinc oxide, zinc tin oxide, indium zinc oxide, gallium zinc oxide, aluminum zinc oxide, cadmium oxide, hafnium indium zinc oxide, tin oxide, stannous tin oxide, stannic tin oxide, indium-tin-zinc oxide, indium-tungsten oxide, indium-gallium-zinc-tin oxide, indium-gallium-zinc-oxynitride, aluminum-indium-gallium-zinc oxide, and zinc-indium oxide.

[00103] In some embodiments, the Amorphous Oxide Semiconductor channel layer, may be doped with at least one dopant selected from the group consisting of Gallium (Ga), Indium (In), Zinc (Zn), Tin (Sn), Hafnium (Hf), Silicon (Si), Aluminum (Al), Magnesium (Mg), Calcium (Ca), Strontium (Sr), Barium (Ba), Titanium (Ti), Zirconium (Zr), Molybdenum (Mo), Tantalum (Ta), Niobium (Nb), Chromium (Cr), Iron (Fe), Cobalt (Co), Nickel (Ni), Copper (Cu), Silver (Ag), Gold (Au), Cerium (Ce), Lanthanum (La), Neodymium (Nd), Samarium (Sm), Europium (Eu), Gadolinium (Gd), Terbium (Tb), Dysprosium (Dy), Holmium (Ho), Erbium (Er), Thulium (Tm), Ytterbium (Yb), Lutetium (Lu), Yttrium (Y), Scandium (Sc), Bismuth (Bi), Lead (Pb), Thallium (Tl), Antimony (Sb), Arsenic (As), Phosphorus (P), Boron (B), Nitrogen (N), Fluorine (F), Chlorine (Cl), Bromine (Br), and Iodine (I). The doping of the channel layer may enhance certain properties of the transistor such as carrier mobility, threshold voltage, subthreshold swing, on-state current, and off-state current.

[00104] In some embodiments, the channel layer of the first transistor is formed from two dimensional materials including transition metal dichalcogenides. The transition metal dichalcogenides may be in a monovalent or divalent form. In certain embodiments, the chalcogenide element in the transition metal dichalcogenides is sulfur, selenium or tellurium.

[00105] The transition metal dichalcogenides (TMDs) may be written as MX_2 where M refers to transition metal atom, such as molybdenum (Mo), tungsten (W), platinum (Pt), and palladium (Pd), while X is the chalcogen atom, such as sulfur (S), selenium (Se), and tellurium (Te). The TMDs present a wide range of electrical properties from semiconducting [molybdenum disulfide (MoS_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), and tungsten diselenide (WSe_2)], to semimetallic [molybdenum ditelluride ($MoTe_2$), tungsten ditelluride (WTe_2), and titanium diselenide ($TiSe_2$)], to metallic niobium disulfide (NbS_2), titanium disulfide (TiS_2), nickel disulfide (NiS_2), and vanadium diselenide (VSe_2)], and to superconducting [niobium diselenide ($NbSe_2$) and tantalum sulfide (TaS_2)] regimes.

[00106] In some embodiments, the channel layer of the integrated circuit is formed from two dimensional materials including transition metal dichalcogenides. The transition metal dichalcogenides may be monovalent in these embodiments.

[00107] In some embodiments, the channel layer of the integrated circuit embodiment may be formed from two dimensional transition metal dichalcogenides materials. Specifically, these transition metal dichalcogenides may have a divalent transition metal composition. The use of divalent transition metal dichalcogenides for the channel layer enables favorable electrical properties for the operation of transistors formed from the integrated circuit components.

[00108] In some embodiments, the transition metal dichalcogenides from which the channel layer is formed can have a chalcogenide element that is sulfur.

[00109] In some embodiments, the integrated circuit may comprise transition metal dichalcogenides wherein the channel layer is formed. The transition metal dichalcogenides may be monovalent or divalent. Optionally, the chalcogenide element in the transition metal dichalcogenides could be selenium.

[00110] In some embodiments, the integrated circuit may involve the channel layer being formed from two dimensional materials including transition metal dichalcogenides. The transition metal dichalcogenides may have a chalcogenide element such as tellurium.

[00111] In some embodiments, the channel layer of the transistor may be formed from Indium Tungsten Oxide (IWO). This material can provide desirable properties for the channel layer, such as high mobility for charge carriers. The use of IWO allows for fabrication of high performance transistors suitable for various integrated circuit applications.

[00112] In some embodiments, the channel layer of the transistor may be formed from an indium gallium zinc oxide (IGZO). The IGZO material provides desirable properties for the channel layer such as high electron mobility and stability when deposited as a thin film, allowing effective operation of the transistors within the integrated circuit.

[00113] In some embodiments, the channel layer may be a thin film.

[00114] The embodiment may involve the ferroelectric layer being composed of hafnium zirconium oxide with an equal molar ratio of hafnium to zirconium ($\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$).

[00115] In some embodiments, the integrated circuit comprising the ferroelectric FET may be disposed on a back-end-of-the-line (BEOL) portion of a semiconductor device fabrication flow. More specifically, this would involve fabricating the integrated circuit containing the ferroelectric layer and channel layer of the FET on the higher layers above the transistor level after the front-end-of-line processing has been completed. Disposing the

integrated circuit in the BEOL portion enables integration with underlying transistor structures and metal interconnect layers that have already been fabricated on the chip.

[00116] In some embodiments, the ferroelectric layer in the integrated circuit is made of transition metal oxides, a perovskite, or a two-dimensional material.

[00117] In some embodiments, the integrated circuit further comprises a metal layer disposed between the channel layer and the ferroelectric layer.

[00118] In some embodiments, the integrated circuit further comprises an insulator layer disposed between the metal layer and the channel layer. Specifically, a metal layer may be disposed between the channel layer and the ferroelectric layer. Additionally, an insulator layer is disposed between this metal layer and the underlying channel layer.

[00119] In some embodiments, the integrated circuit further comprises a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer.

[00120] In some embodiments, the integrated circuit further comprises a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer. Additionally, in some embodiments, an insulation layer is disposed on the channel layer, and the ferroelectric layer is also disposed on the insulation layer.

[00121] The embodiment may further comprise a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer. This additional metal layer on top of the ferroelectric material can serve various purposes, such as providing an improved electrical contact or acting as a barrier layer. Its integration on top of the ferroelectric and channel layers enables optimization of the electrical performance and reliability of the ferroelectric field-effect transistor.

[00122] In some embodiments, the channel layer of the integrated circuit may have a thickness of less than 30 nm. Constructing the channel layer to be this thin allows for reduced dimensions and potentially improved performance of the transistors formed using the channel layer.

[00123] In some embodiments, the channel layer may have a thickness between 1 to 30 nm. Configuring the channel layer to be less than 30 nm in thickness enables effective charge modulation by the adjacent ferroelectric layer within this ultra-scaled dimension. Maintaining dimensions on the lower end of this range, between 1 to 10 nm for example, allows the integrated circuit to leverage improvements in channel controllability and reduced short-channel effects. The relatively thin channel layer dimension thus facilitates low voltage operation and efficient switching.

[00124] In some embodiments, the channel layer of the transistor may be formed using physical vapor deposition or chemical vapor deposition. These deposition techniques can be used to deposit very thin films needed for the channel layer. The channel layer formed in this way may be less than 30 nm in thickness or between 1 to 30 nm in thickness.

[00125] In some embodiments, the channel layer of the integrated circuit is formed using atomic layer deposition. This manufacturing process enables precise thickness control and uniform coverage during the deposition of the thin channel layer. By building up the channel layer one atomic layer at a time through sequential, self-limiting surface reactions, atomic layer deposition allows for sub-nanometer thickness control.

[00126] The embodiment may involve the channel layer being formed by adding a dopant comprising at least one of tungsten, gallium (Ga), and zinc (Zn). In some embodiments, the channel layer is formed using physical vapor deposition or chemical vapor deposition, and the dopant helps enable deposition of the thin channel layer.

[00127] The embodiment may involve the ferroelectric layer being formed using atomic layer deposition.

[00128] In some embodiments, the integrated circuit's ferroelectric layer may be formed using vapor deposition.

[00129] In some embodiments, the ferroelectric layer in the integrated circuit is formed by adding a dopant comprising at least one of Lanthanum, Niobium, Manganese, Zirconium, Tin, Strontium, Calcium, Yttrium, or Magnesium. The doped ferroelectric layer may be formed using atomic layer deposition or vapor deposition methods. Doping the ferroelectric material can potentially enhance characteristics such as crystallization temperature, remanent polarization, and leakage current.

[00130] In some embodiments, the channel layer may be configured to have a carrier concentration ranging from 10^{17} to 10^{20} per cubic centimeter.

[00131] In some embodiments, the channel layer comprises a two-dimensional material. The two-dimensional material may maintain an electron mobility of at least 0.1 cm-squared per Volt-second when the channel layer is less than 30nm in thickness. In certain embodiments, the channel layer comprises fewer than 5 monolayers of the two-dimensional material.

[00132] In some embodiments, the channel layer comprises a two-dimensional material. The two-dimensional material may be configured to maintain an electron mobility of at least 0.1 cm-squared per Volt-second when the channel layer is less than 30nm in thickness.

[00133] In some embodiments, the channel layer may comprise a two-dimensional material that maintains high electron mobility even when the channel layer is less than 30nm

in thickness. Optionally, the channel layer may comprise fewer than 5 monolayers of this two-dimensional material. Using only a few monolayers can help minimize thickness while retaining the beneficial properties of the two-dimensional material.

[00134] In some embodiments, the ferroelectric layer utilized in the integrated circuit is Hafnium Zirconium Oxide.

[00135] In some embodiments, the integrated circuit has a ferroelectric layer with a coercive voltage between -3 volts to 3 volts. This specifies the range of voltages that can switch the electric polarization of the ferroelectric material within the layer. By tuning the composition and thickness of the ferroelectric layer, it may exhibit a coercive voltage within this range which enables switching at low voltages compatible with transistor operation. Keeping the coercive voltage relatively low can help reduce the operating voltages and power consumption of devices incorporating the ferroelectric layer.

[00136] In some embodiments, the integrated circuit may have a ferroelectric layer with an off-state current less than 10^{-7} amps per centimeter cubed.

[00137] In some embodiments, the integrated circuit may involve a ferroelectric layer with an on-state current greater than 10^{-7} amps per centimeter cubed.

[00138] In some embodiments, the integrated circuit has a ferroelectric layer with a crystallization anneal temperature less than or equal to 500 degrees Celsius.

[00139] In some embodiments, the integrated circuit may involve a ferroelectric layer with a remanent polarization greater than 10 microcoulombs per square centimeter.

[00140] In some embodiments, the integrated circuit may involve a channel layer that is annealed at a temperature less than 450 degrees Celsius. Specifically, the channel layer forming part of the transistor structure in the integrated circuit can undergo an annealing process below 450 Celsius. Maintaining a sufficiently low anneal temperature for the channel layer facilitates integration of the ferroelectric material while preserving the integrity of the channel layer itself during device fabrication.

[00141] In some embodiments, the embodiment comprises a channel layer with a channel mobility of less than 100 centimeters squared per volt-second. Specifically, the channel layer that is part of the integrated circuit with a transistor including a channel layer, a ferroelectric layer, a source terminal, a drain terminal, and a gate terminal has a channel mobility that is configured to be less than $100 \text{ cm}^2/\text{V-s}$.

[00142] In some embodiments, the integrated circuit comprises a channel layer with a subthreshold swing of less than 0.3 volts per decade. The subthreshold swing refers to the change in gate voltage needed to reduce the current in the transistor by one decade, and a lower

subthreshold swing enables faster switching speeds and lower power consumption. By using novel materials and optimized interfaces between the layers, the channel layer can achieve this ultra-low subthreshold swing.

[00143] In some embodiments, the channel layer in the integrated circuit may be configured to have an off-state current of less than 10^{-7} amps per micrometer.

[00144] In some embodiments, the embodiment includes a channel layer that is configured to have a channel bandgap greater than 2.5 electron-volts.

[00145] In some embodiments, the channel layer may be configured to have a post-anneal threshold voltage between -1.5 Volts to 1.5 Volts.

[00146] In some embodiments, the integrated circuit may involve a first transistor having a width of less than 200 nm and a length of 50 nm.

[00147] The first transistor may have a device area of less than 30 times the square of the feature size.

[00148] In some embodiments, the integrated circuit may have a first transistor with a low-voltage threshold (LVT) level greater than -2.5V.

[00149] In some embodiments, the integrated circuit may have a first transistor with a high-voltage threshold (HVT) level greater than -2V.

[00150] In some embodiments, a memory cell incorporating the first transistor has a read voltage between 0V to 1V. Operating the memory cell having the first transistor at a read voltage in this range may facilitate low power consumption during read operations. Configuring the transistor characteristics to enable a low read voltage can also contribute to minimizing the overall power requirements of the integrated circuit.

[00151] In some embodiments, a memory cell incorporating the first transistor may have low read energy consumption of less than 10 picojoules. Specifically, a memory cell containing the ferroelectric field effect transistor detailed previously can optionally be designed and configured to enable read operations that dissipate less than 10 picojoules of energy. The extremely low read energy would allow the fabrication of low-power nonvolatile memories well-suited for battery-powered and energy-constrained applications.

[00152] In some embodiments, a memory cell incorporating the first transistor may have a read pulse width of less than 20 nanoseconds.

[00153] In some embodiments, a memory cell having the first transistor may have a read endurance greater than or equal to 10^9 cycles. This indicates that the memory cell can reliably withstand at least one billion read operations without failure, contributing to high reliability and long operating lifetime.

[00154] In some embodiments, a memory cell incorporating the first transistor may have a read disturb tolerance greater than 10^9 cycles. This indicates that the memory cell can withstand at least 10^9 read cycles without the stored data being disturbed or corrupted, enabling reliable long-term data storage. The high read disturb tolerance is achieved in part due to the properties and configuration of the ferroelectric layer, channel layer, and other components in the first transistor.

[00155] In some embodiments, a memory cell incorporating the first transistor may have a read after write latency less than or equal to 10 microseconds. This indicates that the time delay between completing a write operation to the memory cell and being able to reliably read back the stored data is very short. Enabling such fast read access times allows building high performance memory systems.

[00156] In some embodiments, a memory cell incorporating the first transistor described herein has a write voltage less than or equal to 3.0 Volts (V).

[00157] In some embodiments, a memory cell incorporating the first transistor may have a write speed less than or equal to 10 microseconds.

[00158] In some embodiments, a memory cell having the first transistor described herein has a write energy that is less than 10 picojoules.

[00159] In some embodiments, a memory cell incorporating the first transistor may have a write endurance greater than 10^8 cycles. This indicates that the memory cell can withstand at least 100 million write cycles without failure, enabling reliable data storage and retrieval over an extended lifespan. By leveraging the performance characteristics of the underlying ferroelectric field effect transistor, each memory cell can offer improved durability and longevity compared to conventional alternatives. The high write endurance further translates to enhanced data integrity and a reduced need for error correction or redundancy.

[00160] In some embodiments, a memory cell having the first transistor described herein has an off-state resistance to on-state resistance ratio (R_{off}/R_{on}) of about 10^3 or greater than 10^2 .

[00161] In some embodiments, a memory cell incorporating the first transistor may have an on-state current to off-state current ratio (I_{on}/I_{off}) at V_{read} from DC measurement greater than 100. Specifically, the memory cell with the ferroelectric field effect transistor can achieve a high on-state to off-state current ratio during read operations, indicating good discrimination between logic 0 and logic 1 states stored in the cell. The high I_{on}/I_{off} ratio contributes to reliable read operations at low voltages.

[00162] In some embodiments, the memory cell may include the first transistor as described herein and a second transistor having the same configuration as the first transistor. The first transistor and the second transistor can form a bit state for storing a binary value in the memory cell.

[00163] In some embodiments, the integrated circuit may involve a memory cell having the first transistor, wherein the first transistor is configured to have 3 or more states. Each of these states corresponds to a stored value of the memory cell. This allows for multi-level data storage within a single memory cell.

[00164] In some embodiments, the integrated circuit may involve a first transistor that has an on-state current to off-state current ratio (I_{on}/I_{off}) at V_{read} from pulse measurement that is greater than 10^2 .

[00165] In some embodiments, the integrated circuit comprises a first transistor, as described herein. Optionally, the first transistor may include an off-state leakage current (I_{off}) that is less than ten to the negative fourteenth amps per micrometer, providing very low leakage when the transistor is not conducting in the off-state. By having an off-state leakage current below this threshold, the transistor exhibits very little leakage through the channel and maintains the off-state effectively, allowing for low static power consumption.

[00166] In some embodiments, a memory cell having the first transistor may have a reliability endurance greater than or equal to 10^{11} cycles. This high reliability endurance allows the memory cell to withstand an extremely large number of read/write cycles without failure over its lifetime. The robust endurance enables applications requiring frequent data access with minimal downtime for repairs or replacements.

[00167] In some embodiments, a memory cell having the first transistor described herein has a retention time of at least 1 minute when measured at room temperature of 25 C.

[00168] In some embodiments, the channel layer of the first transistor may involve incorporation of another two-dimensional material configured to enhance the on-state current (I_{ON}) through the transistor. The additional two-dimensional material provides increased conductivity to allow higher I_{ON} when the transistor is switched on.

[00169] In some embodiments, the channel layer in the integrated circuit is configured to maintain high mobility despite the presence of the ferroelectric layer. Specifically, the channel layer and ferroelectric layer are designed such that the ferroelectric layer does not significantly impede the electron mobility within the channel layer. This allows the integrated circuit transistor to operate with high channel mobility for improved performance while still utilizing the benefits of the ferroelectric layer.

[00170] In some embodiments, the integrated circuit may be configured such that the ferroelectric layer does not significantly impede the electron mobility within the channel layer. The ferroelectric layer and the channel layer may be designed to maintain high mobility despite the presence of the ferroelectric layer on top of the channel layer. For example, the interface between the ferroelectric layer and the channel layer may be optimized to minimize scattering of electrons flowing through the channel.

[00171] In some embodiments, the channel layer is configured to be directly in contact with the ferroelectric layer without an interfacial layer in between. The direct contact between the channel layer and the ferroelectric layer may facilitate minimized voltage drops across the interface, thereby enabling low voltage operation of the transistor. Moreover, the absence of an interfacial layer between the channel layer and ferroelectric layer can allow for low voltage operation and decreased power consumption.

[00172] In some embodiments, the integrated circuit may comprise a first transistor with a channel layer that is in direct contact with the ferroelectric layer, without an interfacial layer in between. This direct contact configuration may help to minimize voltage drops across the interface between the channel layer and the ferroelectric layer. By reducing such parasitic voltage drops, the first transistor can potentially be operated at lower voltages, thereby enabling low voltage operation and reduced power consumption. The absence of an interfacial layer can also contribute to faster switching times and improved transient characteristics.

[00173] The integrated circuit may involve a first transistor characterized by low voltage operation and low power consumption. This is due to the absence of an interfacial layer between the channel layer and the ferroelectric layer in some embodiments.

[00174] In some embodiments, the integrated circuit may involve a first transistor characterized by low voltage operation and low power consumption. This can be due to the absence of an interfacial layer between the ferroelectric layer and the gate layer of the first transistor. The reduced voltage operation can contribute to a decrease in overall power consumption of the integrated circuit.

[00175] In some embodiments, the integrated circuit is characterized by low voltage operation and low power consumption due to the absence of an interfacial layer between the channel layer and the ferroelectric layer or between the ferroelectric layer and the gate layer. This reduced voltage operation may contribute to a decrease in the overall power consumption of the integrated circuit.

[00176] In some embodiments, the integrated circuit may involve the first transistor being characterized by improved switching characteristics such as faster turn-on and turn-off

times. This may be due to the absence of an interfacial layer between the ferroelectric layer and the channel layer or between the ferroelectric layer and the gate layer. The lack of an interfacial layer can contribute to reduced parasitic capacitance at these interfaces, enabling faster charging and discharging of the ferroelectric layer during write and erase operations of the transistor.

[00177] In some embodiments, the integrated circuit may be characterized by reduced parasitic capacitance at the interface between the channel layer and the ferroelectric layer due to the absence of an interfacial layer between them. The direct contact between the channel layer and the ferroelectric layer can minimize voltage drops across the interface, enabling low voltage operation of the transistors. The reduced parasitic capacitance can also contribute to improved switching characteristics of the transistors, including faster turn-on and turn-off times.

[00178] In some embodiments, the ferroelectric layer may be configured for a substantially uniform electric field distribution across the ferroelectric layer.

[00179] In some embodiments, the integrated circuit may involve the ferroelectric layer being configured for a gradient in the electric field distribution across the ferroelectric layer.

[00180] In some embodiments, the integrated circuit further comprises a microvault formed from a plurality of transistors including the first transistor as described herein. The microvault may be organized into columns comprising 3 terminal bit-cells. Optionally, the microvault is formed via a column in one of a 3D-NOR, a 3D-AND, a 3D-NAND, or a 3D-NAND-PG configuration.

[00181] In some embodiments, the microvault comprises columns of 3-terminal bit cells. Specifically, the plurality of transistors that make up each microvault may be arranged into vertical columns, with each column functioning as a bit cell having three terminals - source, drain, and gate terminals corresponding to the transistors in that column. This 3-terminal bit cell configuration in columnar form facilitates compact integration and wiring of the microvault memory structure.

[00182] In some embodiments, the integrated circuit may comprise a microvault formed from a plurality of transistors. The microvault may be organized into columns comprising 3 terminal bit-cells in one of several configurations, including a 3D-NOR, a 3D-AND, a 3D-NAND, or a 3D-NAND with an additional pass gate (3D-NAND-PG).

[00183] The integrated circuit may comprise a channel material that includes Indium Gallium Zinc Oxide (IGZO) in some embodiments. The channel material formed from IGZO can be incorporated into the transistors described herein.

[00184] The embodiment may comprise a source terminal fixed to the channel layer. In some embodiments, the source terminal is formed from at least one of Tungsten, Titanium Nitride, Nickel, and Molybdenum.

[00185] In some embodiments, the drain terminal of the first transistor comprises at least one of Tungsten, Titanium Nitride, Nickel, and Molybdenum. These materials may be utilized to form the drain contact to enable effective carrier transport and integration within the fabrication process flow.

[00186] In some embodiments, the gate terminal of the first transistor comprises at least one of tungsten, titanium nitride, nickel, and molybdenum. These materials are utilized for their conductive properties and integration compatibility in semiconductor fabrication processes. The selection of an appropriate gate terminal material can impact transistor performance and reliability.

[00187] In some embodiments, the integrated circuit further comprises a memory formed from a plurality of the first transistors. The memory may be formed as a 3D vertical device architecture selected from NAND and NOR configurations.

[00188] In some embodiments, the integrated circuit comprises a microvault column comprising a plurality of transistors. Each of the plurality of transistors in the microvault column may be configured the same as the first transistor described previously. The microvault column comprising the plurality of identical transistors may be organized into a 3D vertical architecture such as a 3D-NOR, a 3D-AND, a 3D-NAND, or a 3D-NAND with pass gate.

[00189] In some embodiments, the integrated circuit may comprise a microvault column comprising a plurality of transistors, each of the transistors configured identically to the first transistor. The microvault column may be organized in a 3D-NOR configuration.

[00190] In some embodiments, the integrated circuit comprises a microvault column comprising a plurality of transistors, each of the transistors configured according to the first transistor. The microvault column may be configured as a 3D-AND structure.

[00191] In some embodiments, the integrated circuit may comprise a microvault column comprising a plurality of transistors, each configured similar to the first transistor. The microvault column may be arranged in a 3D-NAND configuration.

[00192] In some embodiments, the integrated circuit may comprise a microvault column comprising a plurality of transistors, wherein each of the plurality of transistors is configured according to the first transistor design as described previously. The microvault column may be organized in a 3D-NAND architecture with a pass gate coupled to all of the plurality of transistors.

[00193] In some embodiments, the integrated circuit may involve a microvault column comprising a plurality of transistors, wherein each transistor includes a source coupled to a bit line, a drain coupled to a read enable line, and a gate coupled to a write enable line. This microvault column configuration enables independent control of reading and writing operations through separate read and write enable lines.

[00194] In some embodiments, the integrated circuit may comprise a microvault column comprising a plurality of transistors, each formed similarly to the first transistor. The microvault column may be configured as a 3D-AND architecture with an independent read/write enable line coupled to each transistor. Specifically, each transistor in the 3D-AND microvault column may have a source terminal coupled to a bit line, a drain terminal coupled to a select line, and a gate terminal coupled to a read/write enable line that is independent from the other transistors.

[00195] In some embodiments, the ferroelectric layer utilized in the integrated circuit is formed from various ferroelectric materials including but not limited to perovskites, lead zirconate titanate (PZT), barium titanate (BaTiO_3), strontium titanate (SrTiO_3), bismuth ferrite (BiFeO_3), potassium niobate (KNbO_3), lithium niobate (LiNbO_3), lithium tantalate (LiTaO_3), sodium bismuth titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$), bismuth titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), bismuth zinc niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$), bismuth lanthanum titanate (BiLaTiO_3), bismuth nickel titanate (BiNiTiO_3), lead magnesium niobate-lead titanate (PMN-PT), lead lanthanum zirconate titanate (PLZT), neodymium-doped bismuth titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$), hafnium-based oxides like hafnium oxide (HfO_2) and doped hafnium oxide such as zirconium-doped hafnium oxide (HfZrO_2), tungsten bronze structure materials including barium strontium niobate (BSN), lead barium niobate (PBN), and potassium tantalate niobate (KTN), bismuth layer-structured ferroelectrics like bismuth titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), strontium bismuth tantalate (SBT), and calcium bismuth niobate (CBN), organic ferroelectrics such as polyvinylidene fluoride (PVDF), TrFE (trifluoroethylene), and P(VDF-TrFE) copolymers, aurivillius phase oxides, rare earth manganites like YMnO_3 and lanthanum-modified lead zirconate titanate (PLZT), nickel manganese oxide (NiMnO_3), relaxor ferroelectrics including lead magnesium niobate (PMN), lead scandium tantalate (PST), lead indium niobate (PIN), multiferroic materials like terbium manganite (TbMnO_3) and europium titanium oxide (EuTiO_3), SbSI (antimony sulfoiodide), GeTe (germanium telluride), SnTe (tin telluride), thin-film ferroelectrics such as PZT thin films, SBT thin films, and HfO_2 -based thin films, layered superlattices, and $\text{PbTiO}_3/\text{SrTiO}_3$. The wide range of ferroelectric materials provides flexibility in designing the integrated circuit depending on the intended application and desired device characteristics.

[00196] In some embodiments, the integrated circuit comprises a first vertical structure with a dielectric column, a channel column disposed around the dielectric column, and a ferroelectric column disposed around the channel column along its length. The integrated circuit further comprises a plurality of horizontal gate-electrode layers, each disposed a predetermined distance from each other. Each of the horizontal gate-electrode layers is disposed adjacent to the ferroelectric column along its length.

[00197] The integrated circuit embodiment may have a dielectric column that is substantially cylindrical in shape. Specifically, the dielectric column around which the channel column is disposed can be formed to have a circular or elliptical cross-section along its vertical length. Making the dielectric column cylindrical can facilitate conformal deposition of the surrounding channel material.

[00198] In some embodiments, the dielectric column in the first vertical structure is substantially cylindrical. The dielectric column may have a first diameter on a first end and a second diameter on the second end. Optionally, the first and second diameters can be the same or the first diameter can be larger than the second diameter.

[00199] In some embodiments, the dielectric column of the first vertical structure is substantially cylindrical, with a first diameter on a first end and a second diameter on a second, opposite end. Optionally, the first and second diameters of the dielectric column may be configured to be the same.

[00200] In some embodiments, the dielectric column in the first vertical structure has a first diameter on a first end and a second diameter on the second end, where the first diameter is larger than the second diameter.

[00201] In some embodiments, the integrated circuit comprises a first vertical structure with a dielectric column. The dielectric column may be configured as a solid column rather than a hollow column. Forming the dielectric column as a solid structure can provide mechanical stability and robustness to the overall vertical stack.

[00202] In some embodiments, the integrated circuit may involve a dielectric column that is hollow. Specifically, the dielectric column that is disposed around the channel column in the first vertical structure can optionally be configured as a hollow column, rather than a solid column. This hollow configuration of the dielectric column can facilitate certain fabrication processes or enable additional components to be integrated within the column. However, in other embodiments, the dielectric column may be implemented as a solid column instead.

[00203] In some embodiments, the channel column formed around the dielectric column in the first vertical structure may be substantially cylindrical in shape. For example, the channel column could have a circular or oval cross-section along its vertical length. A cylindrical channel column configuration may provide certain advantages related to current flow, capacitance, or ease of manufacturing.

[00204] In some embodiments, the channel column formed around the dielectric column is substantially cylindrical, as described in the summary section. Optionally, the channel column has a first diameter on a first end and a second diameter on the second end. In certain embodiments, the first and second diameters may be the same. In other embodiments, the first diameter may be larger than the second diameter.

[00205] In some embodiments, the channel column of the first vertical structure has a substantially cylindrical shape with a uniform diameter from a first end to a second end.

[00206] In some embodiments, the integrated circuit comprises a first vertical structure with a dielectric column that has a first diameter on a first end and a second diameter on the second end, wherein the first diameter is larger than the second diameter.

[00207] The ferroelectric column may be substantially cylindrical. In some embodiments, the integrated circuit further comprises a first vertical structure with a ferroelectric column disposed around a channel column. Optionally, this ferroelectric column may be formed in a substantially cylindrical shape.

[00208] In some embodiments, the integrated circuit may have a ferroelectric column that is substantially cylindrical, as described for the first vertical structure. This ferroelectric column may have a first diameter on a first end and a second diameter on the second, opposing end. The first and second diameters may be the same or the first diameter may be larger than the second diameter in some cases.

[00209] In some embodiments, the integrated circuit has a ferroelectric column that is substantially cylindrical, with a first diameter on a first end and a second diameter on a second end, where the first and second diameters may be configured to be the same.

[00210] In some embodiments, the integrated circuit may involve a ferroelectric column that is substantially cylindrical. The ferroelectric column may have a first diameter on a first end and a second diameter on the second end, wherein the first diameter is larger than the second diameter.

[00211] In some embodiments, the integrated circuit further comprises a dielectric end column disposed around an end of the channel column. This dielectric end column is positioned

adjacent to an end of the length of the channel column and also adjacent to the ferroelectric column.

[00212] In some embodiments, the integrated circuit further comprises a drain select layer disposed in parallel with the plurality of horizontal gate-electrode layers and adjacent to the dielectric end column. This drain select layer is arranged adjacent to the dielectric end column that surrounds one end of the channel column. By positioning the drain select layer parallel to the horizontal gate-electrode layers and next to the dielectric end column, access to the drain side of the vertical structure can be enabled.

[00213] In some embodiments, the integrated circuit further comprises a second dielectric end column disposed around another end of the channel column. This second dielectric end column is adjacent to another end of the length of the channel column and also adjacent to the ferroelectric column.

[00214] The integrated circuit may further comprise a source select layer disposed in parallel with the plurality of horizontal gate-electrode layers. This source select layer would be adjacent to the second dielectric end column that is disposed around another end of the channel column. The second dielectric end column is adjacent to another end of the length of the channel column and adjacent to the ferroelectric column in some embodiments.

[00215] In some embodiments, the integrated circuit further comprises a second vertical structure. The second vertical structure may be formed to be substantially identical to the first vertical structure, but disposed adjacent to the first vertical column at a predetermined horizontal distance.

[00216] In some embodiments, the integrated circuit may comprise a second vertical structure. The second vertical structure may be formed to be substantially identical to the first vertical structure, but disposed adjacent the first vertical column at a predetermined horizontal distance.

[00217] In some embodiments, the integrated circuit may comprise a first vertical structure and a second vertical structure, wherein the second vertical structure is formed to be substantially identical to the first vertical structure, but disposed adjacent the first vertical column at a predetermined horizontal distance. The first and second vertical structures may be configured to form a single-port 3D NAND structure.

[00218] Optionally, in some embodiments, the plurality of horizontal gate-electrode layers of the first vertical structure are formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide,

Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu , TiW , and Conducting Polymers.

[00219] In some embodiments, the ferroelectric column of the first vertical structure is formed from at least one of the following materials: Perovskites; Lead Zirconate Titanate (PZT); Barium Titanate (BaTiO_3); Strontium Titanate (SrTiO_3); Bismuth Ferrite (BiFeO_3); Potassium Niobate (KNbO_3); Lithium Niobate (LiNbO_3); Lithium Tantalate (LiTaO_3); Sodium Bismuth Titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$); Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$); Bismuth Zinc Niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$); Bismuth Lanthanum Titanate (BiLaTiO_3); Bismuth Nickel Titanate (BiNiTiO_3); Lead Magnesium Niobate-Lead Titanate (PMN-PT); Lead Lanthanum Zirconate Titanate (PLZT); Neodymium-doped Bismuth Titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$); Hafnium-based Oxides like Hafnium Oxide (HfO_2) and doped Hafnium Oxide including Zirconium-doped Hafnium Oxide (HfZrO_2); Tungsten Bronze Structure Materials such as Barium Strontium Niobate (BSN), Lead Barium Niobate (PBN), and Potassium Tantalate Niobate (KTN); Bismuth Layer-Structured Ferroelectrics including Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Strontium Bismuth Tantalate (SBT), and Calcium Bismuth Niobate (CBN); Organic Ferroelectrics like Polyvinylidene Fluoride (PVDF), TrFE (Trifluoroethylene), and P(VDF-TrFE) Copolymers; Aurivillius Phase Oxides; Rare Earth Manganites like YMnO_3 and Lanthanum-modified Lead Zirconate Titanate (PLZT); Relaxor Ferroelectrics such as Lead Magnesium Niobate (PMN), Lead Scandium Tantalate (PST), and Lead Indium Niobate (PIN); Multiferroic Materials like Terbium Manganite (TbMnO_3) and Europium Titanium Oxide (EuTiO_3); as well as Thin-Film Ferroelectrics, Layered Superlattices, and more. The extensive list provides flexibility in selecting suitable ferroelectric materials for the vertical structures in various embodiments.

[00220] In some embodiments, the channel column of the first vertical structure is formed from at least one of Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), Zinc Tin Oxide (ZTO), Aluminum Zinc Oxide (AZO), Indium Tungsten Oxide (IWO), Gallium Zinc Oxide (GZO), Hafnium Indium Oxide (HIO), Cadmium Oxide (CdO), Polysilicon, Polygermanium, Cadmium Selenide (CdSe), Copper Indium Gallium Selenide (CIGS), Crystalline Silicon (c-Silicon), Crystalline Germanium (c-Germanium), Gallium Arsenide (GaAs), Indium Phosphide (InP), Indium Antimonide (InSb), Silicon Carbide (SiC), Gallium Nitride (GaN), Zinc Oxide (ZnO), Pentacene, P3HT (Poly(3-hexylthiophene)), Polythiophene, Polyphenylene vinylene (PPV), Graphene, Carbon Nanotubes (CNTs), Methylammonium Lead Halides ($\text{CH}_3\text{NH}_3\text{PbX}_3$, $\text{X} = \text{Cl, Br, I}$), Cesium Lead Halide (CsPbX_3 , $\text{X} = \text{Cl, Br, I}$),

Lead Sulfide (PbS), Lead Selenide (PbSe), Cadmium Selenide (CdSe), Indium Arsenide (InAs), Skutterudites, Ruddlesden-Popper phases, Clathrates, Perovskite Oxides, or Magnetic Semiconductors.

[00221] In some embodiments, the dielectric column of the first vertical structure is formed from at least one of Hafnium Oxide (HfO₂), Zirconium Oxide (ZrO₂), Aluminum Oxide (Al₂O₃), Silicon Dioxide (SiO₂), Titanium Dioxide (TiO₂), Tantalum Oxide (Ta₂O₅), Lanthanum Oxide (La₂O₃), Yttrium Oxide (Y₂O₃), Silicon Nitride (Si₃N₄), Aluminum Nitride (AlN), Silicon Carbide (SiC), Strontium Titanate (SrTiO₃), Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), Bismuth Ferrite (BiFeO₃), Magnesium Oxide (MgO), Cerium Oxide (CeO₂), Nickel Oxide (NiO), Cobalt Oxide (CoO), Copper Oxide (CuO), Manganese Oxide (MnO), Zinc Oxide (ZnO), Gadolinium Oxide (Gd₂O₃), Dysprosium Oxide (Dy₂O₃), Samarium Oxide (Sm₂O₃), Europium Oxide (Eu₂O₃), Terbium Oxide (Tb₄O₇), Vanadium Oxide (V₂O₅), Niobium Oxide (Nb₂O₅), Chromium Oxide (Cr₂O₃), Iron Oxide (Fe₂O₃), Molybdenum Oxide (MoO₃), Tungsten Oxide (WO₃), Ruthenium Oxide (RuO₂), Rhodium Oxide (Rh₂O₃), Palladium Oxide (PdO), Silver Oxide (Ag₂O), Cadmium Oxide (CdO), Tin Oxide (SnO₂), Antimony Oxide (Sb₂O₃), Tellurium Oxide (TeO₂), Iridium Oxide (IrO₂), Platinum Oxide (PtO₂), Gold Oxide (Au₂O₃), Beryllium Oxide (BeO), Magnesium Aluminate (MgAl₂O₄), Zinc Selenide (ZnSe), Zinc Telluride (ZnTe), Cadmium Sulfide (CdS), Cadmium Selenide (CdSe), Cadmium Telluride (CdTe), Silicon Germanium Oxide (SiGeO_x), Bismuth Oxide (Bi₂O₃), Bismuth Titanate (Bi₄Ti₃O₁₂), Perovskite Oxides, Layered Oxides, or Complex Transition Metal Oxides.

[00222] In some embodiments, one of the plurality of horizontal gate-electrode layers and the first vertical structure may be configured to form a plurality of transistors. These transistors can include the first transistor as described herein. The first vertical structure comprises a dielectric column, a channel column disposed around the dielectric column, a ferroelectric column disposed around the channel column, and a plurality of horizontal gate-electrode layers disposed adjacent to the ferroelectric column.

[00223] In some embodiments, the integrated circuit may comprise a first vertical structure. The first vertical structure may comprise a pass-gate electrode column. A dielectric column may be disposed around the pass-gate electrode column. Optionally, a channel column may be disposed around the dielectric column. Additionally, a ferroelectric column may be disposed around the channel along a length of the channel column. The integrated circuit may further comprise a plurality of horizontal gate-electrode layers, where each layer is disposed a predetermined distance between each other. Each of the plurality of horizontal gate-electrode

layers may be disposed adjacent to the ferroelectric column along the length of the ferroelectric column.

[00224] In some embodiments, the integrated circuit may involve a pass-gate electrode column that is substantially cylindrical in form. This cylindrical pass-gate electrode column can optionally have a first diameter on one end and a second diameter on the other end, with the diameters either being the same or the first diameter larger than the second. The pass-gate electrode column may also be configured as either a solid column or a hollow column in different variants.

[00225] The integrated circuit may have a pass-gate electrode column that is substantially cylindrical, according to one embodiment. In some embodiments, this pass-gate electrode column has a first diameter on a first end and a second diameter on the second end. These first and second diameters may be the same or different in various embodiments, with the first diameter optionally being larger than the second diameter in some cases.

[00226] In some embodiments, the pass-gate electrode column of the first vertical structure is substantially cylindrical, with a first diameter on a first end and a second diameter on a second, opposite end. Optionally, the integrated circuit may be configured such that the first diameter and the second diameter of the pass-gate electrode column are the same.

[00227] In some embodiments, the pass-gate electrode column of the first vertical structure is substantially cylindrical, with a first diameter on a first end and a second diameter on the second end. Optionally, the first diameter of the pass-gate electrode column may be larger than the second diameter.

[00228] In some embodiments, the integrated circuit may comprise a pass-gate electrode column that is part of the first vertical structure. This pass-gate electrode column may be substantially cylindrical in form. Optionally, the pass-gate electrode column is solid rather than hollow.

[00229] In some embodiments, the integrated circuit may have a pass-gate electrode column that is hollow. Specifically, the pass-gate electrode column that is part of the first vertical structure and is disposed around the dielectric column and within the channel column, may be hollow rather than a solid column. Forming the pass-gate electrode column in a hollow configuration may provide certain advantages related to materials cost or processing simplicity.

[00230] In some embodiments, the integrated circuit may comprise a dielectric column that is substantially cylindrical in shape. This cylindrical dielectric column is disposed around a pass-gate electrode column as part of a first vertical structure. The diameter of the dielectric column may be uniform along its length or may vary from one end to the other.

[00231] In some embodiments, the dielectric column of the first vertical structure is substantially cylindrical. Optionally, the dielectric column may have a first diameter on a first end and a second diameter on the second end. The first and second diameters of the dielectric column may be configured to be the same or different in various embodiments.

[00232] In some embodiments, the dielectric column in the first vertical structure is substantially cylindrical, with a first diameter on a first end and a second diameter on the second end. The first and second diameters of the dielectric column may be configured to be the same.

[00233] The integrated circuit may comprise a dielectric column that is substantially cylindrical, wherein the dielectric column has a first diameter on a first end and a second diameter on the second end. In some embodiments, the first diameter of the dielectric column is larger than the second diameter.

[00234] In some embodiments, the integrated circuit may comprise a channel column that is substantially cylindrical in shape. The channel column is disposed around a dielectric column, which itself is disposed around a pass-gate electrode column. A ferroelectric column is disposed around the cylindrical channel column along the length of the channel column.

[00235] In some embodiments, the channel column formed around the dielectric column in the first vertical structure is substantially cylindrical in shape. The channel column may have a first diameter on a first end and a second diameter on a second, opposite end. The first and second diameters of the channel column may be the same or the first diameter may be larger than the second diameter.

[00236] In some embodiments, the channel column in the first vertical structure may have a substantially cylindrical shape with a uniform diameter along its entire length. Specifically, the channel column has a first diameter on a first end and a second diameter on a second, opposite end, wherein the first and second diameters are identical. This uniform cylindrical channel column runs parallel to the ferroelectric column and plurality of horizontal gate-electrode layers in the vertical structure.

[00237] In some embodiments, the integrated circuit may involve a channel column that is substantially cylindrical, wherein the channel column has a first diameter on a first end and a second diameter on the second end. Optionally, the first diameter of the channel column is configured to be larger than the second diameter.

[00238] In some embodiments, the integrated circuit may have a ferroelectric column that is substantially cylindrical in shape. The ferroelectric column is disposed around the channel column along the length of the channel column. The cylindrical ferroelectric column

optionally has a first diameter on a first end and a second diameter on the second end, where the diameters may be the same or the first diameter may be larger than the second diameter.

[00239] In some embodiments, the integrated circuit may comprise a ferroelectric column that is substantially cylindrical. The ferroelectric column may have a first diameter on a first end and a second diameter on the second end. Optionally, the first diameter and the second diameter can be the same or the first diameter can be larger than the second diameter.

[00240] In some embodiments, the ferroelectric column of the first vertical structure is substantially cylindrical, having a first diameter on a first end and a second diameter on the second end. Optionally, the first and second diameters of the ferroelectric column are configured to be the same.

[00241] In some embodiments, the integrated circuit may have a ferroelectric column that is substantially cylindrical, with a first diameter on a first end and a second diameter on the second end, where the first diameter is larger than the second diameter.

[00242] In some embodiments, the integrated circuit further comprises a dielectric end column disposed around an end of the channel column. This dielectric end column is adjacent to an end of the length of the channel column and also adjacent to the ferroelectric column.

[00243] In some embodiments, the integrated circuit further comprises a drain select layer disposed in parallel with the plurality of horizontal gate-electrode layers. The drain select layer is positioned adjacent to the dielectric end column surrounding an end of the channel column. The dielectric end column is adjacent to an end of the length of the channel column and adjacent to the ferroelectric column in the first vertical structure.

[00244] In some embodiments, the integrated circuit further comprises a second dielectric end column disposed around another end of the channel column. This second dielectric end column is adjacent to another end of the length of the channel column and also adjacent to the ferroelectric column.

[00245] In some embodiments, the integrated circuit further comprises a source select layer disposed in parallel with the plurality of horizontal gate-electrode layers and adjacent to the second dielectric end column surrounding the other end of the channel column. The source select layer is positioned adjacent to the end of the length of the channel column and the ferroelectric column.

[00246] In some embodiments, the integrated circuit further comprises a dielectric horizontal layer disposed within the channel column and adjacent to an end of the pass-gate electrode column. Specifically, a dielectric layer may be incorporated horizontally within the cylindrical channel column structure, positioned next to the end of the vertical pass-gate

electrode column. This dielectric isolation layer aids in delimiting the pass-gate region within the 3D NAND string.

[00247] The integrated circuit may comprise a second vertical structure in addition to the first vertical structure. The first vertical structure comprises a pass-gate electrode column, a dielectric column disposed around the pass-gate electrode column, a channel column disposed around the dielectric column, and a ferroelectric column disposed around the channel column along its length. Each of the plurality of horizontal gate-electrode layers is disposed a predetermined distance between each other and adjacent to the ferroelectric column. The second vertical structure may be formed substantially identically to the first vertical structure, but disposed horizontally adjacent to the first vertical structure at a predetermined distance.

[00248] The integrated circuit may comprise a second vertical structure in addition to the first vertical structure described previously. In some embodiments, this second vertical structure is formed to have substantially the same composition and dimensions as the first vertical structure. However, the second structure is disposed horizontally adjacent to the first vertical structure at a predetermined distance between them. Configuring two identical vertical structures in this parallel arrangement enables certain circuit configurations such as forming a dual-port 3D NAND structure with the paired vertical structures.

[00249] The integrated circuit may comprise first and second vertical structures, wherein the second vertical structure is formed to be substantially identical to the first vertical structure, but disposed adjacent to the first vertical column at a predetermined horizontal distance. In some embodiments, these first and second vertical structures are configured to form a dual-port 3D NAND structure.

[00250] In some embodiments, the plurality of horizontal gate-electrode layers of the first vertical structure may be formed from at least one conductive material selected from a group consisting of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides such as TiSi₂, CoSi₂, and NiSi, Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys such as AlCu and TiW, and Conducting Polymers.

[00251] In some embodiments, the pass-gate electrode column of the first vertical structure is formed from at least one of the following materials: Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide,

Silicides such as TiSi_2 , CoSi_2 , and NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys such as AlCu and TiW , and Conducting Polymers. The pass-gate electrode column may be constructed using one or more of these conductive materials.

[00252] In some embodiments, the ferroelectric column of the first vertical structure is formed from at least one of the following ferroelectric materials: Perovskites; Lead Zirconate Titanate (PZT); Barium Titanate (BaTiO_3); Strontium Titanate (SrTiO_3); Bismuth Ferrite (BiFeO_3); Potassium Niobate (KNbO_3); Lithium Niobate (LiNbO_3); Lithium Tantalate (LiTaO_3); Sodium Bismuth Titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$); Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$); Bismuth Zinc Niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$); Bismuth Lanthanum Titanate (BiLaTiO_3); Bismuth Nickel Titanate (BiNiTiO_3); Lead Magnesium Niobate-Lead Titanate (PMN-PT); Lead Lanthanum Zirconate Titanate (PLZT); Neodymium-doped Bismuth Titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$); Hafnium-based Oxides; Hafnium Oxide (HfO_2); Doped Hafnium Oxide; Zirconium-doped Hafnium Oxide (HfZrO_2); Tungsten Bronze Structure Materials; Barium Strontium Niobate (BSN); Lead Barium Niobate (PBN); Potassium Tantalate Niobate (KTN); Bismuth Layer-Structured Ferroelectrics; Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$); Strontium Bismuth Tantalate (SBT); Calcium Bismuth Niobate (CBN); Organic Ferroelectrics; Polyvinylidene Fluoride (PVDF); TrFE (Trifluoroethylene); P(VDF-TrFE) Copolymers; Aurivillius Phase Oxides; Rare Earth Manganites; YMnO_3 ; Lanthanum-modified Lead Zirconate Titanate (PLZT); Nickel Manganese Oxide (NiMnO_3); Relaxor Ferroelectrics; Lead Magnesium Niobate (PMN); Lead Scandium Tantalate (PST); Lead Indium Niobate (PIN); Multiferroic Materials; Terbium Manganite (TbMnO_3); Europium Titanium Oxide (EuTiO_3); SbSI (Antimony Sulfoiodide); GeTe (Germanium Telluride); SnTe (Tin Telluride); Thin-Film Ferroelectrics; PZT Thin Films; SBT Thin Films; HfO_2 -based Thin Films; Layered Superlattices; or $\text{PbTiO}_3/\text{SrTiO}_3$.

[00253] In some embodiments, the channel column of the first vertical structure is formed from at least one of the following materials: Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), Zinc Tin Oxide (ZTO), Aluminum Zinc Oxide (AZO), Indium Tungsten Oxide (IWO), Gallium Zinc Oxide (GZO), Hafnium Indium Oxide (HIO), Cadmium Oxide (CdO), Polysilicon, Polygermanium, Cadmium Selenide (CdSe), Copper Indium Gallium Selenide (CIGS), Crystalline Silicon (c-Silicon), Crystalline Germanium (c-Germanium), Gallium Arsenide (GaAs), Indium Phosphide (InP), Indium Antimonide (InSb), Silicon Carbide (SiC), Gallium Nitride (GaN), Zinc Oxide (ZnO), Pentacene, P3HT (Poly(3-hexylthiophene)), Polythiophene, Polyphenylene vinylene (PPV), Graphene, Carbon

Nanotubes (CNTs), Methylammonium Lead Halides ($\text{CH}_3\text{NH}_3\text{PbX}_3$, $\text{X} = \text{Cl, Br, I}$), Cesium Lead Halide (CsPbX_3 , $\text{X} = \text{Cl, Br, I}$), Lead Sulfide (PbS), Lead Selenide (PbSe), Cadmium Selenide (CdSe), Indium Arsenide (InAs), Skutterudites, Ruddlesden-Popper phases, Clathrates, Perovskite Oxides, and Magnetic Semiconductors. The selection of channel column material can influence characteristics such as electron mobility, switching speed, power consumption, etc.

[00254] In some embodiments, the dielectric column described herein is formed from at least one of Hafnium Oxide (HfO_2), Zirconium Oxide (ZrO_2), Aluminum Oxide (Al_2O_3), Silicon Dioxide (SiO_2), Titanium Dioxide (TiO_2), Tantalum Oxide (Ta_2O_5), Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3), Silicon Nitride (Si_3N_4), Aluminum Nitride (AlN), Silicon Carbide (SiC), Strontium Titanate (SrTiO_3), Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), Bismuth Ferrite (BiFeO_3), Magnesium Oxide (MgO), Cerium Oxide (CeO_2), Nickel Oxide (NiO), Cobalt Oxide (CoO), Copper Oxide (CuO), Manganese Oxide (MnO), Zinc Oxide (ZnO), Gadolinium Oxide (Gd_2O_3), Dysprosium Oxide (Dy_2O_3), Samarium Oxide (Sm_2O_3), Europium Oxide (Eu_2O_3), Terbium Oxide (Tb_4O_7), Vanadium Oxide (V_2O_5), Niobium Oxide (Nb_2O_5), Chromium Oxide (Cr_2O_3), Iron Oxide (Fe_2O_3), Molybdenum Oxide (MoO_3), Tungsten Oxide (WO_3), Ruthenium Oxide (RuO_2), Rhodium Oxide (Rh_2O_3), Palladium Oxide (PdO), Silver Oxide (Ag_2O), Cadmium Oxide (CdO), Tin Oxide (SnO_2), Antimony Oxide (Sb_2O_3), Tellurium Oxide (TeO_2), Iridium Oxide (IrO_2), Platinum Oxide (PtO_2), Gold Oxide (Au_2O_3), Beryllium Oxide (BeO), Magnesium Aluminate (MgAl_2O_4), Zinc Selenide (ZnSe), Zinc Telluride (ZnTe), Cadmium Sulfide (CdS), Cadmium Selenide (CdSe), Cadmium Telluride (CdTe), Silicon Germanium Oxide (SiGeO_x), Bismuth Oxide (Bi_2O_3), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Perovskite Oxides, Layered Oxides, or Complex Transition Metal Oxides.

[00255] In some embodiments, one of the plurality of horizontal gate-electrode layers and the first vertical structure may be configured to form a plurality of transistors. These transistors can include the first transistor as described herein. Specifically, the first vertical structure comprises a pass-gate electrode column, a dielectric column disposed around the pass-gate electrode column, a channel column disposed around the dielectric column, and a ferroelectric column disposed around the channel column along its length. The plurality of horizontal gate-electrode layers are each disposed a predetermined distance between one another and adjacent to the ferroelectric column along its length. Together, one of these horizontal gate-electrode layers and the first vertical structure form the plurality of transistors, which can include the first transistor with the configuration set forth herein.

[00256] In some embodiments, the integrated circuit comprises a first vertical structure. This vertical structure may involve a vertical plug column. Adjacent to this vertical plug column, there may be disposed a source electrode column and a drain electrode column. A channel column may be disposed around the vertical plug column, the source electrode column, and the drain electrode column. Additionally, a ferroelectric column may be disposed around this channel column. The integrated circuit may also involve a plurality of horizontal gate-electrode layers, each disposed a predetermined distance apart from each other. These horizontal gate-electrode layers may each be disposed adjacent to the ferroelectric column along its length.

[00257] In some embodiments, the integrated circuit further comprises an Oxide/Nitride/Oxide stack disposed adjacent to each of the plurality of horizontal gate-electrode layers. The Oxide/Nitride/Oxide stack may provide electrical isolation between the gate-electrode layers while enabling the layers to control channel formation in the vertical channel column structure.

[00258] In some embodiments, the integrated circuit's vertical plug column has a first diameter on a first end and a second diameter on the second end. The first and second diameters may be the same or different.

[00259] In some embodiments, the vertical plug column of the first vertical structure has a first diameter on a first end and a second diameter on a second end. The first and second diameters may be configured to be the same.

[00260] In some embodiments, the vertical plug column in the first vertical structure has a first diameter on a first end and a second diameter on the second end, where the first diameter is larger than the second diameter.

[00261] In some embodiments, the vertical plug column of the first vertical structure is configured to be solid rather than hollow. Specifically, the vertical plug column has a continuous material filling rather than being an empty conduit. Forming the vertical plug column in a solid configuration may provide certain advantages for the overall integrated circuit structure related to simplicity of fabrication or integrity of adjacent components. However, other embodiments may utilize a hollow configuration for the vertical plug column depending on the specific design considerations.

[00262] In some embodiments, the integrated circuit may have a vertical plug column that is hollow. Specifically, the vertical plug column that is disposed adjacent to the source electrode column and the drain electrode column in the first vertical structure may be hollow

rather than solid. Forming a hollow vertical plug column structure enables additional design flexibility.

[00263] In some embodiments, the integrated circuit further comprises a second vertical structure. The second vertical structure may be formed to be substantially identical to the first vertical structure, but disposed adjacent to the first vertical structure at a predetermined horizontal distance. In certain embodiments, the first and second vertical structures can be configured to form a 3D AND-structure or a 3D NOR-structure.

[00264] In some embodiments, the integrated circuit further comprises a second vertical structure. The second vertical structure may be formed to be substantially identical to the first vertical structure, but disposed adjacent to the first vertical structure at a predetermined horizontal distance.

[00265] In some embodiments, the integrated circuit may comprise a first vertical structure and a second vertical structure, wherein the second vertical structure is formed to be substantially identical to the first vertical structure but disposed adjacent to the first vertical structure at a predetermined horizontal distance. The first and second vertical structures may be configured to form a 3D AND-structure.

[00266] In some embodiments, the integrated circuit may comprise a first vertical structure and a second vertical structure, wherein the second vertical structure is formed to be substantially identical to the first vertical structure but disposed adjacent to the first vertical structure at a predetermined horizontal distance. The first and second vertical structures may be configured to form a 3D NOR-structure.

[00267] In some embodiments, the plurality of horizontal gate-electrode layers of the first vertical structure may be formed from at least one material selected from a group consisting of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides such as TiSi₂, CoSi₂, NiSi, Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys such as AlCu and TiW, and Conducting Polymers.

[00268] In some embodiments, the source electrode column of the first vertical structure is formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi₂, CoSi₂, NiSi, Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped

Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys such as AlCu and TiW, and Conducting Polymers.

[00269] In some embodiments, the integrated circuit further comprises a gate electrode column formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides such as TiSi₂, CoSi₂, NiSi, Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys such as AlCu and TiW, and Conducting Polymers.

[00270] In some embodiments, the ferroelectric column of the first vertical structure is formed from at least one of Perovskites, Lead Zirconate Titanate (PZT), Barium Titanate (BaTiO₃), Strontium Titanate (SrTiO₃), Bismuth Ferrite (BiFeO₃), Potassium Niobate (KNbO₃), Lithium Niobate (LiNbO₃), Lithium Tantalate (LiTaO₃), Sodium Bismuth Titanate (Na_{0.5}Bi_{0.5}TiO₃), Bismuth Titanate (Bi₄Ti₃O₁₂), Bismuth Zinc Niobate (Bi(Zn_{1/2}Ti_{1/2})O₃), Bismuth Lanthanum Titanate (BiLaTiO₃), Bismuth Nickel Titanate (BiNiTiO₃), Lead Magnesium Niobate-Lead Titanate (PMN-PT), Lead Lanthanum Zirconate Titanate (PLZT), Neodymium-doped Bismuth Titanate (Bi_{4-x}Nd_xTi₃O₁₂), Hafnium-based Oxides, Hafnium Oxide (HfO₂), Doped Hafnium Oxide, Zirconium-doped Hafnium Oxide (HfZrO₂), Tungsten Bronze Structure Materials, Barium Strontium Niobate (BSN), Lead Barium Niobate (PBN), Potassium Tantalate Niobate (KTN), Bismuth Layer-Structured Ferroelectrics, Bismuth Titanate (Bi₄Ti₃O₁₂), Strontium Bismuth Tantalate (SBT), Calcium Bismuth Niobate (CBN), Organic Ferroelectrics, Polyvinylidene Fluoride (PVDF), TrFE (Trifluoroethylene), P(VDF-TrFE) Copolymers, Aurivillius Phase Oxides, Rare Earth Manganites, YMnO₃, Lanthanum-modified Lead Zirconate Titanate (PLZT), Nickel Manganese Oxide (NiMnO₃), Relaxor Ferroelectrics, Lead Magnesium Niobate (PMN), Lead Scandium Tantalate (PST), Lead Indium Niobate (PIN), Multiferroic Materials, Terbium Manganite (TbMnO₃), Europium Titanium Oxide (EuTiO₃), SbSI (Antimony Sulfoiodide), GeTe (Germanium Telluride), SnTe (Tin Telluride), Thin-Film Ferroelectrics, PZT Thin Films, SBT Thin Films, HfO₂-based Thin Films, Layered Superlattices, and PbTiO₃/SrTiO₃.

[00271] In some embodiments, the channel column of the first vertical structure is formed from at least one of Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), Zinc Tin Oxide (ZTO), Aluminum Zinc Oxide (AZO), Indium Tungsten Oxide (IWO), Gallium Zinc Oxide (GZO), Hafnium Indium Oxide (HIO), and Cadmium Oxide (CdO), Polysilicon, Polygermanium, Cadmium Selenide (CdSe), Copper Indium Gallium Selenide (CIGS),

Crystalline Silicon (c-Silicon), Crystalline Germanium (c-Germanium), Gallium Arsenide (GaAs), Indium Phosphide (InP), Indium Antimonide (InSb), Silicon Carbide (SiC), Gallium Nitride (GaN), Zinc Oxide (ZnO), Pentacene, P3HT (Poly(3-hexylthiophene)), Polythiophene, Polyphenylene vinylene (PPV), Graphene, Carbon Nanotubes (CNTs), Methylammonium Lead Halides ($\text{CH}_3\text{NH}_3\text{PbX}_3$, $\text{X} = \text{Cl, Br, I}$), Cesium Lead Halide (CsPbX_3 , $\text{X} = \text{Cl, Br, I}$), Lead Sulfide (PbS), Lead Selenide (PbSe), Cadmium Selenide (CdSe), Indium Arsenide (InAs), Skutterudites, Ruddlesden-Popper phases, Clathrates, Perovskite Oxides, and Magnetic Semiconductors.

[00272] In some embodiments, the vertical plug column of the first vertical structure is formed from at least one of Hafnium Oxide (HfO_2), Zirconium Oxide (ZrO_2), Aluminum Oxide (Al_2O_3), Silicon Dioxide (SiO_2), Titanium Dioxide (TiO_2), Tantalum Oxide (Ta_2O_5), Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3), Silicon Nitride (Si_3N_4), Aluminum Nitride (AlN), Silicon Carbide (SiC), Strontium Titanate (SrTiO_3), Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), Bismuth Ferrite (BiFeO_3), Magnesium Oxide (MgO), Cerium Oxide (CeO_2), Nickel Oxide (NiO), Cobalt Oxide (CoO), Copper Oxide (CuO), Manganese Oxide (MnO), Zinc Oxide (ZnO), Gadolinium Oxide (Gd_2O_3), Dysprosium Oxide (Dy_2O_3), Samarium Oxide (Sm_2O_3), Europium Oxide (Eu_2O_3), Terbium Oxide (Tb_4O_7), Vanadium Oxide (V_2O_5), Niobium Oxide (Nb_2O_5), Chromium Oxide (Cr_2O_3), Iron Oxide (Fe_2O_3), Molybdenum Oxide (MoO_3), Tungsten Oxide (WO_3), Ruthenium Oxide (RuO_2), Rhodium Oxide (Rh_2O_3), Palladium Oxide (PdO), Silver Oxide (Ag_2O), Cadmium Oxide (CdO), Tin Oxide (SnO_2), Antimony Oxide (Sb_2O_3), Tellurium Oxide (TeO_2), Iridium Oxide (IrO_2), Platinum Oxide (PtO_2), Gold Oxide (Au_2O_3), Beryllium Oxide (BeO), Magnesium Aluminate (MgAl_2O_4), Zinc Selenide (ZnSe), Zinc Telluride (ZnTe), Cadmium Sulfide (CdS), Cadmium Selenide (CdSe), Cadmium Telluride (CdTe), Silicon Germanium Oxide (SiGeO_x), Bismuth Oxide (Bi_2O_3), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Perovskite Oxides, Layered Oxides, or Complex Transition Metal Oxides.

[00273] In some embodiments, the integrated circuit may comprise a plurality of transistors formed from one of the horizontal gate-electrode layers and the first vertical structure according to any of the transistors described herein. The first vertical structure may include components such as a vertical plug column, source and drain electrode columns, a channel column, and a ferroelectric column. The horizontal gate-electrode layers may be disposed at predetermined distances from one another adjacent to the ferroelectric column. Configuring a horizontal gate-electrode layer and the first vertical structure in this manner allows for the formation of transistors with properties such as those described herein.

[00274] BRIEF DESCRIPTION OF THE DRAWINGS

[00275] These and other aspects will become more apparent from the following detailed description of the various embodiments of the present disclosure with reference to the drawings wherein:

[00276] Fig. 1 is a block diagram of an integrated circuit that may be part of a semiconductor device such as a chiplet in accordance with an embodiment of the present disclosure;

[00277] Fig. 2 shows a perspective view of an assembly having the integrated circuit of Fig. 1 implemented on a semiconductor device that is electrically connected to another device to form the assembly in accordance with an embodiment of the present disclosure;

[00278] Fig. 3 shows a block diagram illustrating the memory address space of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure;

[00279] Fig. 4 shows a block diagram illustrating the memory address space with the signal interfaces of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure;

[00280] Fig. 5 shows an illustration of an integrated circuit that may be part of a semiconductor device such as a chiplet in accordance with an embodiment of the present disclosure;

[00281] Fig. 6 shows a perspective of an assembly having the integrated circuit of Fig. 1 implemented on a semiconductor device that is electrically connected to a system-on-a-chip in accordance with an embodiment of the present disclosure;

[00282] Fig. 7 shows a perspective view of an assembly having a semiconductor device with an array of processing elements and a second semiconductor device having an array of microvaults;

[00283] Fig. 8 shows an assembly of a semiconductor devices including several memory types in accordance with an embodiment of the present disclosure;

[00284] Fig. 9 shows an assembly of semiconductor devices including a semiconductor device with a system-on-chip and another semiconductor with microvaults disposed on top in accordance with an embodiment of the present disclosure;

[00285] Fig. 10 shows a semiconductor assembly incorporating a daisy-chained configuration of microvaults operatively connected to a multiplexer and managed by a counter for coordinated data selection and retrieval, in accordance with an embodiment of the present disclosure.

[00286] Fig. 11 shows a semiconductor assembly incorporating a daisy-chained configuration of microvaults in multiple semiconductor devices that are operatively connected to multiplexers and managed by counters for coordinated data selection and retrieval, in accordance with an embodiment of the present disclosure;

[00287] Fig. 12 illustrates a three-dimensional (3D) memory column configured as a 3D-NOR or 3D-AND structure, featuring a series of ferroelectric field-effect transistors (FeFETs) with interconnected drain terminals linked to a common select line and individual gate terminals connected to respective read/write enable lines, all coupled to a common bit line, in accordance with an embodiment of the present disclosure;

[00288] Fig. 13 depicts a three-dimensional (3D) memory column configured as a 3D-NAND structure, consisting of a vertical stack of ferroelectric field-effect transistors (FeFETs), in accordance with an embodiment of the present disclosure;

[00289] Fig. 14 depicts a three-dimensional (3D) memory column configured as a 3D-NAND with an integrated pass gate, in accordance with an embodiment of the present disclosure;

[00290] Fig. 15 illustrates a three-dimensional (3D) memory column 1500, which may be configured as either a 3D-NOR or a 3D-AND structure with independent Read/Write enable capabilities, in accordance with an embodiment of the present disclosure;

[00291] Fig. 16 shows a cross-sectional view of a 3D memory structure configured as a single-port 3D NAND, in accordance with an embodiment of the present disclosure;

[00292] Fig. 17 shows a cross-sectional view of a 3D memory structure that is a dual-port 3D NAND arrangement, in accordance with an embodiment of the present disclosure;

[00293] Fig. 18 illustrates a 3D memory structure that can be configured as a 3D NOR Vertical Transistor memory array, in accordance with an embodiment of the present disclosure;

[00294] Fig. 19 shows a planar FeFET in accordance with an embodiment of the present disclosure; and

[00295] Fig. 20 shows electrical characteristics of an embodiment of a FeFET in accordance with an embodiment of the present disclosure.

[00296] **DETAILED DESCRIPTION**

[00297] Fig. 1 shows a block diagram of an integrated circuit 100 that may be packaged as a bondable chiplet (e.g., face-to-face chiplet bondable) in accordance with an embodiment of the present disclosure. The integrated circuit (IC) 100 includes a modules group 106 consisting of modules 108, 110, 112, and 114. The IC 100 also features a shared write port 102, configured to write to the modules group 106 using a write peripheral 104. Additionally, it

includes read peripherals 116, 118, 120, and 122 and read ports 124, 126, 128, and 130, configured to read from the modules 108, 110, 112, 114.

[00298] The write port 102 may be configured to provide a single write address space for all of the modules group 106 where each of the modules 108, 110, 112, 114 has a dedicated read port 124, 126, 128, 130 respectively. The integrated circuit 100 may be packaged as part of a chiplet configured to be electrically connected to another integrated circuit device (e.g., another chiplet, or IC package, with or without electrical contacts, electrical bumps, etc.). The chiplet may be electrically connected to another device including, for example, by bonding, soldering, wafer-to-wafer bonding, face-to-face chiplet bonding, chiplet-to-wafer bonding, chiplet-to-interposer bonding, and/or may be connected together with an interposer or other interfacing technology. None, one, or more of interposers may be used or other interfacing technologies that are common to heterogeneous 3D system-in-package solutions may be utilized in electrically connecting a chiplet to another device.

[00299] Each read port (124, 126, 128, 130) in the chiplet may feature electrical contacts on a side of the chiplet or on multiple sides of the chiplet. The read ports 124, 126, 128, 130 may use multi-cycle pipelined circuitry. Upon bonding to another device (e.g., wafer, chiplet, chip, SOC, package, FPGA, etc.), the electrical contacts may line up in a manner that provides dedicated access to specific modules of the modules 108, 110, 112, 114. For instance, a processing/computing element may have exclusive access to module 108 via the read port 124, which may contain the neural network weights in a register file. Similarly, a different processing/computing element may have exclusive read access to module 110 via the read port 126, which includes a different register file. In this specific embodiment, this arrangement of the electrical contacts ensures that each computing/processing element has the dedicated access it needs to carry out its specific computation efficiently thereby providing a compact, modular, and scalable system that allows different processing elements to maintain dedicated access to specific modules 108, 110, 112, 114. Without dedicated access, different processing elements might have to queue up to use the same resource which would slow down overall processing speed. By providing dedicated access, the proposed chiplet ensures that each processing element can operate at its maximum capability without interference from other computing elements in this specific embodiment.

[00300] The write peripheral 104 is a peripheral circuitry responsible for processing and writing data into the memory cells found within the modules 108, 110, 112, 114. The write peripheral 104 may include dedicated contacts so that a chip electrically connected (e.g., bonded) to a chiplet of the integrated circuit, such that the write port 102 is accessible via a

shared write logic system that involves utilizing a shift register-based, different voltage design, preferably high voltage design, that has a shared write address and data components. This shared write logic system is designed to be accessed via a bonded chip, another bonded chiplet, and/or via other circuitry in the same package as the integrated circuit 100. A shift register could allow the system to move data through a series of stages, with each subsequent stage receiving the data from the previous stage. By utilizing a shift register, the system can increase the data throughput while maintaining a low rate of data transfers. The shared write address space refers to the location where data is written in the chiplet.

[00301] In another embodiment, an interlock 132 may disable the read ports 124, 126, 128, 130 while data is being written to the modules group 106 via the write port 102. Likewise, the interlock 132 may disable the write port 102 when read operations are being carried out on the read ports 124, 126, 128, 130. The written data can later be accessed concurrently by all processing elements that need to read the data via a respective one of the read ports 124, 126, 128, 130. This ensures that all processing elements have the most commonly used data available to them without regard to other reads being concurrently carried out by other processing elements.

[00302] The write peripheral 104 circuit includes a write driver. This unit receives the data to be written and converts it into suitable signals that can change the state of the memory cells. Depending on the type of memory technology used, these signals could involve voltage levels, current pulses, or other types of energy. The shared write logic system may be high voltage due to the specific voltage requirements of the chiplet. The write driver must provide enough power to reliably change the state of the memory cells, but it must also operate within suitable parameters to avoid causing damage or unnecessary wear.

[00303] The write peripheral 104 circuit may also feature a data buffer or write buffer. This component temporarily stores the data to be written, allowing the write operation to be performed at an optimal pace. By balancing the speed of incoming data with the speed at which the memory cells can be written, the write buffer helps prevent data loss and optimizes system performance.

[00304] The write peripheral 104 may also include, in some embodiment, a write control unit that orchestrates the sequence of operations in the write process. It generates control signals to activate the write driver at the appropriate times, controls the flow of data from the write buffer, and coordinates the timing of the write operations. By synchronizing these various activities, the write control unit ensures efficient and reliable write operations.

[00305] The write peripheral 104 may also include data encoding mechanisms to improve reliability and data integrity. For example, before the data is written to the memory cells, these mechanisms encode it in a way that allows potential errors to be detected, and in some cases, corrected when the data is later read. This can be helpful in systems where data integrity has a higher priority, such as in servers or scientific research devices.

[00306] The write peripheral 104 may also include a timing unit that serves as the system's heartbeat, supplying clock signals that synchronize the operation of the system's various components. In some systems, it may include components like oscillators, clock generators, or phase-locked loops. The timing unit may ensure that all operations occur at the suitable time relative to each other.

[00307] The IC 100 may be implemented as a face-to-face bonded chiplet, with modules 108, 110, 112, and 114 formed from a non-volatile memory. In some specific embodiments, the IC 100 may also feature a dynamic allocation circuitry to allocate memory blocks to the modules group 106 based on the usage of the modules group 106 (e.g., each module 108 may include dynamic allocation circuitry for dynamically allocating a range of read locations for a respective processing element).

[00308] The IC 100 features a plurality of clocks, with each clock of the plurality of clocks feeding a respective module of the plurality of modules, providing each respective module with decoupled timing relative to the other modules of the plurality of modules. The modules group 106 may be arranged in any topology known to one of ordinary skill in the relevant art. Bit-cell density can be up to 10 times more dense than embedded SRAM cells in the modules group 106.

[00309] The IC 100 may be formed on a chiplet that includes a first side and a second side, with the second side configured for bonding to a second semiconductor device. The IC 100 may include a high voltage write logic adjacent to the first side of the chiplet. A decoder circuitry, a driver circuitry, and a register circuitry may be formed on the silicon substrate portion of the chiplet, while the modules group 106 is formed on a second layer portion of the chiplet. The second semiconductor device may comprise a plurality of processing elements. Each processing element includes a respective interface to communicate with a respective module of the plurality of modules on the modules group 106 when the second semiconductor device is bonded to the chiplet.

[00310] The silicon substrate traditionally serves as the initial stage of IC fabrication, focusing on the creation of active components, particularly transistors. Techniques like diffusion, ion implantation, oxidation, and material deposition are employed to fashion the

intricate structures of transistors. These processes operate at small scales. The application of photolithography, etching, and implantation techniques enables the definition of transistor structures with precision. The silicon substrate's significance lies in its ability to establish the fundamental building blocks necessary for signal processing, amplification, and control within the IC. This layer is sometimes called Front-End-Of-The-Line ("FEOL").

[00311] Next in the manufacturing process, a second layer may be added that traditionally takes on the role of interconnect fabrication, facilitating the electrical connections between various IC components. This phase traditionally focused on the creation of passive components, including interconnects, vias, and metal-insulator-metal (MIM) capacitors. The second layer processes typically differ from the processes used on the silicon substrate in terms of precision and scale. The interconnects are formed by depositing and patterning metal layers, typically aluminum or copper, to construct the wiring network. Dielectric layers, such as silicon dioxide or low-k dielectrics, are introduced to insulate the interconnects and prevent signal interference between different wiring layers. The second layer's traditional function is to establish the necessary interconnections that enable the routing and distribution of electrical signals throughout the IC. However, as described herein, circuitry may be utilized within this second layer (sometimes referred to as Back-End-Of-The-Line ("BEOL")).

[00312] Alternate embodiments of the IC 100 may be implemented as a stacked die, a monolithic design, TSVs, or silicon through vias. In a stacked die design, several dies may be stacked on top of each other, with each die performing different functions, such as memory and processing. The stacked die may communicate through wire bonds, microbumps, or bump-less bonds. In a monolithic design, the various functions and modules of the IC 100 may be integrated onto a single die, forming a more compact and power-efficient design.

[00313] Additionally, the IC 100 may include one or more interlocks 132 to prevent conflicts in reading and writing data. The modules group 106 may be formed from a variety of non-volatile or semi-volatile (e.g., very long refresh periods) memory technologies, such as Static Random-Access Memory (SRAM), Ferroelectric Field Effect Transistor (FeFET), Ferroelectric Random Access Memory (FeRAM), Resistive Random Access Memory (ReRAM), Spin-Orbit Torque (SOT) Memory, Spin Transfer Torque (STT) Memory, charge trap, floating gate memories, and/or Schottky diodes.

[00314] The modules group 106 may utilize a Static Random-Access Memory (SRAM) Topology. The SRAM topology may employ a cross-coupled flip-flop structure (e.g., latching flip-flops), ensuring the stored data remains intact as long as power is supplied. Thus, in some

specific embodiments, the modules group 106 may utilize heterogeneous types of memory including volatile and non-volatile memory types.

[00315] The modules group 106 may utilize a Flash Memory Topology. The Flash memory is a non-volatile memory technology used in applications where data persistence is needed, such as solid-state drives (SSDs) and USB flash drives. The flash memory topology disclosed herein features a matrix of memory cells, each consisting of a floating-gate transistor or charge trap device. The modules group 106 may also use wear-leveling techniques to prolong the lifespan of the memory cells.

[00316] The modules group 106 may utilize a Ferroelectric Random-Access Memory (FeRAM) Topology. The FeRAM topology utilizes a ferroelectric material capable of retaining polarization states. One such memory topology may, in specific embodiments, utilize a FeFET to retain state information and program the ferroelectric material. These ferroelectric materials may be used to retain state information and act as a memory bit cell.

[00317] The modules group 106 may utilize a Phase Change Memory (PCM) Topology, which is a non-volatile memory technology that utilizes reversible phase changes in materials to store data. The PCM topology may include any phase change material, for example a chalcogenide alloy or a chalcogenide glass housed within a memory cell.

[00318] The modules group 106 may utilize a Resistive Random-Access Memory (ReRAM) Topology, which is a non-volatile memory technology based on resistive switching phenomena. The ReRAM topology may utilize a thin-film material that exhibits reversible changes in resistance upon the application of electrical stimuli.

[00319] The modules group 106 may utilize a Spin-Orbit Torque (SOT) Magnetic Random-Access Memory Topology. SOT-MRAM is a type of non-volatile memory that utilizes spin-orbit torque to switch the magnetic state of a storage element. The SOT-MRAM topology may incorporate a magnetic tunnel junction (MTJ) structure and leverages the spin-orbit coupling effect to write and read data. The magnetic tunnel junction may have a dielectric layer between a magnetic fixed layer and a magnetic free layer. Writing may be done by switching magnetization of the free magnetic layer by injecting an in-plane current in an adjacent SOT layer. Reading may be done by putting current into the magnetic tunnel junction. The SOT-MRAM can optimize the spin-orbit materials by using current-driven switching schemes while minimizing write energy consumption, in some specific embodiments.

[00320] The modules group 106 may utilize a Spin Transfer Torque (STT) Magnetic Random-Access Memory Topology. The STT-MRAM is another type of non-volatile memory that relies on spin transfer torque to manipulate the magnetic state of a storage element. The

STT-MRAM topology can use a magnetic tunnel junction (MTJ) structure, where the magnetization orientation determines the stored data. Additionally, the orientation of a magnetic layer in a magnetic tunnel junction or spin valve can be changed using a spin-polarized current, for example.

[00321] The IC 100 may include a single write peripheral 104 with a dedicated clock, or each module 108, 110, 112, 114 may have its own dedicated write peripheral utilizing a shared clock (not shown in Fig. 1). Additionally, the modules group 106 may be organized into separate partitions, each with a dedicated read peripheral 116, 118, 120, 122 having an independent clock.

[00322] Another possible embodiment of the IC 100 includes an interface (e.g., the same, different, higher or lower voltage) to enable data transfer external to the packaging of the IC 100. The IC 100 may also include an integrated microcontroller unit (MCU) or a digital signal processor (DSP) for processing data within the IC in yet additional specific embodiments.

[00323] Fig. 2 shows a perspective view an assembly 200 of the integrated circuit 212 of Fig. 1 implemented on a chiplet 230 that is bonded to a second device 226 in accordance with an embodiment of the present disclosure. The integrated circuit 212 is the circuitry within the chiplet 230. The second device 226 may be a chiplet, semiconductor wafer, semiconductor package, encased circuitry, etc. For example, the second device 226 may be an AI accelerator such that each processing unit has read access to one module (or a predetermined set) of the modules group 236. In yet another embodiment, the second device 226 may be a network controller where there is an offload circuit to read the data from each of the modules to processing incoming/outgoing packets, etc. The assembly 200 includes a modules group 236 having a plurality of modules, including a first module 232 and a second module 234. Fig. 2 shows several modules, however, for clarity, only modules 232, 234 have reference numbers. The integrated circuit 212 further comprises a shared write port 222. The shared write port 222 interfaces into the write peripheral 202.

[00324] Although the second device 226 may use the shared write port 222 via an address & data bus with a clock and a enable signal to write data to any modules within the modules group 236, other ways of writing data may be considered. For example, serial connections, parallel connections, various buses, or ports, may be used, such as a DDR (Double Data Rate) Interface, a SRAM (Static Random-Access Memory) Interface, a NAND Flash Memory Interface, a NOR Flash Memory Interface, a HBM (High Bandwidth Memory) Interface, a GDDR (Graphics Double Data Rate) Interface, a NVMe (Non-Volatile Memory

Express) Interface, SPI, IC2, etc. Each of the modules has a read port with a read address 218 (to send an address to a module 234) and read data 214 (which is the data read from the module 232).

[00325] The modules group 236 is formed on a chiplet 230 having two sides including a surface 228 that can be bonded to and complement a second device 226. The chiplet 230 may be formed by forming circuitry on a silicon substrate 204 and then by adding a second layer 206. In other embodiments, these layers may be reversed and/or other layers may be added, removed, etc. The read address 218 and read data 220 are used for reading the module 232.

[00326] Although the second device 226 may use an address & data bus with a clock and an enable signal to read data from the module 232, other ways of reading data may be considered. For example, serial connections, parallel connections, various buses, or ports, may be used, such as a DDR (Double Data Rate) Interface, a SRAM (Static Random-Access Memory) Interface, a NAND Flash Memory Interface, a NOR Flash Memory Interface, a HBM (High Bandwidth Memory) Interface, a GDDR (Graphics Double Data Rate) Interface, a NVMe (Non-Volatile Memory Express) Interface, SPI, IC2, etc.

[00327] All of the read ports (e.g., 218 and 222) are configured to be inactive when a write operation is applied to the shared write port 222. The read ports may also be configured to process reads concurrently with each other. The shared write port 222 is configured to write to an address space, where the shared write port 222 is configured to write to the first module 232 via a first portion of the address space and write to the second module 234 via a second portion of the address space. Each module of the plurality of modules 236 includes an independent read port for concurrent reading via a respective independent read port of any of the plurality of modules.

[00328] Each read port for a respective module may include contacts for circuitry found within the second device 226 to interface via metallic contacts. Thus, there may be metallic contacts on the top layer 208 that are configured to interface with metallic contacts on the surface 228 of the chiplet 230 such that the metallic contacts allow for a read space that is coextensive with a read space of a module of the modules 236. The read spaces of the modules group 236 may all be coextensive with each other (as is described with reference to Figs. 3 and 4).

[00329] In one embodiment, the read peripheral for the first module 232 is implemented on a silicon substrate 204 (sometimes referred to as a Front-end-of-the-line). The second layer 206 (sometimes call the Back-end-of-the-line) may be built next in the manufacturing process

on top of the silicon substrate 204 (and any circuitry) and may contain the respective memory bit cells. In an alternative embodiment, the read peripheral for the first module 232 is implemented in the second layer 206 and is disposed between the modules group 236 and the surface 228 of the chiplet 230.

[00330] The modules group 236 may be configured to process write commands only during reset. The write commands may be “slow write” commands. That is, the modules group 236 may have very low write speeds relative to its read speed. The write logic may be frozen (or disabled) when the modules group 236 are used for reading data. In some specific embodiments, the integrated circuit 212 provides functionality to allocate memory blocks to the modules group 236 based on the usage of the modules group 236. In other embodiments, the memory addresses are fixed along with the allocation. The integrated circuit 212 may be implemented as a face-to-face bonded chiplet 230. The face-to face bonding may be bump-less wafer bonding.

[00331] The modules group 236 can have a single write peripheral 202. In other embodiments, each module of the modules group 236 may have a dedicated write peripheral that utilizes a shared clock. In yet other embodiments, the modules group 236 may also be organized into separate partitions each with partition having a dedicated read peripheral, where each dedicated read peripheral has an independent clock. The partitions may be one, two, or more modules of the modules group 236.

[00332] The write peripheral 202 circuitry's overall architecture may include a series of different components, including write driver, address decoders, sense amplifiers, data input latches, data bus, etc. and/or some combination thereof. Write drivers or write buffers, may be tasked with transferring data onto the memory cell. They may enhance the input signal to achieve a level appropriate for the memory cell. Address decoders may be used to interpret the memory address that is fed as an input where the data needs to be written. By activating the specific row and column of the memory array linked to that address, they may be used to select the target memory cell. Sense amplifiers may be used to identify and boost the signal from the memory cells during reading operations, also participate in refreshing the memory cell post data write in write operations. The write operation is instigated by a write enable signal. When a write command is initiated, this signal propels the write drivers and decoders into the writing process. Data input latches may be used as temporary storage units, retaining the data set to be written into the memory until the write operation is implemented. A data bus with a transmission route, can be used to facilitate the movement of data from the data input latches to the memory cells.

[00333] A write operation to the modules group may be performed through a priority arbitration circuit that facilitates the modules to be accessed in a predetermined order, and the shared write port 222 may be configured to write to a virtual address space that is mapped onto a physical memory space. The integrated circuit 212 may include a high voltage write logic used within the write peripheral 202, and the second semiconductor device 226 may comprise a plurality of processing elements, whereby each processing element includes a respective interface to communicate with a respective module of the modules group 236. Furthermore, the chiplet 230 may include an interface to the shared write port 222 on the second side to thereby interface with a complementary interface on the second semiconductor device 226.

[00334] The integrated circuit 212 may also include a power gating circuitry that selectively powers down a module of the modules 236 when not in use. Additionally, the integrated circuit 212 may have a write peripheral 202 of the modules group 236 connected to a dedicated I/O pad to enable data transfer external to the package of the integrated circuit.

[00335] The integrated circuit 212 may utilize multiple modules of the modules group 234 grouped together. These modules may be synchronized with one another in specific embodiments. In some cases, all the modules are synchronized, while in other instances, only specific modules are to be synchronized. For instance, the circuit on a second device 226 may need to synchronize with a specific module when reading data from one of the modules in the module group 236.

[00336] To synchronize the modules, the integrated circuit 212 may use various timing technologies. In some cases, a plurality of clocks may feed each respective module of the modules group 236, thereby allowing each module to have decoupled timing relative to the other modules in the group. This decoupling ensures that any delay in one module will not affect the functioning of other modules. It is worth noting that the clocks used may or may not need to be synchronized. In some cases, a common clock can be used to synchronize the modules. In yet other embodiments, the clock signal or signals may be provided by the second device 226.

[00337] In alternative embodiments, other synchronization techniques can be used, such as phase comparison of the clock signals or a phase-locked loop (PLL) synchronization method. Another embodiment for synchronizing the modules in the IC could use delay-locked loop (DLL) synchronization. In this method, a delay element is added to the clock signal path, and the output is compared to the input clock signal. The feedback loop adjusts the delay element until the output of the DLL matches the input, resulting in synchronization of the clock signals.

[00338] In another embodiment, the integrated circuit 212 could use a combination of different synchronization techniques to achieve synchronization between the modules. For example, some modules may use PLL synchronization while others use clock delay lines or DLL synchronization, depending on their specific requirements. Additionally, the integrated circuit 212 can also use redundant synchronization techniques to ensure reliability and redundancy in case one method fails. For example, the integrated circuit 212 could use both PLL synchronization and DLL synchronization simultaneously, so that if one method fails, the other can still maintain synchronization.

[00339] Fig. 3 shows a block diagram 300 illustrating the memory address space of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure. The memory address space includes a write address space 316 and read data address spaces 310, 312, 314.

[00340] The write address space 316 consists of various units where data, e.g., weights, and/or instructions can be stored. These units are referred to as memory addresses. The module group 302 includes multiple memory modules 304, 306, 308. The write address space 316 may be distributed among the memory modules 304, 306, 308 such that the write address space 316 spans from 0 to $N*M-1$. As shown in Fig. 3, the modules group 302 has N memory modules 304, 306, 308, where N is a positive integer, and each module has a memory size of M . The total number of unique write memory addresses in the write address space will be $N*M$, which can be referenced by an integer from 0 to $N*M-1$.

[00341] Starting at 0, memory addresses of the write address space 316 are ordered sequentially up to $N*M-1$. In other words, the first address is 0 and the final address is $N*M-1$, encompassing a total of $N*M$ addresses. This ordering can be linear (each address increases by one) or some other specified pattern depending.

[00342] The write memory addressing can be implemented in a variety of ways based on the system architecture. One method used in a specific embodiment is to use the base and limit registers. The base register holds the smallest legal physical write memory address, and the limit register specifies the size of the range. Therefore, to generate a logical address, you would add the base to the relative address. In other embodiments, a memory addressing scheme may be used where the base used is set to be 0. Yet additional write addressing techniques will be appreciated by one of ordinary skill in the relevant art.

[00343] For any device that writes to the modules group 302, each memory module can possess a unique set of write memory addresses such all memory addresses within the modules group 302 is unique with respect to writing data. e.g., the first module starting at 0 and the last

one ending at $N*M-1$. This allocation, in some embodiments, may be dependent on the memory management system of the device writing data to the modules 304, 306, 308, which could range from simple fixed partitioning schemes to more complex dynamic partitioning models.

[00344] For instance, in a straightforward linear model where each module (304, 306, or 308) has an equal size of M addresses, the first module 304 would possess write addresses 0 to $M-1$, the second module would have write addresses M to $2M-1$, the third module would have write addresses $2M$ to $3*M-1$, and so forth. The N th module 308, therefore, would possess write addresses from $(N-1)*M$ to $N*M-1$.

[00345] It is contemplated that one of ordinary skill in the relevant art may use other implementations of write memory addresses from 0 to $N*M-1$ that depends on various factors such as the hardware architecture, operating system, memory management schemes, and the nature of the programs being run on the system, etc.

[00346] The modules group 302 has different read data address spaces 310, 312, 314. These read address spaces 310, 312, 314 may have overlapping addresses spaces, may have contiguous address spaces, or may have coextensive address spaces. The read address spaces 310, 312, 314 may be independent relative to each other. The system includes three independent read address spaces, labeled as read address spaces 310, 312, and 314. Each of these read address spaces is distinct from the others, meaning that reads can be performed in each space without affecting the others.

[00347] The read address spaces 310, 312, 314 may be defined as contiguous blocks of memory addresses, each with its own starting address and ending address. In modules group 302, each read address space 310, 312, 314 may have a range of addresses that corresponds to values from 0 to $M-1$, where M is a maximum value determined by the size of the modules 304, 306, 308 being used.

[00348] In one embodiment, allowing one processing unit to interface with each read address space 310, 312, 314, the concurrent reads may be implemented as described herein. The independence of the read address spaces 310, 312, 314 ensures that each processing unit can access its desired data without causing any interference or conflict with other processing units.

[00349] Fig. 4 shows a block diagram illustrating the memory address space with the signal interfaces of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure. The signals used in Fig. 4 may be used with any embodiment described herein. However, one of ordinary skill in the relevant art will appreciate that different signaling schemes may be used.

[00350] The modules group 402 includes modules 404, 406, 408 that share a common write peripheral 411. The write peripheral 411 includes a write address bus that includes the address of the data being written, a write data bus that includes the data, a write clock cause the writes to occur (e.g., either on a leading or trailing edge of the clock signal, etc.). The writes only occur if the write enable signal indicates a write should occur. Any logic may be used, e.g., high voltage may correspond to 1 and a low voltage may correspond to 0, or vice versa. In some embodiments, the write peripheral 411 may be on the chiplet 230 and in other embodiments, the write peripheral 411 is on the second device 226.

[00351] The modules group 402 has modules 404, 406, 408 where each has a respective read peripheral 410, 412, 414. Each of the read peripheral 410, 412, 414 has a read address bus to send an address for reading, a read data bus to receive the data, a read clock which is the clock used to control the timing of the output of the digital data, and an output enable that is a precondition to outputting data. Any logic may be used, e.g., high voltage may correspond to 1 and a low voltage may correspond to 0, or vice versa. In yet additional embodiments, multi-bit or analog data storage may be used. In some embodiments, one or more of the read peripherals 410, 412, 414 may be on the chiplet 230 and in other embodiments, one or more of the read peripherals 410, 412, 414 are on the second device 226.

[00352] Fig. 5 shows an illustration of an integrated circuit 500 that may be part of a semiconductor device such as a chiplet in accordance with an embodiment of the present disclosure. The integrated circuit 500 may be disposed on a semiconductor device, such as a chiplet, that has a silicon substrate 506 and a second layer portion 508. Within the integrated circuit 500, there may be an array section forming the module 502 where a three-dimensional column array of memory bit cells 522 has the necessary components to store memory in non-voltage, semi-volatile memory, or a memory format as described herein.

[00353] The integrated circuit 500 may include a modules group having a plurality of modules including a first module and a second module, etc. even though only a single module 502 is shown. The memory bit cells 522 are written to by the shared write port 512, 516, which includes both a write address bus line 512 and a write data bus 516. These buses run through the second layer 508 and can be connected to a second semiconductor device via an interposer. The second device has electrical contacts that complement those on the surface 518, allowing it to be electrically coupled to the write address and data buses. The memory bit cells 522 can be read from via the read port 524, 526, which includes a read address bus line 524 and a read data bus 526. Both of these buses can also run through the second layer 508 to the

second semiconductor device coupled to the surface 518, which also has complementary electrical contacts to allow it to be electrically coupled to the read address and data buses.

[00354] Various kinds of memory technologies may be used for the memory bit cells 522, such as a vertical connectivity fabric structure formed from non-volatile memory unit cells arranged in a three-dimensional column array 522. The memory bit cells 522 may utilize one or more of a cross-point, 3D NANDs, 3D NORs, 3D ANDs, and/or a stacked planar layer.

[00355] In some embodiments, the integrated circuit 500 is electrically connected to a second semiconductor device (not shown in Fig. 5) comprising another integrated circuit, which may be a system-on-chip or a Field-Programmable-Gate-Array. In some embodiments, the memory bit cells 522 may be formed from various non-volatile memory types, such as FeFET, FeRAM, ReRAM, SOT, or STT. Additionally, alternatively, or optionally, the memory bit cells may be formed from non-volatile memory unit cells having 2-terminal devices, 3-terminal devices, or 4-terminal devices.

[00356] For example, the memory unit bit cells 522 may be formed from ferroelectric materials, such as a ferroelectric tunnel junction, a diode, a capacitor, a single-gate transistor, or a dual-gate transistor. Alternatively, the memory unit bit cells 522 may be formed from memristive materials, such as at least one ReRAM, or magnetic materials, such as at least one spin-orbit-torque device or at least one spin-transfer-torque device. Moreover, the non-volatile memory unit cells 522 may also be formed from phase-change materials or anti-ferroelectric materials.

[00357] In some alternative embodiments, the non-volatile memory unit cells 522 can be formed from other types of materials, such as phase change materials, anti-ferroelectric materials, or multi-bit PCM materials. The non-volatile unit cells can be formed utilizing different structures, such as resistive random-access memory (RRAM) technology, magnetic random-access memory (MRAM) technology, or ferroelectric random-access memory (FRAM) technology.

[00358] Moreover, in some implementations, 3D NAND technology may be utilized to form the memory unit bit cells 522. For example, the memory unit bit cells 522 may be formed from stacked memory layers where each layer includes a plurality of memory cells that can be accessed using shared bit lines. In such a case, the read port 524, 526 may be coupled to the bit lines, and the write port 512, 516 may be coupled to the word lines that control the access to each layer.

[00359] In another embodiment, the 3D connectivity fabric structure can be built with stacked layers of either NAND gates, NOR gates, or AND gates, and in some cases, different

types of logic gates may be combined to optimize the structure's functionality. In addition, the 3D connectivity fabric structure may be formed utilizing through-silicon-via (TSV) technology, which allows the vertical interconnection of the different layers of the structure.

[00360] Additionally, the non-volatile memory unit cells may include 2-terminal devices, such as a capacitive or a memristive device with or without an additional selector device such as a diode in series, 3-terminal devices, such as a floating-gate transistor, a transistor with an access gate, or 4-terminal devices, such as a transistor with two access gates. The type and configuration of the non-volatile memory unit cells 522 may depend on the specific application requirements, including the speed, power consumption, and reliability of the circuit. The memory unit cell may include or be a single ferroelectric transistor or 6T SRAM cell. The memory unit cell may be a combination of many different devices, including, but not limited to, one or more of a transistor, a memristor, a capacitor, etc.

[00361] In some embodiments, a ferroelectric material can be utilized to form the non-volatile memory unit cells 522. The ferroelectric material may be implemented as any kind of device, including, but not limited to, a thin-film device, such as a ferroelectric tunnel junction, a capacitor, a single-gate transistor, or dual-gate transistors, etc.

[00362] In another embodiment, the non-volatile memory unit cells 522 may be formed from a memristive material, such as a Metal Oxide Memristor (MOM), Conductive-Bridging RAM (CBRAM), or valence change memory (VCM), each of which provides different benefits regarding power consumption, speed, endurance, etc.

[00363] Moreover, in some embodiments, the non-volatile memory unit cells 522 may be formed from a magnetic material, such as spin-orbit-torque (SOT) devices, spin-transfer-torque (STT) devices, or perpendicular magnetic tunnel junctions (p-MTJ).

[00364] In one embodiment, the modules group may include many modules where each of which can be accessed through dedicated read ports 524, 526 with a dedicated read peripheral 520 while sharing the same write port 512, 516 and shared write peripheral 510. The shared write port 512, 516 can be configured to selectively write to one or more of the plurality of modules within the modules group including the memory bit cells 522. Each of the modules may have the same or different sizes, and different module sizes may be configured to optimize the utilization of the memory array with different operating scenarios, etc.

[00365] Furthermore, the integrated circuit 500 may be formed utilizing different manufacturing processes and techniques, which include but not limited to, a CMOS or Bipolar-CMOS-DMOS (BCD) process, a silicon-on-insulator (SOI) process, a FinFET process, a silicon germanium (SiGe) process, a gallium arsenide (GaAs) process, etc.

[00366] In some embodiments, the three-dimensional column array of memory bit cells 522 forms is configured as a microvault. Additionally or alternatively, each of the microvaults will have a dedicated read peripheral 520 and a write peripheral 510 that is also a dedicated write peripheral rather than a shared write peripheral. That is, in some embodiments, each microvault includes a dedicated write connection and a dedicated read connection, predetermined number of microvaults (e.g., 2 or 4), may have a dedicated write connection and a dedicated read connection, with or without dedicated respective peripheries, etc.

[00367] Fig. 6 shows a perspective of an assembly 600 having the integrated circuit of Fig. 1 implemented on a semiconductor device, such as the chiplet 230, that is electrically connected to a system-on-a-chip (“SOC”) 610 in accordance with an embodiment of the present disclosure. The semiconductor device, in this embodiment, is the chiplet 230 that is electrically connected to a system-on-a-chip (“SOC”) 610.

[00368] Referring to Fig. 6, the SOC 610 includes a silicon substrate 602 on which a plurality of processing elements is formed, including a processing element 606. The processing elements can communicate with each other through a Network-on-Chip (“NOC”) 604, which is a communication fabric that directs data transfer between the processing elements. The communication fabric can take various forms, including buses, switches, NOCs, etc. The NOC 604 in the SOC 610 directs data traffic between the various nodes (e.g., the processing element 606) and links, which provide the communication paths between the nodes.

[00369] The plurality of processing elements including the processing element 606 processing elements can be any suitable type of processors capable of executing instructions, including microprocessors, graphics processing units (GPUs), digital signal processors (DSPs), or application-specific integrated circuits (ASICs).

[00370] Additionally, the SOC 610 may comprise various modules, such as module 232, which are grouped together to provide memory functionality to the assembly 600 as described here. The modules in modules group 236 can be coupled to a respective processing element provide it readable memory. In some embodiments, the coupling between the module (e.g., module 232) and the processing element (e.g., 606) can be achieved through interconnects on the silicon substrate 602.

[00371] After the circuitry is formed on the silicon substrate 602, a second layer 608 can be disposed on top of the substrate. The second layer 608 can be any suitable material, such as an insulating material, a metal, a dielectric, or interconnect layer, and it may be bonded to the chiplet 230. The bonding can be done using any suitable technique, including but not limited to, adhesives, soldering, or welding, etc.

[00372] In general, the assembly 600 provides a means of integrating the chiplet 230, which can include the integrated circuit of Fig. 1, with the SOC 610. Integrating the chiplet 230 provides various advantages, such as enhanced functionality, higher performance, and lower power consumption. Moreover, the integration of the chiplet 230 with the SOC 610 can be accomplished in various ways, depending on the particular application and design objectives of the system.

[00373] The assembly 600 can incorporate various variations and modifications, depending on the specific requirements of the system. For example, the processing elements formed on the silicon substrate 602 can vary in their number, type, and arrangement. Similarly, the modules in modules group 236 can vary in their number, type, and function.

[00374] Furthermore, the second layer 608 can be modified to include additional functionality. For instance, the second layer 608 can include passive components, such as resistors, capacitors, and inductors, or active components, such as transistors or diodes. Incorporating these components in the second layer 608 can further enhance the functionality and performance of the system.

[00375] In another variation, the assembly 600 can incorporate a heterogeneous integration approach, where the chiplet 230 is fabricated using a different technology than that used for the SOC 610. This approach allows for the optimal use of different fabrication technologies for different parts of the system, resulting in improved performance and reduced power consumption.

[00376] Fig. 7 shows a perspective view of an assembly 700 having a semiconductor device 707 with an array of processing elements 706 (on a grid of processing element 706a,a to 706n,n, where the first subscript is the columns and the second subscript is the row), and a second semiconductor device 709 having an array of microvaults 708. The array of microvaults 708 are on a grid of microvaults 708a,a to 708n,n, where the first subscript is the columns and the second subscript is the row). These subscripts may line up such that a respective subscript of a processing element 706 corresponds to a respective subscript of a microvault 708. The microvaults 708 are a type of module described herein where it is positioned in a vertical direction, e.g., above a respective processing element 706. The semiconductor device 707 may be a chiplet. Also, the semiconductor device 709 may also be a chiplet. The chiplets 707,709 may be bonded together. The different layers 710 (e.g., 710a through 710d can correspond) may be allocated for separate AI models (e.g., parameters in a neural network, such as a CNN or transformer model).

[00377] The assembly 700 is the overarching structure that houses the various components shown in Fig. 7. It provides mechanical support and integration for the other elements, allowing them to function as a unified system.

[00378] The assembly 700 includes two semiconductor devices - the semiconductor device 707 and the semiconductor device 709. The semiconductor device 707 contains an array of processing elements labeled 706a,a to 706n,n. Similarly, the semiconductor device 709 contains an array of microvaults labeled 708a,a to 708n,n.

[00379] The subscripts a,a to n,n indicate that the processing elements 706 and microvaults 708 are arranged in a grid pattern, with the first subscript referring to the column and the second subscript referring to the row. This grid arrangement allows each processing element 706 to have a corresponding microvault 708 positioned vertically above it. For example, processing element 706a,a has microvault 708a,a above it, processing element 706b,b has microvault 708b,b above it, and so on. The alignment of the grid allows tight integration between the processing and storage components.

[00380] In some embodiments, the semiconductor devices 707 and 709 are potentially separate chiplets that are integrated using packaging techniques into the unified assembly 700. The chiplet form factor allows greater flexibility and customization in assembling the system. This arrangement is such that each processing element 706 can access its respective microvault 708 located above it to retrieve relevant data, such as weights for neural networks or AI models. This may provide high bandwidth and low latency access to the data needed for efficient processing.

[00381] Input data enters the system via the input DRAM memories 702. This data flows into the processing elements 706, where it is operated on locally using weights or parameters from the vertically integrated microvaults 708. The processing results output via the output DRAM memories 704. The input DRAM memories 702 consist of multiple individual DRAM modules labeled 702a, 702b, and 702c. The DRAM memories 702 can be any type of dynamic random access memory, including but not limited to DDR SDRAM, LPDDR SDRAM, GDDR SDRAM, and HBM. The DRAM memories provide high-bandwidth data input capabilities to feed data, such as inference inputs or training data, into the processing pipeline.

[00382] In some embodiments, each individual DRAM module 702a, 702b, and 702c has a dedicated interface and data path to each processing element 706. For example, DRAM module 702a may feed data only to processing element 706a,a, while DRAM module 702b feeds data only to processing element 706b,b. This provides modular scalability, as additional DRAM modules can be added to feed more processing elements.

[00383] The number of input DRAM memories 702 and individual modules 702a-702c may vary depending on the application requirements. For instance, there could be 4, 8, 16, or more input DRAM modules. The capacity of each module can range from gigabytes to terabytes depending on factors such as access speed, power, and cost budget.

[00384] High-speed interfaces like DDR5, GDDR6, or HBM3 may be used to maximize data transfer bandwidth between the input DRAM memories 702 and the processing elements 706 across the semiconductor device 707. Shared data buses, crossbar switches, or on-chip networks may interconnect groups of DRAM modules 702 and processing elements 706.

[00385] In some implementations, the input DRAM modules 702 may be stacked or arranged in a multi-dimensional configuration to increase overall memory capacity and bandwidth while reducing latency and power consumption. Specialized memory controllers and schedulers may manage parallel data access across multiple input DRAM modules 702.

[00386] The input DRAM memories 702 supply the high-bandwidth data needs of the parallel processing elements 706, enabling fast and efficient data-intensive computations such as neural network inferencing. Each processing element 706 can directly access the required input data from its dedicated DRAM module 702 without contending with other processors for data access.

[00387] In alternative embodiments, instead of, or in addition to, the DRAM memories 702, 706, adjacent accelerator chiplets may be in communication with the semiconductor device 707. That is, there may be a grid-like arrangement of assemblies 700 in communication with each other to perform AI inference and/or AI training (e.g., transformer inference, CNN inference, ANN inference, etc.). In some embodiments, there may be clusters of semiconductor devices 707 that share a bank or portion of DRAM memories 702 and/or 706. In some embodiments, the input DRAM memories 702 and the output DRAM memories 704 may be combined into the same DRAM memory.

[00388] The assembly 700 includes a semiconductor device 707 that comprises an array of processing elements labeled from 706a,a to 706n,n. Each processing element in the array may be configured to execute specialized computations and data processing operations. For instance, in some embodiments, the processing elements could be optimized for artificial intelligence workloads like neural network inference. In other cases, the processing elements may focus more on general-purpose capabilities. Ultimately, the capabilities of each processing element depend on its specific microarchitecture which can be tailored for certain applications if desired.

[00389] The processing elements 706 can access nearby memory storage to retrieve data that feeds into their computations. This memory may be physically separate from the processing element arrays 706 as is the case with the microvaults 708 shown in Figure 7. The processing elements 706 and microvaults 708 are aligned so that each microvault is positioned directly above its corresponding processing element in a vertical configuration. This tight coupling provides fast data transfer speeds between each vault-element pair.

[00390] In terms of physical implementation, the array of processing elements 706 resides within the semiconductor device 707. The semiconductor device 707 could potentially be manufactured as a standalone chiplet using advanced packaging techniques. This modular chiplet can then be integrated with other components like the microvault chiplet 709 through high-density interconnections. Some options include bumpless hybrid bonding, interposers, or even monolithic 3D integration. Ultimately, combining chiplets allows creating powerful heterogenous systems with optimized dies.

[00391] The specific number, design, and interconnect scheme of processing elements 706 present can vary between implementations of assembly 700. For instance, simpler systems may need only a 2x2 grid of elements whereas a sophisticated AI accelerator could feature a 32x32 array. The processing elements 706 themselves can also have different memory access routes across the assemblies. Point-to-point links, crossbar switches, or shared buses are possible connection structures. Such architectural decisions depend on the performance and area constraints trying to be met.

[00392] The second semiconductor device 709 is a separate device from the first semiconductor device 707. Like the first semiconductor device 707, the second semiconductor device 709 may also be implemented as a chiplet. The second semiconductor device 709 includes an array of microvaults 708, arranged on a grid spanning from microvault 708a,a to 708n,n.

[00393] As mentioned, the microvaults 708 on the second semiconductor device 709 are positioned vertically above the processing elements 706 on the first semiconductor device 707. Each microvault 708 lines up with and corresponds to the processing element 706 underneath it, based on the subscripts identifying their position in the grid. For example, microvault 708a,a is vertically aligned with and corresponds to processing element 706a,a. This allows each processing element 706 to access the microvault 708 above it.

[00394] The microvaults 708 act as a memory structure, storing things like AI model weights that can be accessed by the processing elements 706 underneath during operations like neural network inference. The microvaults 708 may be optimized for very fast read times but

slower write times. This allows the processing elements 706 to rapidly access the weights and data needed for their computations, while less frequently updated data can still be written at a slower pace.

[00395] In some embodiments, the second semiconductor device 709 containing the array of microvaults 708 is directly bonded to the first semiconductor device 707 with the processing elements 706. This bonding aligns each microvault 708 with its corresponding processing element 706 underneath. Electrically conductive interconnects between the devices allow each processing element 706 to communicate directly upwards with its respective overlying microvault 708. This provides a compact, modular, and efficient system architecture.

[00396] The microvaults 708 may contain multiple memory layers, labeled 710a to 710d, each storing weights or data for a different AI model. For example, layer 710a contains the weights for model A, layer 710b contains the weights for model B, and so on. Stacking these layers vertically contributes to the high density and fast access times of the microvault design.

[00397] The microvaults 708 can be implemented using various memory technologies, including but not limited to SRAM, FeFET, ReRAM, SOT, and STT, optimized for fast readout times to supply data to the processing elements 706 with minimal latency. Specific embodiments may configure the microvaults 708 to have much faster read speeds compared to their write speeds. The microvaults 708 may be implemented using any FeFET or memory structure described herein.

[00398] In some embodiments, each microvault 708 may have a capacity between 4 kilobytes to 128 kilobytes for storing parameters for machine learning models or other data. The bit density per layer may exceed 0.4 gigabits per square millimeter. The microvaults' 708 compact size, between less than 100 micrometers on each side in one embodiment or 12 micrometers by 12 micrometers in another, allows high-density integration of the memory modules.

[00399] The array-based arrangement of the microvaults 708 may enable concurrent parallel data access by the processing elements 706, supporting high-throughput data processing by the assembly 700. The one-to-one alignment of the microvaults 708 and processing elements 706 also ensures that each processing element 706 has dedicated access to its required data without contention.

[00400] The microvaults 708 share the semiconductor device interface provided by the second semiconductor device 709, which facilitates writing data to the microvaults 708 from the input DRAM memories 702. Reading data from the microvaults 708 to the processing

elements 706 and output DRAM memories 704 is handled through dedicated pathways between each vertically aligned microvault 708 and processing element pair.

[00401] The microvault memory layers 710 refer to multiple layers of microvault memories stacked vertically within the second semiconductor device 709. As illustrated in Fig. 7, there are four separate microvault memory layers labeled as 710a, 710b, 710c, and 710d. Each layer contains an array of microvaults, such as the array of microvaults 708 shown in the diagram.

[00402] In one embodiment, the microvaults 708 may utilize a stacked 3D NAND architecture built from multiple layers of NAND memory arrays using charge trap flash technology. Each microvault 708 may contain a dedicated set of wordline drivers on the bottom layer to facilitate access to the 3D NAND cell arrays above, spaced by alternating dielectric layers. The 3D NAND implementation may be used to maximize density and throughput by leveraging vertical scaling.

[00403] In an alternative embodiment, the microvaults 708 employ a 3D NOR architecture constructed from multiple tiers of NOR flash memory arrays. Each plane features NOR strings with a source line and bit line architecture, stacked on top of each other using vias. The 3D NOR arrangement optimizes random read access times to stored data.

[00404] The microvaults 708 may also adopt a hybrid configuration with different types of volatile and/or non-volatile memory, such as combining FeRAM and ReRAM cells, organized into vertical sub-arrays. This heterogeneous 3D integration allows optimizing for speed, endurance, and retention within the same vault structure.

[00405] In certain embodiments, the microvaults 708 integrate processing logic like analog computing directly into the memory array stack itself. This processing-in-memory approach places basic computational operators within the memory peripheral or bit cells, enabling highly parallel and efficient in-situ data processing.

[00406] Some implementations may utilize 2.5D or 3D stacking to integrate the microvaults 708 with other components like logic, CPUs, GPUs or application-specific accelerators. This tight packaging integration via techniques like high-bandwidth memory cube architectures reduces data transfer latency and power consumption.

[00407] The microvaults 708 may also employ a virtualized architecture, with an external memory controller handling translation between the physical array organization and dynamically allocated virtual memory domains. These virtual domains mapped onto the physical array effectively creates separate virtual vaults with flexible capacities tailored to application needs.

[00408] In certain embodiments, the microvaults 708 are designed as Computational RAM (CRAM) with integrated processing capabilities within the bit cell peripheral to enable highly parallel in-memory computing architectures. Gateless transistor structures integrated into the CRAM arrays facilitate efficient execution of bulk bitwise operations.

[00409] Some implementations arrange the microvaults 708 into modular Memory Processing Unit (MPU) structures containing dedicated processing logic tailored for workloads like AI inferencing. The MPU architecture couples vault arrays to vector processors via high-speed interfaces like HBM2 enabling low-latency data transfers.

[00410] The microvaults 708 may also implement content-addressable capabilities by integrating comparison logic into the memory peripheral. This facilitates searching or accessing data based on content rather than explicit addresses, enabling powerful pattern matching capabilities.

[00411] Certain embodiments may stack multiple microvault dies on top of base logic dies featuring things like GPUs or AI accelerators. This creates dense, high-bandwidth heterogeneous systems optimized for data-centric workloads while minimizing data movement.

[00412] The microvault memory layers 710 may be fabricated utilizing three-dimensional integrated circuit manufacturing processes to stack multiple dies or wafers containing microvault 708 arrays on top of each other. Through-silicon vias (TSVs) or other vertical interconnect technologies can be employed to enable communication between the layers.

[00413] In some embodiments, each microvault memory layer 710 corresponds to a different artificial intelligence (AI) model or application. For example, layer 710a could store the weights and parameters for AI model A, layer 710b could store the weights and parameters for AI model B, and so on. This allows multiple AI models to be stored efficiently within the same microvault memory 708 structure.

[00414] The microvaults 708 may possess capacities ranging from 4 kilobytes to 128 kilobytes in some embodiments. In other cases, the capacity could be between 4 kilobytes to 16 kilobytes. Each microvault could have lateral dimensions less than 100 micrometers by less than 100 micrometers, while extending vertically to incorporate potentially over 200 memory cell layers in some implementations.

[00415] In some embodiments, the bit density of per square millimeter per layer within the microvault memory layers 710 may facilitate high-capacity storage with a small footprint.

The layers may utilize non-volatile memory technologies, such as FeFET, STT-MRAM, or ReRAM, to retain data when power is removed.

[00416] In operation, the processing elements 706 may access weights or parameters from the microvault memory layers 710 to perform neural network inferencing or other machine learning computations.

[00417] The inference results of the various AIs may be sent to the output DRAM memories 704, which comprise individual DRAM memory modules labeled 704a, 704b, and 704c. The output DRAM memories 704 are positioned adjacent to the array of microvaults 708 and the second semiconductor device 709. The output DRAM memories 704 may serve as temporary data storage that can buffer output data retrieved from the microvaults 708 before it is transmitted externally.

[00418] Each DRAM memory module 704a, 704b, and 704c may have similar or different storage capacities, depending on the design requirements. For example, in one embodiment, each module contains 16 megabits of storage. The DRAM storage cells utilize a capacitor to retain data bits in the form of electrical charges. Due to charge leakage, the DRAM memories require periodic refresh cycles to maintain the stored data integrity. To enable concurrent reads and writes across multiple modules, each DRAM module 704a, 704b, and 704c can have dedicated internal control circuitry and I/O ports.

[00419] The data outputs from the individual microvaults 708 may get aggregated and buffered in the output DRAM memories 704 before being transmitted to external components via peripheral circuitry. Buffering the data allows the transmission rate to be regulated to match the requirements of the external interfaces. It also enables data processing operations like formatting, encoding, or encryption to be performed by the second semiconductor device 709 prior to output.

[00420] In some embodiments, the output DRAM modules 704a, 704b, and 704c are designed to provide high-density, low-cost temporary data storage to support the high-bandwidth parallel reads from the array of microvaults 708. Optimizing these performance parameters allows efficient extraction of data from the microvaults to feed the computational workflows hosted on external chips or devices. Specific implementations may utilize various types of DRAM, including asynchronous DRAM, synchronous DRAM, graphics DRAM, and low-power DRAM tailored to the application. Overall, the output DRAM memories 704 facilitate seamless data movement from the integrated microvaults to external execution pipelines.

[00421] Fig. 8 shows an assembly 800 of a semiconductor devices 802, 804, 806, 808, 810, 812, 814 including several memory types in accordance with an embodiment of the

present disclosure. Specifically, Fig. 8 shows an exemplary assembly 800 of semiconductor devices 802, 804, 806, 808, 810, 812, 814 configured to provide a hierarchical memory structure. The assembly 800 is modular and scalable, allowing for various combinations and numbers of semiconductor devices, which may be implemented as chiplets in certain embodiments, to be stacked to meet specific performance and density requirements.

[00422] The assembly 800 includes an application semiconductor 802, that may be a plurality of processing elements as described herein. On top of the semiconductor device 802 is semiconductor device 814 that includes an array of microvaults. One top of the semiconductor device 814 is semiconductor device 812, which may also include an array of microvaults. On top of the semiconductor device 812, are semiconductor devices 810, 808, which may be SRAM vaulted dies. One top of the semiconductor device 808, is semiconductor devices 806, 804 may be DRAM vaulted dies. These vaults 816 may be arranged in a grid-like fashion such that 816a,a to 816n,n subscripts the vaults. Each of these vaults may include a respective microvault from semiconductor devices 804, 812, respective SRAM vaults from semiconductor devices 810, 808, and respective DRAM vaults from semiconductor devices 806, 804.

[00423] At the base of assembly 800 lies the semiconductor device 802, which comprises a plurality of processing elements. These processing elements execute computational tasks and facilitating data flow within the system.

[00424] Directly above semiconductor device 802 is semiconductor device 814, which includes an array of microvaults. These microvaults utilize Field-Effect Transistors (FeFETs) known for their non-volatile characteristics and suitability for high-density memory applications. The FeFET-based microvaults may be designed to enable high-speed read operations essential for rapid data retrieval during processing tasks, such as AI inferencing, while supporting slower write operations that are more tolerant to latency. Stacked on top of semiconductor device 814 is semiconductor device 812, which similarly includes an array of microvaults. The presence of multiple layers of microvaults in semiconductor devices 814 and 812 exemplifies the scalable nature of the assembly, where additional memory capacities and functionalities can be integrated through additional layers.

[00425] Further contributing to the memory hierarchy, semiconductor devices 810 and 808, positioned above semiconductor device 812, are depicted as SRAM vaulted dies. SRAM provides fast access memory that can serve as a cache or buffer to the slower, but denser, FeFET microvault memory layers beneath.

[00426] At the top of the assembly 800 and hence the memory structure are semiconductor devices 806 and 804, illustrated as DRAM vaulted dies. DRAM is typically used for main memory due to its relatively high speed and low cost per bit compared to SRAM, offering a balance between performance and economy.

[00427] The arrangement of vaults 816 in a grid-like fashion, subscripted from 816a,a to 816n,n, indicates that each processing element at a given location (a,b) in semiconductor device 802 has dedicated access to the corresponding vertically aligned vaults of microvaults and memory cells in the layers above. This vertical stacking and alignment ensure that data and control signals can be directly routed between processing elements and their respective memory stacks, facilitated by interconnect technologies such as through-silicon vias (TSVs) and micro-bumps, which are used in the assembly's 800 3D integrated circuit architecture.

[00428] The modular and scalable design of assembly 800 allows for various combinations of semiconductor devices or chiplets to be integrated into more extensive systems. The flexibility in the number and combination of stacks provides the adaptability to tailor the assembly to the requirements of different applications and performance demands. Each vault within the vaults 816 within the assembly 800 presents a multi-die structure that contributes to the overall capacity and performance of the system.

[00429] Fig. 9 shows an assembly of semiconductor devices including a semiconductor device with a system-on-chip 914 and another semiconductor 906 with microvaults disposed on top in accordance with an embodiment of the present disclosure. The assembly 900 integrates a semiconductor device 906 and a semiconductor device 914, which may be implemented as separate chiplets bonded together. The semiconductor device 914 includes various components to facilitate reading data from the microvaults on the semiconductor device 906, such as a read address register input interconnect 924, read data register 922, and read data register output interconnect 950. These components pass the read address to the microvaults on semiconductor device 906 and return the read data back to the semiconductor device 914.

[00430] Specifically, the read address enters via interconnect 924 into the read address register 926. The output of this register 926 connects through interconnects and bumpless bonds to another read address register 938 on the semiconductor device 906, which then addresses the target microvault 936. The microvault 936 outputs read data via interconnect 940 to a read data register 942, which passes the data back through bumpless bonds 910, 918 to read data register 922 on semiconductor device 914. This data can then be accessed externally via the read data register output interconnect 950. Additionally, the semiconductor device 914

and 906 have interconnected Through-Silicon Vias 916 and 944 to allow communication with devices potentially stacked above semiconductor device 906.

[00431] The semiconductor device 906 features various memory structures to provide data storage capabilities. This includes a microvault 936, which offers high-density, low-latency data storage, along with other peripheral memory components like read data register 942 and read address register 938 to facilitate data reads. The microvault 936 resides on the BEOL portion of the chiplet, allowing dense 3D integration of memory layers. In some implementations, the microvault utilizes non-volatile memory technologies like FeFET or STT-MRAM for data retention without power.

[00432] The semiconductor device 914 comprises processing elements and data routing circuitry to retrieve and manipulate data stored in semiconductor device 906. Components like read address register 926 and read data register 922 handle sending read addresses and receiving data from the microvault 936 respectively. The device 914 also includes interconnects 924, 950 and Through-Silicon Via 916 to communicate externally.

[00433] The two devices 906 and 914 integrate via fine-pitch interconnects like bumpless hybrid bonds 908, 910, 918, 920, 930 and 932. This allows direct data transfer pathways between processing components in device 914 and memory structures in device 906. Alignment during bonding ensures dedicated access - for instance, read data register output interconnect 950 on 914 links directly to read data register 922 to receive requested data.

[00434] The pathways facilitating data flow during reads can be summarized as follows: A read address enters through interconnect 924 into read address register 926 on device 914. This gets communicated via interconnects and bumpless bonds to read address register 938 on device 906, which then addresses microvault 936. Requested data gets passed via interconnect 940 to read data register 942, then transfers through bonds back to read data register 922 on 914, where it becomes available externally via interconnect 950.

[00435] The assembly 900 exemplifies a modular, high-density architecture optimized for data-centric applications like AI inferencing. Tight integration of processing and storage dies via advanced packaging techniques allows localized data access with minimal latency and power. Scalability is also enabled by incorporating multiple chiplets, in this case devices 906 and 914. The assembly 900 illustrates a potential configuration suited for space-constrained, high-performance computing systems.

[00436] The Through-Silicon Via (TSV) 916 is an electrical connection that passes vertically through the semiconductor device 914. Its purpose is to provide a pathway for signals to travel between the top and to a processing element within the semiconductor device 914.

This allows the device to be stacked and interconnected with other components in a vertical configuration. The TSV 916, along with other TSVs on the device, facilitates high-density 3D integration and heterogeneous stacking of multiple devices like chiplets.

[00437] The TSV 916 interacts with several other components within the system. On the top side of semiconductor device 914, it connects to interconnect 912, which couples it to bumpless bonds 918. These bonds interface with complementary bumpless bonds 910 on the bottom side of semiconductor device 906 when the two devices are stacked. This allows signals to travel from device 914 to device 906 through the TSV 916. The route continues as signals go through interconnect 902 to TSV 944 on device 906. TSV 944 provides a vertical signal pathway to the top surface of device 906 where additional devices could be stacked. In the reverse direction, signals can travel from TSV 944 down through device 906, back up TSV 916, and down into device 914. So the TSV 916 provides bidirectional vertical communication across device boundaries.

[00438] There are a few possible variations for the TSV 916 implementation. First, multiple TSVs arranged in an array could be used instead of a single via to increase throughput and redundancy. Second, the dimensions and materials of the TSV could be optimized- for example, smaller TSV diameters using denser materials like tungsten could be advantageous. Additionally, the interface circuitry driving signals into the TSV, like interconnects 912 and 902, could employ variable line drivers to support different voltage levels or signal integrity enhancements. Further embodiments may include integrated monitoring circuitry within TSV 916 to track metrics like temperature and link utilization. And alternative signaling schemes besides electrical signals could be employed in future cases. For instance, integrated silicon photonics utilizing modulated light to convey data through the TSVs could enable very high bandwidth and low latency connectivity. There are multiple avenues to further develop the capabilities of TSV-based vertical links like TSV 916 within these complex 3D integrated architectures.

[00439] There are several variations and alternatives for the interconnect 912 implementation. For example, different conductive materials such as copper or aluminum may be utilized to fabricate the pathways forming interconnect 912 and optimize for conductivity or thermal dissipation. Additionally, interconnect 912 may feature redundant signal paths or self-repair capabilities using spare interconnect lines to improve reliability and resilience. The bumpless bonds 918 and 910 connecting devices 906 and 914 could also be replaced with other high-density bonding approaches like hybrid bonding or Through-Silicon Vias. Furthermore, alternate signaling schemes besides simple digital logic could be employed on interconnect

912, such as analog signaling or multi-level digital waveforms to enhance data transmission capabilities. The routing and dimensions of interconnect 912 can also be adapted according to bandwidth requirements or circuit layout considerations. Overall, many structural and functional alternatives exist for crafting interconnect 912 to meet application needs.

[00440] The bumpless bonds 918 are electrical connections located on the semiconductor device 914 between an interconnect 912 and bumpless bonds 910 of the semiconductor device 906. The bumpless bonds 918 provide an electrical pathway for signals to travel between the semiconductor device 914 and any additional semiconductor devices, such as the semiconductor device 906, stacked on top of the assembly 900. The signals communicated over the bumpless bonds 918 can include data signals, control signals, address signals, or any other signals needed to coordinate operations between the multiple semiconductor devices.

[00441] There are several possible variations for the bumpless bonds 918. The number of individual bond sites can range from just a few to hundreds, depending on signal bandwidth requirements. The bonding method can utilize techniques like direct bonding, plasma-activated bonding, adhesive bonding, or compression bonding. Hybrid bonding approaches are also possible, combining direct wafer bonds with intermediate metal bonds. The size and pitch of each bond site can vary and may use pitches under 10 micrometers to enable high-density connections. Redundant bonds can provide backup pathways. Shielding structures may surround bonds for noise immunity. Overall, many embodiments of bumpless bonds 918 are possible to meet cost, reliability, and performance needs.

[00442] The bumpless bonds 910 provide an interface for communicating signals between the semiconductor device 906 and semiconductor device 914. Specifically, the bumpless bonds 910 of the semiconductor device 906 are electrically coupled to the complementary bumpless bonds 918 of the semiconductor device 914. This allows signals like read/write data and addresses to be transmitted between the two devices. The bumpless nature of the bonds allows for a low-profile, high-density interconnection.

[00443] The bumpless bonds 910 interact with other components in the system to facilitate data transfer operations. For writes, data enters the semiconductor device 914 via the Through-Silicon Via 916, passes through interconnect 912 and bumpless bonds 918 before reaching bumpless bonds 910 of device 906. For reads, addresses flow from the read address register 926 of device 914 through interconnects 928, 930 and bumpless bonds 932 into the read address register 938 on device 906. Read data then returns through bumpless bonds 908

and 920 back to device 914. So the bumpless bonds 910 provide key data and address routing between the devices.

[00444] Possible variations of the bumpless bonds 910 include using different bond densities, materials, or electrical contact configurations to optimize performance. The bonds can use alloying or doping techniques to improve conductivity. Additionally, the routing of signals can be changed, for example by using separate ports for input and output instead of shared ports. More bumpless bonds can be added to increase bandwidth between devices. Shielding may be added around the bonds to reduce interference. Overall, many modifications to the bumpless bonds 910 are possible within the scope of electrically interconnecting multiple devices.

[00445] The Through-Silicon Via (TSV) 944 is an electrical connection that passes vertically through the semiconductor device 906 from the top surface to the bottom surface. Its purpose is to facilitate communication of signals and data between the semiconductor device 906 and any additional semiconductor devices potentially stacked on top of it in a 3D integrated circuit configuration. The TSV 944 enables high-density interconnections between multiple stacked semiconductor layers, providing an efficient means for data routing and signaling.

[00446] The TSV 944 interfaces with surrounding circuitry within the semiconductor device 906, allowing signals to be transmitted upwards or downwards depending on the system configuration. On one end, the TSV 944 couples to the read data register 942 via interconnect 946. The read data register 942 can use the TSV 944 path to transfer read data from the microvault 936 to external semiconductor devices. This enables efficient data offloading from the on-chip memory. On the other end, the TSV 944 continues through to the top surface of semiconductor device 906, where it may interface with complementary contacts or interconnects on the bonded semiconductor above it. This facilitates the vertical transfer of signals and data along the assembly 900.

[00447] There can be many variations in the specific implementation of the TSV 944. Its dimensions can range from a few microns to tens of microns to match pitch requirements. The TSV 944 can be tapered, straight, or have non-uniform cross-sections. It may utilize different conductive materials as liners and fills, including metals like copper, tungsten or alloys. Insulating liners made of materials like silicon dioxide can separate the conductive fill from the substrate. The contacts and interconnects coupling into the TSV 944 can also have diverse layouts. Multiple TSVs can be placed adjacent to each other in a high-density array configuration if desired. Overall, many architectural optimizations in the design and fabrication process of the TSV 944 are possible within the scope of the present disclosure.

[00448] Fig. 10 shows a semiconductor assembly 1000 incorporating a daisy-chained configuration of microvaults 1036, 1058, operatively connected to a multiplexer 1060 and managed by a counter 1062 for coordinated data selection and retrieval, in accordance with an embodiment of the present disclosure. This assembly 1000 is designed to carry out data processing tasks, potentially for applications such as artificial intelligence (AI) and machine learning, where high-speed data access and processing are utilized.

[00449] The assembly 1000 comprises two primary semiconductor devices: semiconductor device 1006 and semiconductor device 1014. Semiconductor device 1014 is depicted as containing several interfaces and registers for data communication, including a read address register input interconnect 1024. This interconnect 1024 facilitates the delivery of read addresses to a read address register 1026, which temporarily holds these addresses before they are transmitted to corresponding microvaults 1036, 1058 in semiconductor device 1006 for data retrieval operations.

[00450] In semiconductor device 1014, interconnect 1028 serves as a pathway for read addresses from the read address register 1026 to transition to bumpless bonds 1030. Bumpless bonds 1030 and 1032 represent high-density, low-profile electrical connections between semiconductor device 1014 and semiconductor device 1006, ensuring the transmission of read addresses with minimal signal loss and physical space requirements.

[00451] Through interconnect 1034, the received addresses reach the read address register 1038 in semiconductor device 1006, which then directs the microvault 1036 to output the requested read data. Microvault 1036, a memory storage unit, may encompass a variety of memory technologies, such as FeFETs and/or 3D-NAND structures as described herein, to facilitate the storage and rapid retrieval of data.

[00452] The multiplexer 1060 selects the appropriate data stream from multiple microvault 1036, 1058 outputs. Controlled by a counter 1062, which may operate according to a predefined sequence or be driven by external control signals, the multiplexer 1060 arbitrates between the outputs of microvault 1036 and another microvault, denoted as microvault 1058. Microvault 1058, similar in function and potential memory technology to microvault 1036, provides an additional source of data for the multiplexer 1060 to select from.

[00453] Once the desired data is selected by the multiplexer 1060, it is temporarily stored in a read data register 1042, also located within semiconductor device 1006. This register 1042 acts as a buffer, holding the data for subsequent processing or transmission. The read data is then routed via interconnect 1004 to bumpless bonds 1008, which facilitate the transfer of data to the semiconductor device 1014.

[00454] Bumpless bonds 1010, 1018 facilitate the continued data's journey through the assembly 1000, ensuring data transfer from semiconductor device 1006 to semiconductor device 1014. Once the read data arrives at semiconductor device 1014, it is channeled via interconnect 1048 to a read data register, specifically read data register 1022, where it can be accessed by external systems, such as an application-specific integrated circuit (ASIC) or a system-on-chip (SoC), via the read data register output interconnect 1050.

[00455] Additionally, the assembly 1000 encompasses Through-Silicon Vias (TSVs) 1016 and 1044, providing vertical electrical connections through the semiconductor devices 1014 and 1006, respectively. These TSVs enable the stacking of additional semiconductor devices or chipllets atop the assembly 1000, thus allowing for vertical expansion of the system's capabilities. Interconnects 1012 and 1046 serve as horizontal pathways for signals to travel to and from the TSVs 1016 and 1044, respectively.

[00456] Although the description presents a specific configuration, the assembly 1000 may be subject to various modifications and alternative embodiments. For example, the number and arrangement of microvaults, the specific types of memory technologies employed within the microvaults, and the configuration of interconnects and bonding areas may be tailored to meet the requirements of different applications.

[00457] In some embodiments, the semiconductor devices 1006 and 1014 may be designed to accommodate additional functionality, such as thermal management layers for heat dissipation, hardware-based encryption modules for data security, or power management circuits to optimize energy consumption. The detailed structure of Fig. 10, therefore, serves as a foundation upon which a variety of sophisticated semiconductor systems can be constructed, each tailored to the specific needs of its intended application.

[00458] In the configuration of assembly 1000 as depicted in Fig. 10, the microvaults, exemplified by microvaults 1036 and 1058, present a daisy-chaining configuration that allows for an expandable and flexible memory architecture within the semiconductor device 1006. This daisy-chaining is facilitated through a series of interconnected pathways and controlled by the multiplexer 1060 in coordination with the counter 1062.

[00459] Each microvault, such as 1036 and 1058, is designed to hold and provide rapid access to data, which may be in the form of stored charge, magnetic states, ferroelectric material states, or other physical embodiments of binary information. The microvaults are interconnected such that the output of one microvault can be routed to the input of another, creating a chain of memory elements. This is achieved through a series of interconnects, such

as interconnect 1034 for microvault 1036 and interconnect 1056 for microvault 1058, which serve as conduits for the read data signals emanating from the microvaults.

[00460] The multiplexer 1060 manages the flow of data from this daisy chain of microvaults. It is designed with multiple inputs, each connected to the output of a microvault via respective interconnects. In the example provided, interconnect 1040 carries the read data from microvault 1036, and interconnect 1056 carries the read data from microvault 1058 to the multiplexer 1060. The multiplexer 1060 is capable of selecting which input to connect to its output at any given time, thus controlling which microvault's data is forwarded to the read data register 1042.

[00461] The counter 1062 orchestrates the operation of the multiplexer 1060. It may be a binary counter or any form of sequential logic circuit that produces a series of output states in response to a clock signal. The counter 1062 progresses through its states with each tick of the clock, which may be provided by an external clock source or generated internally within the semiconductor device 1006. As the counter 1062 advances, it outputs a control signal that instructs the multiplexer 1060 on which input to select.

[00462] For instance, at the first clock pulse, the counter 1062 may instruct the multiplexer 1060 to connect the output from microvault 1036 to the read data register 1042. At the next clock pulse, the counter may switch the connection to microvault 1058's output, and so on, cycling through the available microvaults in a predefined order. The counter's sequence and timing can be configured based on the desired data access patterns and the specific requirements of the processing tasks at hand.

[00463] This clock-driven coordination allows for an efficient and organized retrieval of data from a potentially large array of microvaults. It ensures that each microvault has an equal opportunity to present its data for processing, and it simplifies the control scheme by reducing it to a predictable, rhythmic progression of states. This is particularly advantageous in systems where a large volume of data must be processed in parallel, as it provides a systematic method for accessing and utilizing the stored information.

[00464] It should be noted that while Fig. 10 illustrates only two microvaults, the described daisy-chaining mechanism can be extended to accommodate any arbitrary number of microvaults. Additional microvaults can be added to the chain, with each new microvault connected to the multiplexer via an additional input line. The multiplexer 1060 and counter 1062 would be scaled accordingly to manage the increased number of inputs, maintaining the same clock-driven, sequential data retrieval process across the expanded memory architecture.

[00465] This daisy-chaining of microvaults, in conjunction with the multiplexing and counter-driven control system, exemplifies a modular and scalable approach to memory design in semiconductor devices. It allows for the customization of memory arrays to match the capacity and performance needs of a wide range of applications, from embedded systems to large-scale data centers, providing a versatile solution for modern computing challenges.

[00466] Fig. 11 shows a semiconductor assembly 1100 incorporating a daisy-chained configuration of microvaults in multiple semiconductor devices 1106, 1116 that are operatively connected to multiplexers and managed by counters for coordinated data selection and retrieval, in accordance with an embodiment of the present disclosure.

[00467] The present detailed description relates to Fig. 11 of the accompanying drawings, which illustrates an embodiment of an assembly 1100 as part of an integrated circuit. The assembly 1100 may be seen as a hierarchical structure that includes a bottom semiconductor device 1122, a middle semiconductor device 1116, and a top semiconductor device 1106 (each of these may be chiplets). Each semiconductor device is configured to interface with the others through a series of bumpless bonds, such as bumpless bonds 1128, 1129, 1158, 1159, 1160, 1161, 1162, and 1163, which facilitate electrical connectivity without the added profile of traditional bonding methods, thus enabling a compact and dense stacking of semiconductor layers.

[00468] The bottom semiconductor device 1122 includes a read address register 1126, which may be configured to store and communicate read addresses to microvaults located across the assembly 1100. The read address register 1126 communicates via an interconnect 1174, which serves as a conduit for signals directed to bumpless bonds 1128. These bonds in turn engage with bumpless bonds 1129 of the middle semiconductor device 1116, thus transferring the read addresses into the middle semiconductor device. The bottom semiconductor device 1122 also comprises a read data register 1124, which may serve as a repository for read data received. Read data is received through an interconnect 1176 that connects to bumpless bonds 1158, which are in communication with bumpless bonds 1159 of the middle semiconductor device 1116.

[00469] The middle semiconductor device 1116 serves as an intermediary layer within the assembly 1100, housing microvaults such as microvault 1132 and microvault 1118, each of which may be designed to store and rapidly provide access to data. These microvaults are linked to other components within the device via interconnects, such as interconnect 1130 and interconnect 1134, which guide the flow of read addresses and read data, respectively. The middle semiconductor device 1116 also features a read address register 1146, which receives

read addresses from interconnect 1130, and a read data register 1154, which collects read data from TSV 1152.

[00470] The multiplexer 1114, within the middle semiconductor device 1116 selects between various data streams. This multiplexer is controlled by a phase counter 1110, which determines the sequence of data selection based on the input received from the top semiconductor device 1106 via the TSV 1152. The read data register 1112 serves as a holding area for the selected data stream from the multiplexer 1114.

[00471] The top semiconductor device 1106 features a phase counter 1102 and a read data register 1104, which are used for coordinating data flow within the assembly 1100. The phase counter 1102, in conjunction with multiplexer 1150, dictates the output of read data from microvaults 1138 and 1164 based on the selected phase. The read data register 1104 captures the output from the multiplexer 1150, which is then relayed through interconnect 1108 to bumpless bonds 1162, facilitating communication with the middle semiconductor device 1116.

[00472] The assembly 1100 illustrates the integration of multiple microvaults across different semiconductor devices. For example, the microvault 1132 on the middle semiconductor device 1116 may receive read addresses from read address register 1146 via an interconnect 1134, path "1". Similarly, microvault 1118 may receive read addresses from the same register via an interconnect 1156, path "2". Microvaults 1138 and 1164 on the top semiconductor device 1106 receive read addresses via interconnect 1140 and paths "3" and "4", respectively, from read address register 1142, which is in communication with the middle semiconductor device 1116 via TSV 1136 and bumpless bonds 1160 and 1161.

[00473] Each microvault, such as 1132, 1118, 1138, and 1164, can potentially output read data to the multiplexer 1114 or 1150, where the data is then selected based on the configuration of the respective phase counter, 1110 or 1102. The selected data is temporarily stored in a read data register, either 1112 or 1104, before being transmitted down the assembly 1100 through the respective bumpless bonds and interconnects, ultimately reaching the read data register 1124 of the bottom semiconductor device 1122. This arrangement allows for a synchronized read-out of data from all microvaults, which may be essential in applications requiring parallel processing and high-speed data access.

[00474] The TSVs, such as 1136 and 1152, provide vertical connectivity across the semiconductor devices, enabling the integration of additional layers or functionalities atop the existing assembly 1100. These TSVs are coupled to various interconnects and bumpless bonds that establish the necessary pathways for signal transmission both within and between the semiconductor devices.

[00475] In some embodiments, the microvaults within the assembly 1100 may include various memory technologies, such as 3D-NAND or 3D-NOR structures, and are arranged to facilitate parallel processing and efficient data retrieval. Each microvault may include additional features, such as thermal management layers for heat dissipation, hardware-based encryption modules for data security, or power management circuits to optimize energy consumption.

[00476] Datapath 1 within the assembly 1100 exemplifies a route through which read addresses and corresponding read data are transmitted across the assembly, specifically directing operations from the read address register 1126 located on the bottom semiconductor device 1122 to the read data register 1124 within the same device.

[00477] The process begins with the read address register 1126 holding a specific read address. This address is sent through interconnect 1174, which acts as a channel for the signal. The read address is then transmitted to bumpless bonds 1128, which are meticulously designed to create a reliable electrical connection without the physical protrusion associated with traditional bonding methods. These bonds ensure a low-profile interface that preserves the compactness of the semiconductor stack.

[00478] The signal continues from bumpless bonds 1128 to engage with bumpless bonds 1129 of the middle semiconductor device 1116. The read address is carried forward by interconnect 1130, which delivers the address to the read address register 1146 of the middle semiconductor device. Read address register 1146, in turn, propagates the read address through interconnect 1134, designated as path "1" guiding the signal to the microvault 1132.

[00479] Upon receiving the read address, microvault 1132 accesses the requested data. This data is then outputted through interconnect 1170 and directed to the multiplexer 1114. In some embodiments, multiplexer 1114 functions as a selective switch that chooses between data streams based on the configuration determined by phase counter 1110. This phase counter may be designed to cycle through a sequence that dictates the timing and selection of data streams, ensuring that each microvault is read in a coordinated manner.

[00480] The selected data from multiplexer 1114 is then captured by read data register 1112, which holds the data momentarily. The data is subsequently sent via interconnect 1120, which carries the signal to bumpless bonds 1159. These bonds are part of a sophisticated electrical interconnection system that, along with bumpless bonds 1158 on the bottom semiconductor device 1122, enables vertical and horizontal integration within the semiconductor stack.

[00481] The signal, now in the form of read data, traverses from bumpless bonds 1159 to bumpless bonds 1158 and is finally introduced into interconnect 1176. This interconnect completes the connection to read data register 1124, which is configured to receive and hold the read data. The read data register 1124 may be equipped to retain the data for subsequent processing or external communication.

[00482] Datapath 2 within the assembly 1100 delineates a route specifically designed for the transmission of read addresses from the read address register 1126 on the bottom semiconductor device 1122 to the microvault 1118 located on the middle semiconductor device 1116 and the subsequent transfer of read data back to the read data register 1124 on the bottom device.

[00483] The journey commences at the read address register 1126, where a read address is held in preparation for dispatch. This register is a part of the semiconductor device's control mechanism, orchestrating the retrieval of data by issuing specific addresses to the memory units. From the read address register 1126, the read address is sent through the interconnect 1174, which provides a secure and reliable pathway for electrical signals within the integrated circuit.

[00484] The read address continues from the interconnect 1174 to bumpless bonds 1128, which offer a seamless and low-profile connection to the middle semiconductor device 1116 via the corresponding bumpless bonds 1129. These bonds maintain the signal's integrity during inter-layer communication and are designed to accommodate the requirements of modern semiconductor architectures.

[00485] The signal is then channeled via interconnect 1130 to the read address register 1146 within the middle semiconductor device 1116. The read address register 1146 acts as a secondary store and hold register from there, the read address is directed down interconnect 1156, labeled as path "2," which terminates at the microvault 1118.

[00486] Upon receipt of the read address, microvault 1118 accesses the corresponding data. This data retrieval process is facilitated by the microvault's internal architecture, which may comprise an array of memory cells optimized for rapid access and data stability. The read data is outputted from microvault 1118 and travels through interconnect 1172, which leads to the multiplexer 1114.

[00487] Multiplexer 1114 determines which data stream to forward based on input from the phase counter 1110. The phase counter 1110 operates in synchronization with the system clock or an external control signal, cycling through various states to control the selection process of the multiplexer 1114 in a precise and predictable manner.

[00488] The output of the multiplexer 1114, now carrying the selected read data, is conveyed to read data register 1112. This register temporarily stores the read data, acting as a buffer. The read data is then dispatched via interconnect 1120 towards bumpless bonds 1159.

[00489] Bumpless bonds 1159 form the interface with bumpless bonds 1158 on the bottom semiconductor device 1122, where the signal is transmitted downward through the assembly. The read data then traverses the interconnect 1176 to reach its final destination, the read data register 1124. The read data register 1124 captures the read data, holding it in readiness for further processing or transmission to external circuits.

[00490] Datapath 3 within the assembly 1100 is another communication route that illustrates the data transfer sequence from the read address register 1126 on the bottom semiconductor device 1122, through various components, ultimately to the microvault 1138 on the top semiconductor device 1106, and then back to the read data register 1124 on the bottom device.

[00491] The sequence initiates at the read address register 1126, which serves as the origin point for read addresses. The register 1126 securely holds the address before it is dispatched through the interconnect 1174. Interconnect 1174 acts as a dedicated channel, ensuring that the read address is conveyed with precision to the bumpless bonds 1128. These bumpless bonds 1128 facilitate a streamlined connection to the bumpless bonds 1129 of the middle semiconductor device 1116, preserving the integrity and compactness of the signal pathway.

[00492] Upon reaching the middle semiconductor device 1116, the read address is relayed through interconnect 1130 to the read address register 1146. The read address register 1146 acts as a juncture that further propagates the address signal through the Through-Silicon Via (TSV) 1136. The TSV 1136 is a vertical interconnect that pierces through the semiconductor substrate, providing a direct link from the middle semiconductor device 1116 to the top semiconductor device 1106, thus exemplifying the 3D integration capabilities of semiconductor design.

[00493] The read address ascends from TSV 1136 and emerges onto bumpless bonds 1160 on the middle semiconductor device 1116. The bumpless bonds 1160 are connected to the bumpless bonds 1161 of the top semiconductor device 1106. The address signal is conducted through interconnect 1140 to the read address register 1142 on the top device 1106.

[00494] The read address register 1142, upon receiving the read address, directs the signal along interconnect 1144. This path, denoted as "3," leads the address to the microvault 1138. Microvault 1138, designed for data storage, retrieves the requested information in

response to the read address. The read data is outputted through interconnect 1166, which feeds the data into the multiplexer 1150.

[00495] The multiplexer 1150 in the top semiconductor device 1106 is governed by the phase counter 1102, which dictates the selection of the data stream to be channeled to the read data register 1104. The chosen data stream is temporarily housed in the read data register 1104, where it awaits downstream transmission.

[00496] The read data departs from the read data register 1104 via interconnect 1108, which connects to bumpless bonds 1162. These bonds 1162 engage with the corresponding bumpless bonds 1163 on the middle semiconductor device 1116, transferring the read data to TSV 1152.

[00497] TSV 1152 operates as a vertical conduit, allowing the read data to traverse down into the middle semiconductor device 1116, where it is received by the read data register 1154. The read data register 1154 holds the read data momentarily before it is directed to the multiplexer 1114 through interconnect 1156.

[00498] The multiplexer 1114 in the middle semiconductor device 1116, coordinated by the phase counter 1110, selects the appropriate data for output. The read data is then channeled to the read data register 1112, where it is briefly stored. Following this, the read data travels via interconnect 1120 to bumpless bonds 1159.

[00499] The bumpless bonds 1159 form an interface with bumpless bonds 1158 on the bottom semiconductor device 1122. The read data signal is then carried through interconnect 1176, culminating its journey at the read data register 1124 on the bottom device.

[00500] Datapath 4 within the assembly 1100 is a path that establishes the flow of read addresses from the read address register 1126 on the bottom semiconductor device 1122 to the microvault 1164 located on the top semiconductor device 1106, and subsequently facilitates the movement of read data back down to the read data register 1124 on the bottom device.

[00501] This datapath begins at the read address register 1126, which is responsible for holding and issuing the read addresses necessary for data retrieval from the microvaults. The read address is sent from the register 1126 through interconnect 1174, a pathway that maintains signal integrity and facilitates electrical communication.

[00502] From interconnect 1174, the read address is directed to bumpless bonds 1128. These bonding areas create an interconnection between the bottom semiconductor device 1122 and the middle semiconductor device 1116 through bumpless bonds 1129. The design of these bumpless bonds facilitates data transmission.

[00503] Once the read address reaches the middle semiconductor device 1116, it is carried forward by interconnect 1130 to the read address register 1146. This register acts as an intermediary, preparing the address for its vertical ascent through the device stack. The address is then transmitted via the Through-Silicon Via (TSV) 1136 that facilitates vertical integration by providing a direct electrical link through the semiconductor substrate.

[00504] After ascending through TSV 1136, the read address emerges onto bumpless bonds 1160, which are aligned to connect with bumpless bonds 1161 on the top semiconductor device 1106. The read address then proceeds along interconnect 1140 to the read address register 1142 located on the top device.

[00505] The read address register 1142 serves to forward the read address to its final destination, the microvault 1164, through interconnect 1148, labeled as path "4". Microvault 1164, upon receiving the read address, retrieves the requested data, which is then outputted through interconnect 1168. This data is directed to the multiplexer 1150, which is under the control of phase counter 1102.

[00506] The phase counter 1102 determines which data stream is selected by the multiplexer 1150, which then sends the read data to the read data register 1104. The read data register 1104 acts as a temporary repository, holding the data until it can be sent downwards through the device stack.

[00507] The data leaves the read data register 1104 and travels via interconnect 1108 to bumpless bonds 1162. These bonds maintain a connection to bumpless bonds 1163 on the middle semiconductor device 1116. The read data is then transferred to TSV 1152, which carries the data vertically down to the read data register 1154 on the middle semiconductor device 1116.

[00508] The read data register 1154 temporarily holds the read data before it is fed into the multiplexer 1114 via interconnect 1156. The multiplexer 1114, coordinated by the phase counter 1110, channels the appropriate data stream to the read data register 1112. This register serves as a staging area for the read data, which is then sent through interconnect 1120 to bumpless bonds 1159.

[00509] Bumpless bonds 1159 interface with bumpless bonds 1158 on the bottom semiconductor device 1122 to provide a downward transmission of the read data. Finally, the signal is routed through interconnect 1176 and arrives at read data register 1124, where the data is made available for subsequent processing or external communication.

[00510] Fig. 12 illustrates a three-dimensional (3D) memory column 1200 configured as a 3D-NOR or 3D-AND structure, featuring a series of ferroelectric field-effect transistors

(FeFETs) 1202 with interconnected drain terminals 1204 linked to a common select line 1212 and individual gate terminals 1206 connected to respective read/write enable lines 1214 (e.g., 1214a for FeFET 1202a, all coupled to a common bit line, in accordance with an embodiment of the present disclosure.

[00511] Thus, Fig. 12 depicts a three-dimensional (3D) memory column, designated as element 1200, which can be configured in various embodiments as either a 3D-NOR or 3D-AND structure, providing flexibility in the application and use of the integrated circuit. This memory column is an assembly of multiple ferroelectric field-effect transistors (FeFETs), collectively referred to as fefets 1202, where each FeFET is indicated by elements such as 1202a, 1202b, 1202c, and 1202d, among others potentially present in the array.

[00512] Within each FeFET, such as 1202a, there is a drain terminal 1204a. This drain terminal is part of the memory cell's output path and is connected to a common select line 1212. In some embodiments, the common select line 1212 serves as a control mechanism that enables the selection of a particular FeFET for data read or write operations.

[00513] The gate terminal of each FeFET, exemplified by 1206a for FeFET 1202a, is individually connected to a respective read/write enable line, such as 1214a. This enables control of the FeFET's state, allowing it to be in a conductive (on) state for reading or writing data or in a non-conductive (off) state to prevent data flow. The presence of individual read/write lines for each FeFET may allow for precise control and operation of each memory cell.

[00514] Moreover, each FeFET, such as 1202a, comprises a source terminal, such as 1208a, which is coupled to a common bit line 1210. The bit line 1210 provides a conduit for data being written to or read from the FeFETs. In some embodiments, this bit line can be shared across multiple memory columns, which can facilitate parallel processing and increased data throughput.

[00515] In accordance with various embodiments of the present disclosure, the 3D memory column 1200 may incorporate additional elements and configurations to enhance performance and functionality. For instance, the 3D memory column 1200 may include insulating materials, conductive pathways, and other structural components not explicitly shown in Fig. 12 but which are inherent to the implementation of such 3D memory structures. The FeFETs 1202 may also exhibit variations in terms of material composition, structural dimensions, and electrical properties, contributing to a range of performance characteristics suitable for different applications.

[00516] Furthermore, the memory column 1200 may be incorporated into larger memory arrays, forming part of a memory module or system. These arrays can be arranged in various configurations, such as rows and columns, to create a matrix that efficiently addresses the demands of high-density data storage. The memory column 1200 can also be interfaced with other circuit elements and control logic, which may govern the operation of the memory array, including data management protocols, error correction algorithms, and power optimization strategies.

[00517] In some embodiments, the memory column 1200 may be fabricated using advanced semiconductor manufacturing techniques, such as photolithography, etching, deposition, and planarization processes. The choice of materials for the FeFETs, including the ferroelectric material, the semiconductor channel, and the conductive elements, can be selected based on desired electrical characteristics, such as charge retention, switching speed, and energy efficiency.

[00518] The 3D memory column 1200, as illustrated in Fig. 12, may include FeFETs, such as 1202, fabricated from a variety of materials that provide the necessary electrical and physical properties to achieve the desired functionality. For instance, in some embodiments, the channel layer of each FeFET in the FeFETs 1202 could be constructed from materials such as Indium Gallium Zinc Oxide (IGZO) or other Amorphous Oxide Semiconductors (AOS) like Zinc Tin Oxide or Indium Tungsten Oxide (IWO). These materials are selected for their electronic properties, such as carrier mobility and stability.

[00519] The ferroelectric material rigidly coupled to the channel layer in each FeFET may comprise hafnium zirconium oxide (HfZrO₂) or other transition metal oxides, perovskites, etc. These ferroelectric materials are chosen for their ability to maintain a polarization state when an electric field is applied, which is used for the non-volatile memory characteristics of the FeFETs. The thickness, crystalline structure, and stoichiometry of the ferroelectric layer can be controlled to achieve the desired coercive voltage, remanent polarization, and other electrical parameters for reliable data storage and retrieval.

[00520] The drain 1204 and source 1208 terminals of the FeFETs 1202 are connected to the common select line 1212 and common bit line 1210, respectively. These common lines may be formed from conductive materials such as tungsten, titanium nitride, or other metals and metal alloys that provide low-resistance pathways for electrical signals. The configuration of these terminals and their respective common lines ensures that the FeFETs can be accessed and controlled effectively during operation.

[00521] Each gate terminal, such as the gate 1206 of the FeFET 1202a, is connected to its respective read/write enable line, such as 1214a. The gate terminals help control the state of the FeFET, and the materials chosen for these terminals may include various conductive materials that can provide a reliable electrical interface with the ferroelectric material. The read/write enable 1214 lines are designed to deliver suitable voltage levels to the gates 1206 of the FeFETs 1202 for switching between states.

[00522] The memory column 1200 as a whole is designed to support a range of operating parameters. In some embodiments, these parameters may include, but are not limited to, an off-state current of less than 10^{-8} amps per centimeter cubed, an on-state current greater than 10^{-7} amps per centimeter cubed, and a channel mobility that is maintained despite the presence of the ferroelectric layer. The channel layer's thickness can be less than 30 nm to ensure high device density, while the ferroelectric layer's characteristics, such as coercive voltage and remanent polarization, are optimized to provide the necessary memory functionality.

[00523] In some embodiments, the FeFETs 1202 may include additional materials or dopants to enhance their electrical properties. For instance, dopants such as gallium (Ga), indium (In), or zinc (Zn) may be introduced into the channel layer to modulate the carrier concentration or to adjust the threshold voltage of the FeFETs. Similarly, the ferroelectric layer may include dopants like lanthanum (La) or niobium (Nb) to adjust its ferroelectric properties.

[00524] In other embodiments, the 3D memory column 1200 may be integrated with additional semiconductor devices and structures to form complex memory systems. These systems can provide storage capabilities and support various memory architectures.

[00525] Fig. 13 depicts a three-dimensional (3D) memory column 1300 configured as a 3D-NAND structure, consisting of a vertical stack of ferroelectric field-effect transistors (FeFETs) 1302, each with source 1304 and drain 1308 terminals. The source 1304 of each FeFET, such as 1304a for FeFET 1302a, is coupled to the start of a bit line 1310 or connected to the drain of the preceding FeFET, exemplified by source 1304b of FeFET 1302b coupled to drain 1308a of FeFET 1302a. Each FeFET includes a gate 1306, such as 1306a for FeFET 1302a, connected to a respective read/write enable line, illustrated by 1314a for FeFET 1302a, in accordance with an embodiment of the present disclosure.

[00526] The 3D memory column 1300 is composed of a series of vertically stacked Field-Effect Transistors (FeFETs), identified collectively as FeFETs 1302. These transistors, which include FeFETs 1302a, 1302b, 1302c, 1302d, and so on, are characterized by their incorporation of ferroelectric materials within their gate structure. Each FeFET in the series is of the memory column contributes to the memory storage capabilities of the device.

[00527] In the depicted embodiment, each FeFET, such as FeFET 1302a, includes a source terminal 1304, for instance, source 1304a, which is coupled to a bit line 1310. The bit line 1310 serves as a conduit for electrical signals that are used to read from and write to the memory cell associated with FeFET 1302a. In scenarios where FeFET 1302a is not the bottom-most transistor in the column, its source 1304b may be connected to the drain 1308a of the immediately preceding FeFET, such as FeFET 1302a, facilitating a serial connection that defines the vertical NAND architecture.

[00528] Each FeFET within the FeFETs 1302 is further equipped with a gate terminal 1306, exemplified by gate 1306a for FeFET 1302a. This gate terminal 1306 is coupled to a respective read/write enable line, exemplified by 1314a for FeFET 1302a. The read/write enable line 1314a is responsible for controlling the state of the FeFET, allowing it to either conduct or prevent the flow of current through the device, thereby enabling the writing or reading of data.

[00529] Moreover, each FeFET of the FeFETs 1302 also includes a drain terminal 1308, such as drain 1308a for FeFET 1302a, which is typically connected to the source of the subsequent FeFET in the vertical stack. This arrangement ensures that the charge stored in the ferroelectric material of the gate can modulate the current flowing from the source to the drain, allowing for the storage and retrieval of data.

[00530] The memory column 1300 within Fig. 13 is indicative of a memory architecture that can be utilized in various applications, from portable electronics to enterprise-level data storage systems. In some embodiments, the ferroelectric material used in the FeFETs may include various compositions, such as hafnium oxide, zirconium oxide, or any combination thereof, which can be doped with elements such as lanthanum or yttrium to adjust the ferroelectric properties as required.

[00531] In some variations, the 3D memory column 1300 can incorporate additional features that enhance performance, reliability, or manufacturability. For instance, the FeFETs 1302 may include protective layers to shield the ferroelectric material from environmental factors or process-induced damage. The column 1300 may also be integrated with other circuit elements, such as capacitors or diodes, to facilitate operations like charge pumping or to provide additional functionality within the memory array.

[00532] The 3D memory column 1300 may be fabricated from a variety of materials that confer specific electrical properties to enhance device performance. In some embodiments, the channel layer of each FeFET may be formed from materials such as Indium Gallium Zinc

Oxide (IGZO). Other materials for the channel layer could include Amorphous Oxide Semiconductors (AOS) like Zinc Tin Oxide or Aluminum Zinc Oxide.

[00533] The ferroelectric layer within the FeFETs 1302 may comprise materials such as Hafnium Zirconium Oxide (HfZrO₂). The ferroelectric layer's thickness and material composition can be controlled through methods like Atomic Layer Deposition (ALD) to achieve the desired coercive voltages, remanent polarizations, and endurance characteristics. In some implementations, the coercive voltage of the ferroelectric layer may be tuned to be between -3 Volts to +3 Volts, facilitating low-voltage operation of the memory devices.

[00534] The source and drain terminals of the FeFETs 1302 may be composed of conductive materials such as Tungsten or Titanium Nitride. These materials may also be selected to optimize the contact resistance with the channel layer, reducing overall power consumption and improving the Ion/Ioff ratio of the device.

[00535] Additionally, the FeFETs 1302 may be engineered to exhibit specific electrical parameters. For instance, the channel layer's thickness may be less than 30 nm in some embodiments. In some embodiments, the channel layer may demonstrate a carrier concentration of 10^{17} to 10^{20} per centimeter-cubed, which can be adjusted through doping with elements such as Gallium, Indium, or Zinc to modulate the electrical properties.

[00536] The memory cells formed by the FeFETs 1302 within the 3D memory column 1300 may also target operational parameters such as read and write latencies, endurance, and energy consumption. For example, read and write operations may be executed with energies less than 10 picojoules and within timeframes less than 20 nanoseconds, contributing to the low power and high-speed attributes of the memory column.

[00537] Furthermore, the 3D-NAND configuration of the memory column 1300 may be designed to achieve a high off-state resistance to on-state resistance ratio (R_{off}/R_{on}), which is critical for distinguishing between different data states and ensuring reliable data retention. This ratio may be about 10^3 or greater, which helps to maintain a high signal-to-noise ratio during memory operations.

[00538] The FeFETs 1302 in the memory column 1300 may also be designed to sustain a high degree of reliability, with endurance ratings greater than or equal to 10^{11} cycles, ensuring the longevity and durability of the memory device. This endurance is complemented by the ferroelectric layer's ability to maintain data retention for at least 1 minute at room temperature, which is 25°C.

[00539] Fig. 14 depicts a three-dimensional (3D) memory column configured as a 3D-NAND with an integrated pass gate, in accordance with an embodiment of the present

disclosure. This figure illustrates a series of ferroelectric field-effect transistors (FeFETs) 1402, each including source 1404 and drain 1408 terminals, gated by respective gate terminals 1406 and coupled to read/write enable lines 1414. The FeFETs are interconnected, forming a vertical memory structure with pass gates 1418 linked to a pass gate line 1416.

[00540] Thus, Fig. 14 illustrates a three-dimensional (3D) memory column, designated as element 1400, which can be configured as a 3D-NAND structure with an integrated pass gate. This configuration enables enhanced control over individual memory cells within the 3D structure, potentially improving read/write operations and facilitating efficient memory management.

[00541] In detail, the 3D memory column 1400 comprises multiple ferroelectric field-effect transistors (FeFETs), collectively referred to as FeFETs 1402. Each FeFET within the 1402 series, such as 1402a, 1402b, 1402c, 1402d, etc., is a constituent memory cell of the 3D memory column 1400. These FeFETs are utilized for their ability to retain data in a non-volatile manner due to the ferroelectric properties of their gate material, which allows for data retention without continuous power supply for a time.

[00542] Each FeFET in the series 1402 includes a source, exemplified by source 1404a for FeFET 1402a. The source 1404 for each FeFET is either coupled to a bit line, illustrated as bit line 1410 for FeFET 1402a, or is connected to the drain of the preceding FeFET in the series. For instance, source 1404b of FeFET 1402b is electrically coupled to drain 1408a of FeFET 1402a. This serial connection forms the basis for the daisy-chain configuration, which is used in NAND architectures, allowing for sequential access to the array of FeFETs.

[00543] Furthermore, each FeFET within the FeFETs 1402 is equipped with a gate terminal, such as gate 1406a for FeFET 1402a. The gates of the FeFETs are connected to their respective read/write enable lines, which are depicted as element 1414 in the figure. For example, gate 1406a of FeFET 1402a is influenced by read/write enable line 1414a. These enable lines control the application of appropriate voltages for the reading and writing of data.

[00544] Additionally, each FeFET in the FeFETs 1402 series includes a drain, such as drain 1408a for FeFET 1402a. This drain is connected to the source of the subsequent FeFET in the series, thus establishing the continuity for the columnar structure of the 3D memory stack.

[00545] In some embodiments, each FeFET of the FeFETs 1402 incorporates a pass gate, for example, pass gate 1418a, which is connected to a pass gate line, represented by 1416 in the figure. The pass gate line 1416 is a conductive pathway that provides electrical signals to control the pass gates 1418 of the FeFETs. The inclusion of pass gates in the FeFETs may

allow for improved isolation between memory cells during operation, thereby reducing interference and potentially enhancing the reliability of data storage and retrieval.

[00546] The 3D memory column 1400, as depicted in Fig. 14 also encompasses a diverse range of materials and parameters that could be utilized to optimize its performance in various embodiments. Each FeFET 1402 within the column could be fabricated using a variety of semiconductor materials. For instance, the channel layer of the FeFETs could be formed from materials such as Indium Gallium Zinc Oxide (IGZO).

[00547] The ferroelectric layer, which is a defining characteristic of the FeFETs, may be composed of materials like Hafnium Zirconium Oxide (HfZrO₂) or other perovskite materials, which are known for their remanent polarization. This property determines the data retention capabilities of the FeFETs. The coercive voltage of this layer, which affects the energy required to switch the polarization state, is another critical parameter that can be adjusted according to the requirements of the specific application, with a range in one embodiment being between -3 Volts to 3 Volts.

[00548] The source and drain terminals of the FeFETs, which include elements 1404 and 1408, respectively, could be composed of conductive materials such as Tungsten or Titanium Nitride. These materials provide pathways for current flow, which is for switching. The read/write enable lines 1414, which control the gates 1406 of the FeFETs, could also be fabricated from similar materials, ensuring consistent electrical characteristics throughout the device.

[00549] In terms of the physical parameters, the channel layer thickness may be less than 30 nm in thickness. The electron mobility within these channel layers may be maintained at a predetermined level even when the layer is less than 30nm in thickness.

[00550] The pass gates 1418 may be manufactured using low-resistance materials to enable quick switching times, which is beneficial when the memory column is accessed frequently during operation.

[00551] Fig. 15 illustrates a three-dimensional (3D) memory column 1500, which may be configured as either a 3D-NOR or a 3D-AND structure with independent Read/Write enable capabilities, in accordance with an embodiment of the present disclosure. This memory column encompasses a series of vertically aligned FeFETs 1502, such as FeFETs 1502a, 1502b, 1502c, 1502d, and so forth, each integrated with a source 1504 (e.g., source 1504a for FeFET 1502a) linked to a respective read enable line 1520 (e.g., read enable line 1520a for FeFET 1502a), and a gate 1506 (e.g., gate 1506a for FeFET 1502a) connected to a corresponding write enable line 1522 (e.g., write enable line 1522a for FeFET 1502a). All FeFETs within the column share

a common bit line 1510 connected to their drains 1508, enabling the column to perform coordinated memory operations.

[00552] Fig. 15 presents a detailed depiction of a three-dimensional (3D) memory column 1500, which can be configured as a 3D-NOR or 3D-AND structure with independent Read/Write enable functionalities. This memory column is an assembly of Field-Effect Transistors with ferroelectric gate layers, commonly referred to as FeFETs 1502, which are individually identified, for example, as 1502a, 1502b, 1502c, 1502d, etc., each representing a memory cell within the column.

[00553] In the illustrated embodiment, each FeFET 1502 includes a source 1504, such as source 1504a corresponding to FeFET 1502a. The source 1504 is designed to be electrically coupled to a respective read enable line 1520, such as read enable line 1520a which is dedicated to FeFET 1502a. The read enable line 1520 functions to selectively activate the FeFET 1502 for reading operations, allowing the readout of stored data from the memory cell.

[00554] Additionally, each FeFET 1502 is equipped with a gate 1506, exemplified by gate 1506a for FeFET 1502a. The gate 1506 is connected to a respective write enable line 1522, such as write enable line 1522a, which is specific to FeFET 1502a. The write enable line 1522 serves to selectively activate the FeFET 1502 for writing operations, enabling the storage of data within the memory cell.

[00555] Furthermore, each FeFET 1502 includes a drain 1508, for instance, drain 1508a affiliated with FeFET 1502a. The drain 1508 is connected to a common bit line 1510. The bit line 1510 acts as a conduit for transferring data to and from the memory cells during read and write operations. The commonality of the bit line 1510 across multiple FeFETs 1502 signifies that data from any activated memory cell can be routed through this shared path.

[00556] In some embodiments of the memory column 1500, the configuration of the FeFETs 1502 allows for a high density of memory cells vertically stacked within a compact footprint.

[00557] The ferroelectric material utilized in the gate 1506 of the FeFETs 1502 may comprise various compositions, such as hafnium oxide-based materials, which can be deposited using atomic layer deposition techniques. The ferroelectric property of the material allows for data retention, enabling the memory cells to maintain stored information even when power is not supplied.

[00558] The source 1504, gate 1506, and drain 1508 of each FeFET 1502 can be fabricated from materials that provide predetermined electrical performance. These materials may include metals such as tungsten or copper, or metal nitrides such as titanium nitride.

[00559] The read enable lines 1520 and write enable lines 1522 can be designed to minimize crosstalk and interference between adjacent lines, in some embodiments. In some specific embodiments, shielding layers or insulating materials may be included to further isolate the signal paths.

[00560] Furthermore, the described memory column 1500 may be integrated within a larger semiconductor device, such as a processor or a storage module. It may form part of a system-on-chip (SoC) or be included in a multi-chip module (MCM), contributing to a data storage and retrieval system.

[00561] The materials that constitute the FeFETs 1502 within the memory column 1500 are selected to provide specific electrical and physical properties to optimize the performance of the integrated circuit. For instance, the channel layer in each FeFET may be formed from advanced semiconductor materials, such as Indium Gallium Zinc Oxide (IGZO) or other Amorphous Oxide Semiconductors (AOS) like Zinc Tin Oxide or Cadmium Oxide. These materials are chosen for their excellent electron mobility characteristics and stability.

[00562] The ferroelectric layer, integral to the FeFETs 1502, may be fabricated from various ferroelectric materials that exhibit suitable polarization properties. Materials such as Hafnium Zirconium Oxide (HfZrO₂) or Lead Zirconate Titanate (PZT) could be utilized. These materials can be doped with elements such as Lanthanum, Yttrium, or other suitable dopants to modify their ferroelectric properties, such as coercive voltage, remanent polarization, and crystallization temperature. The ferroelectric layer's thickness and material composition may be adjusted to achieve desired memory characteristics, such as write endurance and retention time, while ensuring the layer remains compatible with the overall semiconductor manufacturing process, or other considerations, etc.

[00563] The source 1504, gate 1506, and drain 1508 terminals of the FeFETs 1502 may be composed of conductive materials like Tungsten, Titanium Nitride, Nickel, or Molybdenum. Connections to the read enable lines 1520 and the write enable lines 1522 may be facilitated through conductive vias or contacts.

[00564] The read enable lines 1520 and write enable lines 1522, along with the common bit line 1510, may be patterned using lithographic techniques to achieve the predetermined precision and alignment for proper functionality. These lines may be insulated from one another using dielectric materials like Silicon Dioxide (SiO₂), Silicon Nitride (Si₃N₄), or low-k dielectrics to reduce parasitic capacitance and crosstalk.

[00565] Each element within the memory column 1500 may consider factors such as line width, spacing, and aspect ratio to ensure manufacturability, functionality, and/or other

goals or characteristics. The materials and processes used in the construction of the memory column 1500 are chosen to ensure compatibility with standard semiconductor fabrication techniques, such as photolithography, etching, deposition, and annealing, while also enabling the integration of materials and structures.

[00566] The fabrication of the FeFETs 1502 within the memory column 1500 may involve deposition techniques such as atomic layer deposition (ALD), chemical vapor deposition (CVD), or physical vapor deposition (PVD) to create uniform and/or non-uniform layers.

[00567] Fig. 16 presents a cross-sectional view of a 3D memory structure, designated as 1600, configured as a single-port 3D NAND, in accordance with an embodiment of the present disclosure. The structure includes a first vertical structure 1608a and a second identical vertical structure 1608b, each comprising a dielectric column 1610a, 1610b, a channel column 1612a, 1612b disposed around the dielectric column, and a ferroelectric column 1614a, 1614b disposed around the channel column. A series of horizontal gate-electrode layers 1606a-c are disposed at predetermined distances from each other, adjacent to the ferroelectric column along the length of the vertical structures. The assembly further includes a drain select layer 1602 and a source select layer 1604, with respective end dielectric columns 1618a, 1618b, and 1616a, 1616b positioned at the interfaces with the vertical structures, illustrating a detailed and intricate design for high-density data storage.

[00568] Thus, fig. 16 provides a cross-sectional view of a three-dimensional (3D) memory structure, designated as 1600, which is configured as a single-port 3D NAND architecture. This structure incorporates a pair of vertical structures, 1608a and 1608b, which may be fabricated to be substantially identical, as indicated by their respective subscripts a and b, suggesting the potential for a modular and scalable memory array design.

[00569] Each vertical structure, exemplified by the first vertical structure 1608a, includes a dielectric column 1610a. The dielectric column may adopt various geometric forms—it can be cylindrical, substantially cylindrical, or feature curves. Additionally, it may present a tapered form, having different diameters at each end, implying a design that narrows towards the top. Both solid and hollow configurations of the dielectric column are contemplated within the scope of the disclosure, offering design flexibility for different electrical and structural requirements.

[00570] Surrounding the dielectric column 1610a is a channel column 1612a, which is the locus for charge carriers during device operation. The channel column is also described as

potentially cylindrical, substantially cylindrical, or feature curves and/or and may exhibit similar variations in diameter along its length as the dielectric column.

[00571] Enveloping the channel column 1612a is a ferroelectric column 1614a, which extends along the length of the channel column but may recede at the ends, thereby meaning the ferroelectric column 1614 does not extend the entire length of the channel column 1612a.

[00572] Intersecting with the vertical structures is a series of horizontal gate-electrode layers, 1606a-c, which are positioned at predetermined distances from one another. These layers play a role in controlling the operational states of the device by influencing the electric field within the ferroelectric column.

[00573] Atop the 3D memory structure 1600 sits a drain select layer 1602, parallel to the horizontal gate-electrode layers 1606. Where the drain select layer 1602 meets the vertical structures 1608a, 1608b, end dielectric columns, 1618a and 1618b, are discernible. These end dielectric columns 1618 interface with the channel column 1612 and the drain select layer 1602, contributing to the isolation and control of the charge carriers within the channel column. They may contact the ferroelectric layer 1614, as they envelop the channel column 1612 at different positions along its length.

[00574] Similarly, a source select layer 1604 is situated at the bottom of the structure 1600, again parallel to the horizontal gate-electrode layers 1606. Corresponding end dielectric columns, 1616a and 1616b, are present where the source select layer 1604 interfaces with the vertical structures, serving analogous functions to the end dielectric columns 1618 near the drain select layer 1602.

[00575] The horizontal gate-electrode 1606 layers could be constructed from a range of conductive materials, including metals and metal compounds, which may offer different work functions, conductivity, and compatibility with other materials in the structure. Similarly, the ferroelectric column 1614 might incorporate a variety of ferroelectric materials each with its unique polarization characteristics, coercive fields, and dielectric constants, affecting the device's memory retention and switching behaviors.

[00576] The channel column 1612 materials can be chosen based on their electronic properties, such as carrier mobility and bandgap, to achieve the desired levels of on-state and off-state current. The dielectric column 1610 provides the electrical insulation necessary to prevent leakage currents and ensure the proper functioning of the device.

[00577] The dielectric column, such as 1610a for the first vertical structure, may be constructed from materials that offer insulating properties to mitigate any potential leakage

currents. Choices for the dielectric material may be Hafnium Oxide (HfO₂) or Silicon Dioxide (SiO₂).

[00578] Surrounding the dielectric column, the channel column (1612a) has channel material can be selected from a wide range of semiconducting materials that offer predetermined carrier mobility. For example, Indium Gallium Zinc Oxide (IGZO) can be used for its electrical properties. The channel layer's thickness may vary, with some embodiments considering a thickness less than 30 nm. This thickness is chosen to achieve a predetermined electrical performance. The ferroelectric column, like 1614a, may include perovskite structures, such as Lead Zirconate Titanate (PZT).

[00579] The horizontal gate-electrode layers, represented by 1606a-c, are composed of conductive materials that facilitate the application of an electric field to the ferroelectric column, such as Tungsten or Titanium Nitride, which may be chosen for their electrical behavior. The selection of gate-electrode materials also takes into consideration factors such as work function, thermal stability, and ease of integration with the existing semiconductor manufacturing processes.

[00580] The drain and source select layers, 1602 and 1604 respectively, are incorporated to enable the addressing of individual memory cells within the array. The materials used for these layers are chosen for their conductive properties and compatibility with the channel and ferroelectric materials. The design of these layers may also incorporate considerations for reducing parasitic capacitance and ensuring swift data access.

[00581] The end dielectric columns, like 1618a and 1616a, provide electrical insulation at the ends of the channel column, where the ferroelectric material does not extend.

[00582] The disclosed embodiments within the 3D memory structure 1600 outline an assembly capable of providing data storage. The design allows for variations in structural dimensions, such as the diameter of the cylindrical columns, which can be uniform or tapered. Additionally, the option for solid or hollow configurations may be used.

[00583] Fig. 17 shows a 3D memory structure that is a dual-port 3D NAND arrangement in accordance with an embodiment of the present disclosure. The three-dimensional (3D) memory structure illustrated in Fig. 17, referred to as 3D memory structure 1700, exemplifies a dual-port 3D NAND arrangement to provide a memory functionality. This structure is characterized by two primary vertical formations, designated as the first vertical structure 1708a and the second vertical structure 1708b, which may be identical or near identical, as evidenced by the designating subscripts 'a' and 'b'.

[00584] The first vertical structure 1708a includes a hollow or solid, tapered pass-gate electrode column 1718a that is substantially cylindrical in shape. The pass-gate electrode column 1718a may be made of titanium nitride and may have a larger diameter at the bottom end compared to the top end.

[00585] Surrounding the pass-gate electrode column 1718a is a dielectric column 1710a that may be made of hafnium oxide. The dielectric column 1710a is also substantially cylindrical with a slightly tapered shape, having a marginally larger diameter at the top. The dielectric column 1710a provides electrical isolation between the pass-gate electrode and subsequent layers.

[00586] Disposed around the dielectric column 1710a is a cylindrical channel column 1712a that may be made of IGZO semiconductor material. The channel column 1712a features curves along its length and has a uniform diameter throughout. The thickness of the channel column may be less than 30 nm.

[00587] Enclosing the channel column 1712a is a PZT ferroelectric column 1714a that covers most of the length of the channel column 1712a but recedes at the ends, leaving a portion of the channel column 1712a uncovered. The ferroelectric column 1714a is substantially cylindrical and contains lead, zirconium and titanium as key elemental constituents.

[00588] The vertical structures 1708a and 1708b traverse through several horizontal gate-electrode layers 1706a, 1706b and 1706c that may be made of tungsten, which are positioned at fixed intervals to form an interconnected grid layout. These layers influence the electric field within the ferroelectric column 1714a during memory operations.

[00589] At the top of the memory structure 1700, a drain select layer 1702 (e.g., titanium nitride) runs parallel to the horizontal gate-electrode layers 1706. Where the drain select layer 1702 intersects the vertical structures 1708a and 1708b, end dielectric columns 1718a and 1718b are visible. These end columns (e.g., made of HfO₂) touch the ferroelectric column 1714a on one end and surround the uncovered portion of channel column 1712a, providing insulation.

[00590] Similarly at the bottom of the structure 1700, a source select layer 1704 (e.g., made of tungsten), also parallel to the electrode layers 1706, interfaces with the vertical structures. End dielectric columns 1716a and 1716b can be observed at these intersection points, enclosing the open ends of the channel columns 1712a and 1712b.

[00591] Within the hollow region of the pass-gate electrode columns 1718a and 1718b at the ends, a thin dielectric horizontal layers 1720a and 1720b may be placed near the bottom terminals (e.g., HfO₂). These layers seal off the bottom open ends of the vertical hollow voids.

[00592] Fig. 18 illustrates a 3D memory structure 1800 that can be configured as a 3D NOR Vertical Transistor memory array. The 3D memory structure 1800 comprises a first vertical structure 1808a and an identical (or substantially identical) second vertical structure 1808b arranged adjacent to one another.

[00593] The first vertical structure 1808a includes a vertical plug column 1802a that provides an electrical connection to the lower portions of the 3D memory structure. The vertical plug column 1802a may have a uniform diameter along its entire length or may have a larger diameter on its lower end than on its upper end. The plug column 1802a can be fabricated as a solid column or as a hollow column in various embodiments.

[00594] Disposed adjacent to the vertical plug column 1802a is a source electrode column 1804a and a drain electrode column 1816a. The source electrode column 1804a and drain electrode column 1816a provide electrical connections to the source and drain nodes of the vertical transistors formed along the vertical structure 1808a. The source electrode column 1804a and drain electrode column 1816a may be comprised of various conducting materials including, but not limited to, tungsten, titanium nitride, tantalum nitride, nickel, molybdenum, platinum, palladium, cobalt, gold, aluminum, copper, hafnium, hafnium nitride, iridium, iridium oxide, ruthenium, ruthenium oxide, silicides, graphene, carbon nanotubes, doped polysilicon, indium tin oxide, silver, aluminum-doped zinc oxide, gallium, gallium arsenide, indium gallium zinc oxide, metal alloys such as AlCu and TiW, and conducting polymers.

[00595] Surrounding the vertical plug column 1802a, source electrode column 1804a, and drain electrode column 1816a is a channel column 1812a that provides the semiconductor channel region for the vertical transistors along the first vertical structure 1808a. The channel column 1812a may be formed from materials including, but not limited to, indium gallium zinc oxide (IGZO), indium zinc oxide (IZO), zinc tin oxide (ZTO), aluminum zinc oxide (AZO), indium tungsten oxide (IWO), gallium zinc oxide (GZO), hafnium indium oxide (HIO), cadmium oxide (CdO), polysilicon, polygermanium, cadmium selenide (CdSe), copper indium gallium selenide (CIGS), crystalline silicon, crystalline germanium, gallium arsenide (GaAs), indium phosphide (InP), indium antimonide (InSb), silicon carbide (SiC), gallium nitride (GaN), zinc oxide (ZnO), pentacene, P3HT, polythiophene, PPV, graphene, carbon nanotubes (CNTs), methylammonium lead halides, cesium lead halides, lead sulfide (PbS), lead selenide (PbSe), cadmium selenide (CdSe), indium arsenide (InAs), and other semiconducting materials.

[00596] Surrounding the channel column 1812a is a ferroelectric column 1814a that provides the gate dielectric for the vertical transistors along the first vertical structure 1808a.

The ferroelectric column 1814a may be comprised of ferroelectric materials including, but not limited to, perovskite oxides, lead zirconate titanate (PZT), barium titanate (BaTiO_3), strontium titanate (SrTiO_3), bismuth ferrite (BiFeO_3), potassium niobate (KNbO_3), lithium niobate (LiNbO_3), lithium tantalate (LiTaO_3), sodium bismuth titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$), bismuth titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), bismuth zinc niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$), bismuth lanthanum titanate (BiLaTiO_3), bismuth nickel titanate (BiNiTiO_3), PMN-PT, PLZT, neodymium-doped bismuth titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$), hafnium-based oxides like hafnium oxide (HfO_2) and doped hafnium oxide, tungsten bronze structure materials, barium strontium niobate (BSN), lead barium niobate (PBN), potassium tantalate niobate (KTN), bismuth titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), strontium bismuth tantalate (SBT), calcium bismuth niobate (CBN), organic ferroelectrics like PVDF, TrFE and P(VDF-TrFE) copolymers, aurivillius phase oxides, rare earth manganites like YMnO_3 , lanthanum-modified PLZT, nickel manganese oxide (NiMnO_3), relaxor ferroelectrics like PMN, PST and PIN, multiferroic materials like TbMnO_3 , EuTiO_3 , SbSI , GeTe , SnTe , PZT thin films, SBT thin films, HfO_2 -based thin films, layered superlattices, and $\text{PbTiO}_3/\text{SrTiO}_3$.

[00597] The 3D memory structure 1800 further comprises multiple horizontal gate electrode layers 1806 including layers 1806a, 1806b, 1806c etc. The horizontal gate electrode layers 1806 are disposed at regular intervals along the vertical structures 1808 and provide the gate electrodes for the vertical transistors. The gate electrode layers 1806 may be formed from materials such as tungsten, titanium nitride, tantalum nitride, nickel, molybdenum, platinum, palladium, cobalt, gold, aluminum, copper, hafnium, hafnium nitride, iridium, iridium oxide, ruthenium, ruthenium oxide, silicides, graphene, carbon nanotubes, doped polysilicon, indium tin oxide, silver, aluminum-doped zinc oxide, gallium, gallium arsenide, indium gallium zinc oxide, metal alloys such as AlCu and TiW , and conducting polymers.

[00598] Each of the horizontal gate electrode layers 1806 may be surrounded by an oxide/nitride/oxide (ONO) stack 1810, such as 1810a surrounding gate electrode layer 1806a, to provide insulation between the gate electrodes.

[00599] The second vertical structure 1808b in the 3D memory structure 1800 is identically configured as the first vertical structure 1808a. The two vertical structures 1808a and 1808b are arranged horizontally adjacent to each other with a spacing that allows integration of the gate electrode layers 1806 and ONO stacks 1810. Together, the first and second vertical structures 1808a, 1808b along with the horizontal gate electrode layers 1806 can be configured as a 3D NOR memory architecture.

[00600] Fig. 19 illustrates an embodiment of a planar FeFET 1900. The FeFET 1900 comprises a substrate 1910 upon which various layers and components are formed. The substrate 1910 may be comprised of silicon or other suitable semiconductor materials. Disposed on top of the substrate 1910 is a layer of TiN 1912. The TiN layer 1912 may act as an electrode and can be deposited by sputtering or other suitable deposition techniques.

[00601] On top of the substrate 1910 and TiN layer 1912, a layer of HZO 1908 is disposed. HZO 1908 comprises hafnium, zirconium, and oxygen and can exhibit ferroelectric properties. The HZO 1908 may be deposited by ALD, CVD, PVD or other suitable deposition methods and can have a thickness in the range of 5-50 nm. Acting as a ferroelectric layer, the HZO 1908 enables the non-volatile storage of data in the FeFET 1900.

[00602] Deposited conformally on top of the HZO 1908 is a layer of IWO 1906. IWO 1906 comprises indium, tungsten, and oxygen. It can be deposited by sputtering or other suitable techniques and may have a thickness in various ranges. The IWO 1906 layer serves as a control oxide layer in the FeFET 1900.

[00603] On top of the IWO 1906 layer, a drain contact 1904 and source contact 1914 are formed. The drain contact 1904 and source contact 1914 may comprise metals such as copper, aluminum, or alloys thereof and can be deposited by PVD, CVD or other suitable methods. The drain contact 1904 and source contact 1914 allow electrical connection to the FeFET 1900. They may have thicknesses in the range of 50-500 nm.

[00604] In operation, a voltage applied to the drain 1904, source 1914, and TiN gate contact 1912 can control the ferroelectric polarization of the HZO 1908 layer. The polarization state can be used to store information in a non-volatile manner, enabling memory storage capabilities. The IWO 1906 layer helps improve the switching speed and endurance of the FeFET 1900. Overall, the layered structure shown in Fig. 19 enables a FeFET 1900 suitable for non-volatile memory applications.

[00605] Fig. 20 presents the transfer characteristics of a Ferroelectric FET (FeFET) device, illustrating the relationship between the gate voltage (V_{GS}) on the x-axis and the resulting drain current (I_D) on the y-axis. Fig. 20 may show the characteristics of a FeFET as disclosed herein. The x-axis spans from -1V to 1V, while the y-axis, on a logarithmic scale, displays current values from $10^{-12} \text{A}/\mu\text{m}$ to $10^{-4} \text{A}/\mu\text{m}$.

[00606] Two distinct curves represent the drain current behavior under clockwise (CW) and counterclockwise (MW) polarization of the FeFET. The blue curve (CW) starts at approximately $10^{-11} \text{A}/\mu\text{m}$ at -1V and exhibits a steep increase around -1 V, reaching just

above 10^{-5} A/ μm at 1V. This demonstrates the rapid increase in drain current exhibited by the FeFET under forward bias in the clockwise polarization state.

[00607] Conversely, the red curve (MW) starts at approximately 10^{-11} A/ μm at -1V and increases more gradually as it approaches 0V. At around 1V, it then follows closely with the blue curve past 1V. This demonstrates comparable drain current behavior under reverse bias conditions regardless of the polarization state.

[00608] Notably, the separation between the red and blue curves spans several orders of magnitude in the negative voltage range near -1V. This substantial difference in off-state current highlights the non-volatile memory effect achievable with the FeFET depending on its polarization direction. This large memory window is explicitly called out in the green box labeled “Large Memory Window” at the top left.

[00609] Additional key details provided include the FeFET device dimensions, with a width/length ratio of $1\mu\text{m}/50\text{nm}$ specified. The drain voltage is also fixed at 0.05V. Specific points along the curves are annotated, such as “MW @ $5\text{e-}7$ A/ μm = 1V” on the red MW curve denoting the 1V memory window at 5×10^{-7} A/ μm drain current. Another point marked is “CW @ -0.5V = 1×10^6 ” on the blue CW curve, highlighting the clockwise current value of 1×10^{-6} A/ μm at -0.5V gate voltage.

[00610] In summary, Fig. 20 comprehensively depicts the bidirectional transfer characteristics of the FeFET device, highlighting the large memory window achievable through polarization switching and providing detailed voltage, current, and dimensional specifications to fully convey the measurement conditions and transistor performance. The paired curves effectively compare the clockwise and counterclockwise operation modes over the full gate voltage range.

[00611] Various alternatives and modifications can be devised by those skilled in the art without departing from the disclosure. Accordingly, the present disclosure is intended to embrace all such alternatives, modifications, and variances. Additionally, while several embodiments of the present disclosure have been shown in the drawings and/or discussed herein, it is not intended that the disclosure be limited thereto, as it is intended that the disclosure be as broad in scope as the art will allow and that the specification be read likewise. Therefore, the above description should not be construed as limiting, but merely as exemplifications of particular embodiments. And those skilled in the art will envision other modifications within the scope and spirit of the claims appended hereto. Other elements, steps, methods, and techniques that are insubstantially different from those described above and/or in the appended claims are also intended to be within the scope of the disclosure.

[00612] The embodiments shown in the drawings are presented only to demonstrate certain examples of the disclosure. And the drawings described are only illustrative and are non-limiting. In the drawings, for illustrative purposes, the size of some of the elements may be exaggerated and not drawn to a particular scale. Additionally, elements shown within the drawings that have the same numbers may be identical elements or may be similar elements, depending on the context.

[00613] Where the term "comprising" is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun, e.g., "a," "an," or "the," this includes a plural of that noun unless something otherwise is specifically stated. Hence, the term "comprising" should not be interpreted as being restricted to the items listed thereafter; it does not exclude other elements or steps, and so the scope of the expression "a device comprising items A and B" should not be limited to devices consisting only of components A and B. This expression signifies that, with respect to the present disclosure, the only relevant components of the device are A and B.

[00614] Furthermore, the terms "first," "second," "third," and the like, whether used in the description or in the claims, are provided for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances (unless clearly disclosed otherwise) and that the embodiments of the disclosure described herein are capable of operation in other sequences and/or arrangements than are described or illustrated herein.

[00615] Each of the characteristics and examples described herein, and combination thereof, may be said to be encompassed by the present disclosure. The present disclosure is thus drawn to the following non-limiting numbered aspects:

[00616] 1. An integrated circuit, comprising: a first transistor comprising: a channel layer formed using a semiconductor material; and a ferroelectric rigidly coupled to the channel layer; a source terminal fixed to the channel layer; a drain terminal fixed to the channel layer; and a gate terminal fixed to the ferroelectric layer.

[00617] 2. An integrated circuit as aspected or disclosed herein wherein the channel layer is formed from a polycrystalline silicon.

[00618] 3. An integrated circuit as aspected or disclosed herein wherein the channel layer is formed from an Amorphous Oxide Semiconductor.

[00619] 4. The integrated circuit according to aspect 3 wherein the Amorphous Oxide Semiconductor includes at least one of Indium Oxide, Indium Gallium Zinc Oxide, Zinc Tin Oxide, Indium Zinc Oxide, Gallium Zinc Oxide, Aluminum Zinc Oxide, Cadmium Oxide,

Hafnium Indium Zinc Oxide, Tin Oxide, stannous Tin Oxide, stannic Tin Oxide, Indium-Tin-Zinc Oxide, Indium-Tungsten Oxide, Indium-Gallium-Zinc-Tin Oxide, Indium-Gallium-Zinc-Ozynitride, Aluminum-Indium-Gallium-Zinc Oxide, and Zinc-Indium Oxide.

[00620] 5. The integrated circuit as in aspect 3 or 4, wherein the Amorphous Oxide Semiconductor is doped with at least one of Gallium (Ga), Indium (In), Zinc (Zn), Tin (Sn), Hafnium (Hf), Silicon (Si), Aluminum (Al), Magnesium (Mg), Calcium (Ca), Strontium (Sr), Barium (Ba), Titanium (Ti), Zirconium (Zr), Molybdenum (Mo), Tantalum (Ta), Niobium (Nb), Chromium (Cr), Iron (Fe), Cobalt (Co), Nickel (Ni), Copper (Cu), Silver (Ag), Gold (Au), Cerium (Ce), Lanthanum (La), Neodymium (Nd), Samarium (Sm), Europium (Eu), Gadolinium (Gd), Terbium (Tb), Dysprosium (Dy), Holmium (Ho), Erbium (Er), Thulium (Tm), Ytterbium (Yb), Lutetium (Lu), Yttrium (Y), Scandium (Sc), Bismuth (Bi), Lead (Pb), Thallium (Tl), Antimony (Sb), Arsenic (As), Phosphorus (P), Boron (B), Nitrogen (N), Fluorine (F), Chlorine (Cl), Bromine (Br), and Iodine (I).

[00621] 6. An integrated circuit as aspected or disclosed herein wherein the channel layer is formed from two dimensional materials to include transition metal dichalcogenides.

[00622] 7. The integrated circuit as in aspect 6, wherein the transition metal dichalcogenides is monovalent.

[00623] 8. The integrated circuit as in aspect 6, wherein the transition metal dichalcogenides is divalent.

[00624] 9. The integrated circuit as in aspect 6, wherein a chalcogenide element in the transition metal dichalcogenides is sulfur.

[00625] 10. The integrated circuit as in aspect 6, wherein a chalcogenide element in the transition metal dichalcogenides is selenium.

[00626] 11. The integrated circuit as in aspect 6, wherein a chalcogenide element in the transition metal dichalcogenides is tellurium.

[00627] 12. An integrated circuit as aspected or disclosed herein where the channel layer is formed from Indium Tungsten Oxide ("IWO").

[00628] 13. An integrated circuit as aspected or disclosed herein wherein the channel layer is formed from an indium galium zinc oxide ("IGZO").

[00629] 14. The integrated circuit as in any of the preceding aspects, wherein the channel layer is a thin film.

[00630] 15. The integrated circuit as in any of the preceding aspects, wherein the hafnium zirconium oxide is $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$.

- [00631] 16. The integrated circuit as in any of the preceding aspects, wherein the integrated circuit is disposed on a back-end-of-the-line portion of a semiconductor device fabrication flow.
- [00632] 17. The integrated circuit as in any of the preceding aspects, wherein the ferroelectric layer is made of transition metal oxides, a perovskite, or a two-dimensional material.
- [00633] 18. The integrated circuit as in any of the preceding aspects, wherein a metal layer is disposed between the channel layer and the ferroelectric layer.
- [00634] 19. The integrated circuit according to aspect 18, further comprising an insulator layer disposed between the metal layer and the channel layer.
- [00635] 20. The integrated circuit according to aspect 1, further comprising a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer.
- [00636] 21. The integrated circuit according to aspect 1, further comprising: a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer; and an insulation layer disposed on the channel layer, wherein the ferroelectric layer is also disposed on the insulation layer.
- [00637] 22. The integrated circuit according to aspect 1, further comprising a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer.
- [00638] 23. The integrated circuit as in any of the preceding aspects, wherein the channel layer is less than 30 nm in thickness.
- [00639] 24. The integrated circuit as in any of the preceding aspects, wherein the channel layer is between 1 to 30 nm in thickness.
- [00640] 25. The integrated circuit as in any of the preceding aspects, wherein the channel layer is formed using physical vapor deposition or chemical vapor deposition.
- [00641] 26. The integrated circuit as in any of the preceding aspects, wherein the channel layer is formed using atomic layer deposition.
- [00642] 27. The integrated circuit as in aspect 25 or 26, wherein the channel layer is formed by adding a dopant comprising at least one of tungsten, Ga, and Zn.
- [00643] 28. The integrated circuit as in any of the preceding aspects, wherein the ferroelectric layer is formed using atomic layer deposition.
- [00644] 29. The integrated circuit as in any of the preceding aspects, wherein the ferroelectric layer is formed using vapor deposition.

- [00645] 30. The integrated circuit as in aspect 28 or 29, wherein the ferroelectric layer is formed by adding a dopant comprising at least one of Lanthanum, Niobium, Manganese, Zirconium, Tin, Strontium, Calcium, Yttrium, Magnesium.
- [00646] 31. The integrated circuit as in any of the preceding aspects, wherein the channel layer is configured to have a carrier concentration of 10^{17} to 10^{20} per centimeter-cubed.
- [00647] 32. The integrated circuit as in any of the preceding aspects, wherein the channel layer comprises a two-dimensional material.
- [00648] 33. The integrated circuit according to aspect 32, wherein the two-dimensional material maintains an electron mobility of at least 0.1 cm-squared per Volt-second when the channel layer is less than 30nm in thickness.
- [00649] 34. The integrated circuit according to aspect 33, wherein the channel layer comprises fewer than 5 monolayers of the two-dimensional material.
- [00650] 35. The integrated circuit as in any of the preceding aspects, wherein the ferroelectric layer is Hafnium Zirconium Oxide.
- [00651] 36. The integrated circuit as in any of the preceding aspects, wherein a coercive voltage of the ferroelectric layer is between -3 Volts to 3 Volts.
- [00652] 37. The integrated circuit as in any of the preceding aspects, wherein an off-state current of the ferroelectric layer is less than 10^{-7} amps per centimeter cubed.
- [00653] 38. The integrated circuit as in any of the preceding aspects, wherein an on-state current of the ferroelectric layer is greater than 10^{-7} amps per centimeter cubed.
- [00654] 39. The integrated circuit as in any of the preceding aspects, wherein a crystallization anneal temperature of the ferroelectric layer is less than or equal to 500 degrees Celsius.
- [00655] 40. The integrated circuit as in any of the preceding aspects, wherein a remanent polarization of the ferroelectric layer is greater than 10 microcoulombs per square centimeter.
- [00656] 41. The integrated circuit as in any of the preceding aspects, wherein an anneal temperature of the channel layer is less than 450 Celsius.
- [00657] 42. The integrated circuit as in any of the preceding aspects, wherein a channel mobility of the channel layer is less than 100 centimeters squared per Volt-second.
- [00658] 43. The integrated circuit as in any of the preceding aspects, wherein a subthreshold swing of the channel layer is less than 0.3 volts per decade.

- [00659] 44. The integrated circuit as in any of the preceding aspects, wherein the channel layer is configured to have an off-state current of less than 10^{-7} amps per micrometer.
- [00660] 45. The integrated circuit as in any of the preceding aspects, wherein the channel layer is configured to have a channel bandgap of greater than 2.5 electron-volts.
- [00661] 46. The integrated circuit as in any of the preceding aspects, wherein the channel layer is configured to have a post-anneal threshold voltage between -1.5 Volts to 1.5 Volts.
- [00662] 47. The integrated circuit as in any of the preceding aspects, wherein the first transistor has a width of less than 200nm and a length of 50 nano meters.
- [00663] 48. The integrated circuit as in any of the preceding aspects, wherein the first transistor has a device area of less than 30 times the square of the feature size. Unclear
- [00664] 49. The integrated circuit as in any of the preceding aspects, wherein the first transistor has a LVT (low-voltage threshold) level greater than $-2.5V$.
- [00665] 50. The integrated circuit as in any of the preceding aspects, wherein the first transistor has a HVT (high-voltage threshold) level greater than $-2V$.
- [00666] 51. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a read voltage is between 0V to 1V.
- [00667] 52. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a read energy is less than 10 picojoules.
- [00668] 53. The integrated circuit as in any of the preceding aspects wherein a memory cell having the first transistor has a read pulse width (PW) less than 20 nanoseconds (ns).
- [00669] 54. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a read endurance is greater than or equal to 10^9 cycles.
- [00670] 55. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a read disturb tolerance is greater than 10^9 cycles.
- [00671] 56. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a read after write latency is less than or equal to 10 microseconds.
- [00672] 57. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a write voltage is less than or equal to 3.0 Volts (V).

- [00673] 58. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a write speed is less than or equal to 10 microseconds.
- [00674] 59. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a write energy is less than 10 picojoules.
- [00675] 60. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a write endurance is greater than 10^8 cycles.
- [00676] 61. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a off-state resistance to on-state resistance ratio (R_{off}/R_{on}) is about 10^3 or greater than 10^2 .
- [00677] 62. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has an on-state current to off-state current ratio (I_{on}/I_{off}) at V_{read} from DC measurement is greater than 10^2 .
- [00678] 63. The integrated circuit as in one of aspects 51-62, wherein the memory cell includes the first transistor and a second transistor, wherein the second transistor is the same configuration as the first transistor, wherein the first and second transistors form a bit state.
- [00679] 64. The integrated circuit as in one of aspects 51-62, the first transistor is configured to have 3 or more states each state corresponding to a stored value of the memory cell.
- [00680] 65. The integrated circuit as in any of the preceding aspects, wherein the first transistor has an on-state current to off-state current ratio (I_{on}/I_{off}) at V_{read} from pulse measurement is greater than 10^2 .
- [00681] 66. The integrated circuit as in any of the preceding aspects, wherein the first transistor has an off-state current (I_{off}) is less than 10^{-14} amps per micrometer.
- [00682] 67. The integrated circuit as in any of the preceding aspects, wherein a memory cell having the first transistor has a reliability endurance is greater than or equal to 10^{11} cycles.
- [00683] 68. The integrated circuit as in any of the preceding aspects wherein a memory cell having the first transistor has a retention is at least 1 minute at room temperature of 25C.
- [00684] 69. The integrated circuit as in any of the preceding aspects, wherein another two-dimensional material is incorporated into the channel layer to enhance the ION current in the first transistor.

- [00685] 70. The integrated circuit as in any of the preceding aspects, wherein the channel layer is configured to maintained high mobility despite the presence of the ferroelectric layer.
- [00686] 71. The integrated circuit as in any of the preceding aspects, wherein the ferroelectric layer and the channel layer are configured such that the ferroelectric layer does not significantly impede the electron mobility within the channel layer.
- [00687] 72. The integrated circuit as in any of the preceding aspects, wherein the channel layer is directly in contact with the ferroelectric layer without an interfacial layer in between.
- [00688] 73. The integrated circuit according to aspect 72, wherein the direct contact between the channel layer and the ferroelectric layer is configured to minimize voltage drops across the interface thereby enabling low voltage operation of the first transistor.
- [00689] 74. The integrated circuit according to any of the preceding aspect, wherein the first transistor is characterized by low voltage operation and low power consumption due to the absence of an interfacial layer between the channel layer and the ferroelectric layer.
- [00690] 75. The integrated circuit according to any of the preceding aspect, wherein the first transistor is characterized by low voltage operation and low power consumption due to the absence of an interfacial layer between the ferroelectric layer and the gate layer.
- [00691] 76. The integrated circuit as in aspect 74 or 75, wherein a reduced voltage operation contributes to a decrease in overall power consumption of the integrated circuit.
- [00692] 77. The integrated circuit as in aspect 74 or 75, wherein the first transistor is configured for improved switching characteristics including faster turn-on and turn-off times due to the absence of the interfacial layer.
- [00693] 78. The integrated circuit as in aspect 74 or 75, wherein the ferroelectric layer and the channel larger are configured for reduced parasitic capacitance at the channel layer and ferroelectric layer interface due to the absence of the interfacial layer.
- [00694] 79. The integrated circuit as in any of the preceding aspects, wherein ferroelectric layer is configured for a substantially uniform electric field distribution across the ferroelectric layer.
- [00695] 80. The integrated circuit as in one of aspects 1- 8, wherein ferroelectric layer is configured for a gradient in an electric field distribution across the ferroelectric layer.
- [00696] 81. The integrated circuit as in any of the preceding aspects, further comprising a microvault formed from a plurality of transistors including the first transistor.

- [00697] 82. The integrated circuit according to aspect 81, wherein the micro-vault is organized into columns comprising 3 terminal bit-cells.
- [00698] 83. The integrated circuit according to aspect 81, wherein the microvault is formed via a column in one of a 3D-NOR, a 3D-AND, a 3D-NAND, or a 3D-NAND-PG configuration.
- [00699] 84. The integrated circuit as in any of the preceding aspects, wherein the channel material comprises Indium Gallium Zinc Oxide (“IGZO”).
- [00700] 85. The integrated circuit as in any of the preceding aspects, wherein the source terminal comprises at least one of Tungsten, Titanium Nitride, Nickel, and Molybdenum.
- [00701] 86. The integrated circuit as in any of the preceding aspects, wherein the drain terminal comprises at least one of Tungsten, Titanium Nitride, Nickel, and Molybdenum.
- [00702] 87. The integrated circuit as in any of the preceding aspects, wherein the gate terminal comprises at least one of Tungsten, Titanium Nitride, Nickel, and Molybdenum.
- [00703] 88. The integrated circuit as in any of the preceding aspects, further comprising a memory formed from a plurality of the first transistors, the memory formed as a 3D vertical device architecture selected from a NAND and a NOR configurations.
- [00704] 89. The integrated circuit as in any of the preceding aspects, comprising a microvault column comprising a plurality of transistors, each of the plurality of transistors is according to the first transistor.
- [00705] 90. The integrated circuit according to aspect 89, wherein the microvault column is configured as a 3D-NOR.
- [00706] 91. The integrated circuit according to aspect 89, wherein the microvault column is configured as a 3D-AND.
- [00707] 92. The integrated circuit according to aspect 89, wherein the microvault column is configured as a 3D-NAND.
- [00708] 93. The integrated circuit according to aspect 89, wherein the microvault column is configured as a 3D-NAND with pass gate.
- [00709] 94. The integrated circuit according to aspect 89, wherein the microvault column is configured as a 3D-NOR with an independent read enable and an independent write enable.
- [00710] 95. The integrated circuit according to aspect 89, wherein the microvault column is configured as a 3D-AND with an independent read/write enable.

[00711] 96. The integrated circuit as in one of aspects 1-95, wherein the ferroelectric layer is formed from at least one of Perovskites, Lead Zirconate Titanate (PZT), Barium Titanate (BaTiO_3), Strontium Titanate (SrTiO_3), Bismuth Ferrite (BiFeO_3), Potassium Niobate (KNbO_3), Lithium Niobate (LiNbO_3), Lithium Tantalate (LiTaO_3), Sodium Bismuth Titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Bismuth Zinc Niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$), Bismuth Lanthanum Titanate (BiLaTiO_3), Bismuth Nickel Titanate (BiNiTiO_3), Lead Magnesium Niobate-Lead Titanate (PMN-PT), Lead Lanthanum Zirconate Titanate (PLZT), Neodymium-doped Bismuth Titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$), Hafnium-based Oxides, Hafnium Oxide (HfO_2), Doped Hafnium Oxide, Zirconium-doped Hafnium Oxide (HfZrO_2), Tungsten Bronze Structure Materials, Barium Strontium Niobate (BSN), Lead Barium Niobate (PBN), Potassium Tantalate Niobate (KTN), Bismuth Layer-Structured Ferroelectrics, Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Strontium Bismuth Tantalate (SBT), Calcium Bismuth Niobate (CBN), Organic Ferroelectrics, Polyvinylidene Fluoride (PVDF), TrFE (Trifluoroethylene), P(VDF-TrFE) Copolymers, Aurivillius Phase Oxides, Rare Earth Manganites, YMnO_3 , Lanthanum-modified Lead Zirconate Titanate (PLZT), Nickel Manganese Oxide (NiMnO_3), Relaxor Ferroelectrics, Lead Magnesium Niobate (PMN), Lead Scandium Tantalate (PST), Lead Indium Niobate (PIN), Multiferroic Materials, Terbium Manganite (TbMnO_3), Europium Titanium Oxide (EuTiO_3), SbSI (Antimony Sulfoiodide), GeTe (Germanium Telluride), SnTe (Tin Telluride), Thin-Film Ferroelectrics, PZT Thin Films, SBT Thin Films, HfO_2 -based Thin Films, Layered Superlattices, and $\text{PbTiO}_3/\text{SrTiO}_3$.

[00712] 97. An integrated circuit, comprising: a first vertical structure, comprising: a dielectric column; a channel column disposed around the dielectric column; and a ferroelectric column disposed around the channel along a length of the channel column; and a plurality of horizontal gate-electrode layers, each of the plurality of horizontal gate-electrode layers disposed a predetermined distance between each other, each of the plurality of horizontal gate-electrode layers disposed adjacent to the ferroelectric column along the length of the ferroelectric column.

[00713] 98. The integrated circuit according to aspect 97, wherein the dielectric column is substantially cylindrical.

[00714] 99. The integrated circuit according to aspect 98, wherein the dielectric column has a first diameter on a first end and a second diameter on the second end.

[00715] 100. The integrated circuit according to aspect 99, wherein the first diameter and the second diameter are the same.

- [00716] 101. The integrated circuit according to aspect 99, wherein the first diameter is larger than the second diameter.
- [00717] 102. The integrated circuit as in one of aspects 97-101, wherein the dielectric column is solid.
- [00718] 103. The integrated circuit as in one of aspects 97-101, wherein the dielectric column is hollow.
- [00719] 104. The integrated circuit according to aspect 97, wherein the channel column is substantially cylindrical.
- [00720] 105. The integrated circuit according to aspect 104, wherein the channel column has a first diameter on a first end and a second diameter on the second end.
- [00721] 106. The integrated circuit according to aspect 105, wherein the first diameter and the second diameter are the same.
- [00722] 107. The integrated circuit according to aspect 105, wherein the first diameter is larger than the second diameter.
- [00723] 108. The integrated circuit according to aspect 96, wherein the ferroelectric column is substantially cylindrical.
- [00724] 109. The integrated circuit according to aspect 108, wherein the ferroelectric column has a first diameter on a first end and a second diameter on the second end.
- [00725] 110. The integrated circuit according to aspect 109, wherein the first diameter and the second diameter are the same.
- [00726] 111. The integrated circuit according to aspect 109, wherein the first diameter is larger than the second diameter.
- [00727] 112. The integrated circuit according to aspect 96, further comprising a dielectric end column disposed around an end of the channel column and adjacent to an end of the length of the channel column and adjacent to the ferroelectric column.
- [00728] 113. The integrated circuit according to aspect 112, further comprising a drain select layer disposed in parallel with the plurality of horizontal gate-electrode layers and adjacent to the dielectric end column.
- [00729] 114. The integrated circuit as in aspect 112 or 113, further comprising a second dielectric end column disposed around another end of the channel column and adjacent to another end of the length of the channel column and adjacent to the ferroelectric column.
- [00730] 115. The integrated circuit according to aspect 114, further comprising a source select layer disposed in parallel with the plurality of horizontal gate-electrode layers and adjacent to the second dielectric end column.

[00731] 116. The integrated circuit according to any one of aspects 96-115, further comprising a second vertical structure.

[00732] 117. The integrated circuit according to aspect 116, wherein the second vertical structure is formed to be substantially identical to the first vertical structure, but disposed adjacent the first vertical column at a predetermined horizontal distance.

[00733] 118. The integrated circuit as in aspect 116 or 117, wherein the first and second vertical structures are configured to form a single-port 3D NAND structure.

[00734] 119. The integrated circuit as in one of aspects 97-118, wherein the plurality of horizontal gate-electrode layers is formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu, TiW, and Conducting Polymers.

[00735] 120. The integrated circuit as in one of aspects 97-119, wherein the ferroelectric column is formed from at least one of Perovskites, Lead Zirconate Titanate (PZT), Barium Titanate (BaTiO_3), Strontium Titanate (SrTiO_3), Bismuth Ferrite (BiFeO_3), Potassium Niobate (KNbO_3), Lithium Niobate (LiNbO_3), Lithium Tantalate (LiTaO_3), Sodium Bismuth Titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Bismuth Zinc Niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$), Bismuth Lanthanum Titanate (BiLaTiO_3), Bismuth Nickel Titanate (BiNiTiO_3), Lead Magnesium Niobate-Lead Titanate (PMN-PT), Lead Lanthanum Zirconate Titanate (PLZT), Neodymium-doped Bismuth Titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$), Hafnium-based Oxides, Hafnium Oxide (HfO_2), Doped Hafnium Oxide, Zirconium-doped Hafnium Oxide (HfZrO_2), Tungsten Bronze Structure Materials, Barium Strontium Niobate (BSN), Lead Barium Niobate (PBN), Potassium Tantalate Niobate (KTN), Bismuth Layer-Structured Ferroelectrics, Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Strontium Bismuth Tantalate (SBT), Calcium Bismuth Niobate (CBN), Organic Ferroelectrics, Polyvinylidene Fluoride (PVDF), TrFE (Trifluoroethylene), P(VDF-TrFE) Copolymers, Aurivillius Phase Oxides, Rare Earth Manganites, YMnO_3 , Lanthanum-modified Lead Zirconate Titanate (PLZT), Nickel Manganese Oxide (NiMnO_3), Relaxor Ferroelectrics, Lead Magnesium Niobate (PMN), Lead Scandium Tantalate (PST), Lead Indium Niobate (PIN), Multiferroic Materials, Terbium Manganite (TbMnO_3), Europium Titanium Oxide (EuTiO_3), SbSI (Antimony Sulfoiodide), GeTe (Germanium Telluride), SnTe (Tin Telluride), Thin-Film Ferroelectrics, PZT Thin Films, SBT Thin Films, HfO_2 -based Thin Films, Layered Superlattices, and $\text{PbTiO}_3/\text{SrTiO}_3$.

[00736] 121. The integrated circuit as in one of aspects 97-120, wherein the channel column is formed from at least one of Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), Zinc Tin Oxide (ZTO), Aluminum Zinc Oxide (AZO), Indium Tungsten Oxide (IWO), Gallium Zinc Oxide (GZO), Hafnium Indium Oxide (HIO), and Cadmium Oxide (CdO), Polysilicon, Polygermanium Cadmium Selenide (CdSe), Copper Indium Gallium Selenide (CIGS), Crystalline Silicon (c-Silicon), Crystalline Germanium (c-Germanium), Gallium Arsenide (GaAs), Indium Phosphide (InP), Indium Antimonide (InSb), Silicon Carbide (SiC), Gallium Nitride (GaN), Zinc Oxide (ZnO), Pentacene, P3HT (Poly(3-hexylthiophene)), Polythiophene, Polyphenylene vinylene (PPV), Graphene, Carbon Nanotubes (CNTs), Methylammonium Lead Halides ($\text{CH}_3\text{NH}_3\text{PbX}_3$, $\text{X} = \text{Cl, Br, I}$), Cesium Lead Halide (CsPbX_3 , $\text{X} = \text{Cl, Br, I}$), Lead Sulfide (PbS), Lead Selenide (PbSe), Cadmium Selenide (CdSe), Indium Arsenide (InAs), Skutterudites, Ruddlesden-Popper phases, Clathrates, Perovskite Oxides, and Magnetic Semiconductors.

[00737] 122. The integrated circuit as in one of aspects 97-121, wherein the dielectric column is formed from at least one of Hafnium Oxide (HfO_2), Zirconium Oxide (ZrO_2), Aluminum Oxide (Al_2O_3), Silicon Dioxide (SiO_2), Titanium Dioxide (TiO_2), Tantalum Oxide (Ta_2O_5), Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3), Silicon Nitride (Si_3N_4), Aluminum Nitride (AlN), Silicon Carbide (SiC), Strontium Titanate (SrTiO_3), Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), Bismuth Ferrite (BiFeO_3), Magnesium Oxide (MgO), Cerium Oxide (CeO_2), Nickel Oxide (NiO), Cobalt Oxide (CoO), Copper Oxide (CuO), Manganese Oxide (MnO), Zinc Oxide (ZnO), Gadolinium Oxide (Gd_2O_3), Dysprosium Oxide (Dy_2O_3), Samarium Oxide (Sm_2O_3), Europium Oxide (Eu_2O_3), Terbium Oxide (Tb_4O_7), Vanadium Oxide (V_2O_5), Niobium Oxide (Nb_2O_5), Chromium Oxide (Cr_2O_3), Iron Oxide (Fe_2O_3), Molybdenum Oxide (MoO_3), Tungsten Oxide (WO_3), Ruthenium Oxide (RuO_2), Rhodium Oxide (Rh_2O_3), Palladium Oxide (PdO), Silver Oxide (Ag_2O), Cadmium Oxide (CdO), Tin Oxide (SnO_2), Antimony Oxide (Sb_2O_3), Tellurium Oxide (TeO_2), Iridium Oxide (IrO_2), Platinum Oxide (PtO_2), Gold Oxide (Au_2O_3), Beryllium Oxide (BeO), Magnesium Aluminate (MgAl_2O_4), Zinc Selenide (ZnSe), Zinc Telluride (ZnTe), Cadmium Sulfide (CdS), Cadmium Selenide (CdSe), Cadmium Telluride (CdTe), Silicon Germanium Oxide (SiGeO_x), Bismuth Oxide (Bi_2O_3), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Perovskite Oxides, Layered Oxides, and Complex Transition Metal Oxides.

[00738] 123. The integrated circuit as in one of aspects 97-122, wherein one of plurality of horizontal gate-electrode layers and the first vertical structure are configured to

form a plurality of transistors including the first transistor according to any one of aspects 1-96.

[00739] 124. An integrated circuit, comprising: a first vertical structure, comprising: a pass-gate electrode column; a dielectric column disposed around the pass-gate electrode column; a channel column disposed around the dielectric column; and a ferroelectric column disposed around the channel along a length of the channel column; and a plurality of horizontal gate-electrode layers, each of the plurality of horizontal gate-electrode layers disposed a predetermined distance between each other, each of the plurality of horizontal gate-electrode layers disposed adjacent to the ferroelectric column along the length of the ferroelectric column.

[00740] 125. The integrated circuit according to aspect 124, wherein the pass-gate electrode column is substantially cylindrical.

[00741] 126. The integrated circuit according to aspect 125, wherein the pass-gate electrode column has a first diameter on a first end and a second diameter on the second end.

[00742] 127. The integrated circuit according to aspect 126, wherein the first diameter and the second diameter are the same.

[00743] 128. The integrated circuit according to aspect 126, wherein the first diameter is larger than the second diameter.

[00744] 129. The integrated circuit as in one of aspects 124 to 128, wherein the pass-gate electrode column is solid.

[00745] 130. The integrated circuit as in one of aspects 124 to 128, wherein the pass-gate electrode column is hollow.

[00746] 131. The integrated circuit according to aspect 124, wherein the dielectric column is substantially cylindrical.

[00747] 132. The integrated circuit according to aspect 131, wherein the dielectric column has a first diameter on a first end and a second diameter on the second end.

[00748] 133. The integrated circuit according to aspect 132, wherein the first diameter and the second diameter are the same.

[00749] 134. The integrated circuit according to aspect 132, wherein the first diameter is larger than the second diameter.

[00750] 135. The integrated circuit according to aspect 124, wherein the channel column is substantially cylindrical.

[00751] 136. The integrated circuit according to aspect 135, wherein the channel column has a first diameter on a first end and a second diameter on the second end.

- [00752] 137. The integrated circuit according to aspect 136, wherein the first diameter and the second diameter are the same.
- [00753] 138. The integrated circuit according to aspect 136, wherein the first diameter is larger than the second diameter.
- [00754] 139. The integrated circuit according to aspect 124, wherein the ferroelectric column is substantially cylindrical.
- [00755] 140. The integrated circuit according to aspect 139, wherein the ferroelectric column has a first diameter on a first end and a second diameter on the second end.
- [00756] 141. The integrated circuit according to aspect 140, wherein the first diameter and the second diameter are the same.
- [00757] 142. The integrated circuit according to aspect 140, wherein the first diameter is larger than the second diameter.
- [00758] 143. The integrated circuit according to aspect 124, further comprising a dielectric end column disposed around an end of the channel column and adjacent to an end of the length of the channel column and adjacent to the ferroelectric column.
- [00759] 144. The integrated circuit according to aspect 143, further comprising a drain select layer disposed in parallel with the plurality of horizontal gate-electrode layers and adjacent to the dielectric end column.
- [00760] 145. The integrated circuit as in aspect 143 or 144, further comprising a second dielectric end column disposed around another end of the channel column and adjacent to another end of the length of the channel column and adjacent to the ferroelectric column.
- [00761] 146. The integrated circuit according to aspect 145, further comprising a source select layer disposed in parallel with the plurality of horizontal gate-electrode layers and adjacent to the second dielectric end column.
- [00762] 147. The integrated circuit as in one of aspects 143-146, further comprising dielectric horizontal layer disposed within the channel column and adjacent to an end of the pass-gate electrode column.
- [00763] 148. The integrated circuit according to any one of aspects 124-147, further comprising a second vertical structure.
- [00764] 149. The integrated circuit according to aspect 148, wherein the second vertical structure is formed to be substantially identical to the first vertical structure, but disposed adjacent the first vertical column at a predetermined horizontal distance.
- [00765] 150. The integrated circuit as in aspect 148 or 149, wherein the first and second vertical structures are configured to form a dual-port 3D NAND structure.

[00766] 151. The integrated circuit as in one of aspects 124-150, wherein the plurality of horizontal gate-electrode layers is formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu , TiW , and Conducting Polymers.

[00767] 152. The integrated circuit as in one of aspects 124-151, wherein the pass-gate electrode column is formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu , TiW , and Conducting Polymers.

[00768] 153. The integrated circuit as in one of aspects 124-152, wherein the ferroelectric column is formed from at least one of Perovskites, Lead Zirconate Titanate (PZT), Barium Titanate (BaTiO_3), Strontium Titanate (SrTiO_3), Bismuth Ferrite (BiFeO_3), Potassium Niobate (KNbO_3), Lithium Niobate (LiNbO_3), Lithium Tantalate (LiTaO_3), Sodium Bismuth Titanate ($\text{Na}_0.5\text{Bi}_0.5\text{TiO}_3$), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Bismuth Zinc Niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$), Bismuth Lanthanum Titanate (BiLaTiO_3), Bismuth Nickel Titanate (BiNiTiO_3), Lead Magnesium Niobate-Lead Titanate (PMN-PT), Lead Lanthanum Zirconate Titanate (PLZT), Neodymium-doped Bismuth Titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$), Hafnium-based Oxides, Hafnium Oxide (HfO_2), Doped Hafnium Oxide, Zirconium-doped Hafnium Oxide (HfZrO_2), Tungsten Bronze Structure Materials, Barium Strontium Niobate (BSN), Lead Barium Niobate (PBN), Potassium Tantalate Niobate (KTN), Bismuth Layer-Structured Ferroelectrics, Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Strontium Bismuth Tantalate (SBT), Calcium Bismuth Niobate (CBN), Organic Ferroelectrics, Polyvinylidene Fluoride (PVDF), TrFE (Trifluoroethylene), P(VDF-TrFE) Copolymers, Aurivillius Phase Oxides, Rare Earth Manganites, YMnO_3 , Lanthanum-modified Lead Zirconate Titanate (PLZT), Nickel Manganese Oxide (NiMnO_3), Relaxor Ferroelectrics, Lead Magnesium Niobate (PMN), Lead Scandium Tantalate (PST), Lead Indium Niobate (PIN), Multiferroic Materials, Terbium Manganite (TbMnO_3), Europium Titanium Oxide (EuTiO_3), SbSI (Antimony Sulfoiodide), GeTe (Germanium Telluride), SnTe (Tin Telluride), Thin-Film Ferroelectrics, PZT Thin Films, SBT Thin Films, HfO_2 -based Thin Films, Layered Superlattices, and $\text{PbTiO}_3/\text{SrTiO}_3$.

[00769] 154. The integrated circuit as in one of aspects 124-153, wherein the channel column is formed from at least one of Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), Zinc Tin Oxide (ZTO), Aluminum Zinc Oxide (AZO), Indium Tungsten Oxide (IWO), Gallium Zinc Oxide (GZO), Hafnium Indium Oxide (HfIO), and Cadmium Oxide (CdO), Polysilicon, Polygermanium Cadmium Selenide (CdSe), Copper Indium Gallium Selenide (CIGS), Crystalline Silicon (c-Silicon), Crystalline Germanium (c-Germanium), Gallium Arsenide (GaAs), Indium Phosphide (InP), Indium Antimonide (InSb), Silicon Carbide (SiC), Gallium Nitride (GaN), Zinc Oxide (ZnO), Pentacene, P3HT (Poly(3-hexylthiophene)), Polythiophene, Polyphenylene vinylene (PPV), Graphene, Carbon Nanotubes (CNTs), Methylammonium Lead Halides ($\text{CH}_3\text{NH}_3\text{PbX}_3$, $\text{X} = \text{Cl, Br, I}$), Cesium Lead Halide (CsPbX_3 , $\text{X} = \text{Cl, Br, I}$), Lead Sulfide (PbS), Lead Selenide (PbSe), Cadmium Selenide (CdSe), Indium Arsenide (InAs), Skutterudites, Ruddlesden-Popper phases, Clathrates, Perovskite Oxides, and Magnetic Semiconductors.

[00770] 155. The integrated circuit as in one of aspects 124-154, wherein the dielectric column is formed from at least one of Hafnium Oxide (HfO_2), Zirconium Oxide (ZrO_2), Aluminum Oxide (Al_2O_3), Silicon Dioxide (SiO_2), Titanium Dioxide (TiO_2), Tantalum Oxide (Ta_2O_5), Lanthanum Oxide (La_2O_3), Yttrium Oxide (Y_2O_3), Silicon Nitride (Si_3N_4), Aluminum Nitride (AlN), Silicon Carbide (SiC), Strontium Titanate (SrTiO_3), Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), Bismuth Ferrite (BiFeO_3), Magnesium Oxide (MgO), Cerium Oxide (CeO_2), Nickel Oxide (NiO), Cobalt Oxide (CoO), Copper Oxide (CuO), Manganese Oxide (MnO), Zinc Oxide (ZnO), Gadolinium Oxide (Gd_2O_3), Dysprosium Oxide (Dy_2O_3), Samarium Oxide (Sm_2O_3), Europium Oxide (Eu_2O_3), Terbium Oxide (Tb_4O_7), Vanadium Oxide (V_2O_5), Niobium Oxide (Nb_2O_5), Chromium Oxide (Cr_2O_3), Iron Oxide (Fe_2O_3), Molybdenum Oxide (MoO_3), Tungsten Oxide (WO_3), Ruthenium Oxide (RuO_2), Rhodium Oxide (Rh_2O_3), Palladium Oxide (PdO), Silver Oxide (Ag_2O), Cadmium Oxide (CdO), Tin Oxide (SnO_2), Antimony Oxide (Sb_2O_3), Tellurium Oxide (TeO_2), Iridium Oxide (IrO_2), Platinum Oxide (PtO_2), Gold Oxide (Au_2O_3), Beryllium Oxide (BeO), Magnesium Aluminate (MgAl_2O_4), Zinc Selenide (ZnSe), Zinc Telluride (ZnTe), Cadmium Sulfide (CdS), Cadmium Selenide (CdSe), Cadmium Telluride (CdTe), Silicon Germanium Oxide (SiGeO_x), Bismuth Oxide (Bi_2O_3), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Perovskite Oxides, Layered Oxides, and Complex Transition Metal Oxides.

[00771] 156. The integrated circuit as in one of aspects 124-155, wherein one of plurality of horizontal gate-electrode layers and the first vertical structure are configured to

form a plurality of transistors including the first transistor according to any one of aspects 1-96.

[00772] 157. An integrated circuit, comprising: a first vertical structure, comprising: a vertical plug column; a source electrode column disposed adjacent to the vertical plug column; a drain electrode column disposed adjacent to the vertical plug column; a channel column disposed around the vertical plug column, the source electrode column, and the drain electrode column; and a ferroelectric column disposed around the channel column; and a plurality of horizontal gate-electrode layers, each of the plurality of horizontal gate-electrode layers disposed a predetermined distance between each other, each of the plurality of horizontal gate-electrode layers disposed adjacent to the ferroelectric column along the length of the ferroelectric column.

[00773] 158. The integrated circuit according to aspect 157, wherein each of the horizontal gate-electrode layers includes an Oxide/Nitride/Oxide disposed adjacent thereto.

[00774] 159. The integrated circuit according to aspect 157, wherein the vertical plug column has a first diameter on a first end and a second diameter on the second end.

[00775] 160. The integrated circuit according to aspect 159, wherein the first diameter and the second diameter are the same.

[00776] 161. The integrated circuit according to aspect 159, wherein the first diameter is larger than the second diameter.

[00777] 162. The integrated circuit as in one of aspects 157-161, wherein the vertical plug column is solid.

[00778] 163. The integrated circuit as in one of aspects 157-161, wherein the vertical plug column is hollow.

[00779] 164. The integrated circuit according to any one of aspects 157-163, further comprising a second vertical structure.

[00780] 165. The integrated circuit according to aspect 164, wherein the second vertical structure is formed to be substantially identical to the first vertical structure but disposed adjacent the first vertical structure at a predetermined horizontal distance.

[00781] 166. The integrated circuit as in aspect 164 or 165, wherein the first and second vertical structures are configured to form a 3D AND-structure.

[00782] 167. The integrated circuit as in aspect 164 or 165, wherein the first and second vertical structures are configured to form a 3D NOR-structure.

[00783] 168. The integrated circuit as in one of aspects 157-167, wherein the plurality of horizontal gate-electrode layers is formed from at least one of Tungsten, Titanium Nitride,

Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu, TiW, and Conducting Polymers.

[00784] 169. The integrated circuit as in one of aspects 157-168, wherein source electrode column is formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu, TiW, and Conducting Polymers.

[00785] 170. The integrated circuit as in one of aspects 157-169, wherein the gate electrode column is formed from at least one of Tungsten, Titanium Nitride, Tantalum Nitride, Nickel, Molybdenum, Platinum, Palladium, Cobalt, Gold, Aluminum, Copper, Hafnium, Hafnium Nitride, Iridium, Iridium Oxide, Ruthenium, Ruthenium Oxide, Silicides, TiSi_2 , CoSi_2 , NiSi , Graphene, Carbon Nanotubes, Doped Polysilicon, Indium Tin Oxide, Silver, Aluminum-doped Zinc Oxide, Gallium, Gallium Arsenide, Indium Gallium Zinc Oxide, Metal Alloys, AlCu, TiW, and Conducting Polymers.

[00786] 171. The integrated circuit as in one of aspects 157-170, wherein the ferroelectric column is formed from at least one of Perovskites, Lead Zirconate Titanate (PZT), Barium Titanate (BaTiO_3), Strontium Titanate (SrTiO_3), Bismuth Ferrite (BiFeO_3), Potassium Niobate (KNbO_3), Lithium Niobate (LiNbO_3), Lithium Tantalate (LiTaO_3), Sodium Bismuth Titanate ($\text{Na}_{0.5}\text{Bi}_{0.5}\text{TiO}_3$), Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Bismuth Zinc Niobate ($\text{Bi}(\text{Zn}_{1/2}\text{Ti}_{1/2})\text{O}_3$), Bismuth Lanthanum Titanate (BiLaTiO_3), Bismuth Nickel Titanate (BiNiTiO_3), Lead Magnesium Niobate-Lead Titanate (PMN-PT), Lead Lanthanum Zirconate Titanate (PLZT), Neodymium-doped Bismuth Titanate ($\text{Bi}_{4-x}\text{Nd}_x\text{Ti}_3\text{O}_{12}$), Hafnium-based Oxides, Hafnium Oxide (HfO_2), Doped Hafnium Oxide, Zirconium-doped Hafnium Oxide (HfZrO_2), Tungsten Bronze Structure Materials, Barium Strontium Niobate (BSN), Lead Barium Niobate (PBN), Potassium Tantalate Niobate (KTN), Bismuth Layer-Structured Ferroelectrics, Bismuth Titanate ($\text{Bi}_4\text{Ti}_3\text{O}_{12}$), Strontium Bismuth Tantalate (SBT), Calcium Bismuth Niobate (CBN), Organic Ferroelectrics, Polyvinylidene Fluoride (PVDF), TrFE (Trifluoroethylene), P(VDF-TrFE) Copolymers, Aurivillius Phase Oxides, Rare Earth Manganites, YMnO_3 , Lanthanum-modified Lead Zirconate Titanate (PLZT), Nickel

Manganese Oxide (NiMnO₃), Relaxor Ferroelectrics, Lead Magnesium Niobate (PMN), Lead Scandium Tantalate (PST), Lead Indium Niobate (PIN), Multiferroic Materials, Terbium Manganite (TbMnO₃), Europium Titanium Oxide (EuTiO₃), SbSI (Antimony Sulfoiodide), GeTe (Germanium Telluride), SnTe (Tin Telluride), Thin-Film Ferroelectrics, PZT Thin Films, SBT Thin Films, HfO₂-based Thin Films, Layered Superlattices, and PbTiO₃/SrTiO₃.

[00787] 172. The integrated circuit as in one of aspects 157-171, wherein the channel column is formed from at least one of Indium Gallium Zinc Oxide (IGZO), Indium Zinc Oxide (IZO), Zinc Tin Oxide (ZTO), Aluminum Zinc Oxide (AZO), Indium Tungsten Oxide (IWO), Gallium Zinc Oxide (GZO), Hafnium Indium Oxide (HIO), and Cadmium Oxide (CdO), Polysilicon, Polygermanium Cadmium Selenide (CdSe), Copper Indium Gallium Selenide (CIGS), Crystalline Silicon (c-Silicon), Crystalline Germanium (c-Germanium), Gallium Arsenide (GaAs), Indium Phosphide (InP), Indium Antimonide (InSb), Silicon Carbide (SiC), Gallium Nitride (GaN), Zinc Oxide (ZnO), Pentacene, P3HT (Poly(3-hexylthiophene)), Polythiophene, Polyphenylene vinylene (PPV), Graphene, Carbon Nanotubes (CNTs), Methylammonium Lead Halides (CH₃NH₃PbX₃, X = Cl, Br, I), Cesium Lead Halide (CsPbX₃, X = Cl, Br, I), Lead Sulfide (PbS), Lead Selenide (PbSe), Cadmium Selenide (CdSe), Indium Arsenide (InAs), Skutterudites, Ruddlesden-Popper phases, Clathrates, Perovskite Oxides, and Magnetic Semiconductors.

[00788] 173. The integrated circuit as in one of aspects 157-172, wherein the vertical plug column is formed from at least one of Hafnium Oxide (HfO₂), Zirconium Oxide (ZrO₂), Aluminum Oxide (Al₂O₃), Silicon Dioxide (SiO₂), Titanium Dioxide (TiO₂), Tantalum Oxide (Ta₂O₅), Lanthanum Oxide (La₂O₃), Yttrium Oxide (Y₂O₃), Silicon Nitride (Si₃N₄), Aluminum Nitride (AlN), Silicon Carbide (SiC), Strontium Titanate (SrTiO₃), Barium Strontium Titanate (BST), Lead Zirconate Titanate (PZT), Bismuth Ferrite (BiFeO₃), Magnesium Oxide (MgO), Cerium Oxide (CeO₂), Nickel Oxide (NiO), Cobalt Oxide (CoO), Copper Oxide (CuO), Manganese Oxide (MnO), Zinc Oxide (ZnO), Gadolinium Oxide (Gd₂O₃), Dysprosium Oxide (Dy₂O₃), Samarium Oxide (Sm₂O₃), Europium Oxide (Eu₂O₃), Terbium Oxide (Tb₄O₇), Vanadium Oxide (V₂O₅), Niobium Oxide (Nb₂O₅), Chromium Oxide (Cr₂O₃), Iron Oxide (Fe₂O₃), Molybdenum Oxide (MoO₃), Tungsten Oxide (WO₃), Ruthenium Oxide (RuO₂), Rhodium Oxide (Rh₂O₃), Palladium Oxide (PdO), Silver Oxide (Ag₂O), Cadmium Oxide (CdO), Tin Oxide (SnO₂), Antimony Oxide (Sb₂O₃), Tellurium Oxide (TeO₂), Iridium Oxide (IrO₂), Platinum Oxide (PtO₂), Gold Oxide (Au₂O₃), Beryllium Oxide (BeO), Magnesium Aluminate (MgAl₂O₄), Zinc Selenide (ZnSe), Zinc Telluride (ZnTe), Cadmium Sulfide (CdS), Cadmium Selenide (CdSe), Cadmium Telluride (CdTe),

Silicon Germanium Oxide (SiGeO_x), Bismuth Oxide (Bi₂O₃), Bismuth Titanate (Bi₄Ti₃O₁₂), Perovskite Oxides, Layered Oxides, and Complex Transition Metal Oxides.

[00789] 174. The integrated circuit as in one of aspects 157-173, wherein one of plurality of horizontal gate-electrode layers and the first vertical structure are configured to form a plurality of transistors including the first transistor according to any one of aspects 1-96.

[00790] 175. The integrated circuit according to aspect 6, wherein the transition metal dichalcogenide (TMD) may be written as MX₂, wherein M refers to transition metal atom, and X is the chalcogen atom.

[00791] 176. The integrated circuit according to aspect 6, wherein the TMD is selected from the group consisting of molybdenum disulfide (MoS₂), molybdenum diselenide (MoSe₂), tungsten disulfide (WS₂), tungsten diselenide (WSe₂), molybdenum ditelluride (MoTe₂), tungsten ditelluride (WTe₂), titanium diselenide (TiSe₂), niobium disulfide (NbS₂), titanium disulfide (TiS₂), nickel disulfide (NiS₂), and vanadium diselenide (VSe₂), niobium diselenide (NbSe₂), and tantalum sulfide (TaS₂).

What is claimed is:

1. An integrated circuit, comprising:
 - a first transistor comprising:
 - a channel layer formed using a semiconductor material; and
 - a ferroelectric rigidly coupled to the channel layer;
 - a source terminal fixed to the channel layer;
 - a drain terminal fixed to the channel layer; and
 - a gate terminal fixed to the ferroelectric layer.
2. An integrated circuit as claimed or disclosed herein wherein the channel layer is formed from a polycrystalline silicon.
3. An integrated circuit as claimed or disclosed herein wherein the channel layer is formed from an Amorphous Oxide Semiconductor.
4. The integrated circuit according to claim 3 wherein the Amorphous Oxide Semiconductor includes at least one of Indium Oxide, Indium Gallium Zinc Oxide, Zinc Tin Oxide, Indium Zinc Oxide, Gallium Zinc Oxide, Aluminum Zinc Oxide, Cadmium Oxide, Hafnium Indium Zinc Oxide, Tin Oxide, stannous Tin Oxide, stannic Tin Oxide, Indium-Tin-Zinc Oxide, Indium-Tungsten Oxide, Indium-Gallium-Zinc-Tin Oxide, Indium-Gallium-Zinc-Oxynitride, Aluminum-Indium-Gallium-Zinc Oxide, and Zinc-Indium Oxide.
5. The integrated circuit according to claim 3, wherein the Amorphous Oxide Semiconductor is doped with at least one of Gallium (Ga), Indium (In), Zinc (Zn), Tin (Sn), Hafnium (Hf), Silicon (Si), Aluminum (Al), Magnesium (Mg), Calcium (Ca), Strontium (Sr), Barium (Ba), Titanium (Ti), Zirconium (Zr), Molybdenum (Mo), Tantalum (Ta), Niobium (Nb), Chromium (Cr), Iron (Fe), Cobalt (Co), Nickel (Ni), Copper (Cu), Silver (Ag), Gold (Au), Cerium (Ce), Lanthanum (La), Neodymium (Nd), Samarium (Sm), Europium (Eu), Gadolinium (Gd), Terbium (Tb), Dysprosium (Dy), Holmium (Ho), Erbium (Er), Thulium (Tm), Ytterbium (Yb), Lutetium (Lu), Yttrium (Y), Scandium (Sc), Bismuth (Bi), Lead (Pb), Thallium (Tl), Antimony (Sb), Arsenic (As), Phosphorus (P), Boron (B), Nitrogen (N), Fluorine (F), Chlorine (Cl), Bromine (Br), and Iodine (I).
6. The integrated circuit according to 1, further comprising:
 - a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer; and
 - an insulation layer disposed on the channel layer, wherein the ferroelectric layer is also disposed on the insulation layer.

7. The integrated circuit according to claim 1, further comprising a metal layer disposed on the ferroelectric layer, wherein the ferroelectric layer is disposed on the channel layer.
8. The integrated circuit according to claim 1, wherein the channel layer is less than 30 nm in thickness.
9. The integrated circuit according to claim 1, wherein the channel layer is between 1 to 30 nm in thickness.
10. The integrated circuit according to claim 1, wherein the channel layer is configured to have a carrier concentration of 10^{17} to 10^{20} per centimeter-cubed.
11. The integrated circuit according to claim 1, wherein the channel layer comprises a two-dimensional material.
12. The integrated circuit according to claim 11, wherein the two-dimensional material maintains an electron mobility of at least 0.1 cm-squared per Volt-second when the channel layer is less than 30nm in thickness.
13. The integrated circuit according to claim 12, wherein the channel layer comprises fewer than 5 monolayers of the two-dimensional material.
14. The integrated circuit according to claim 1, wherein the ferroelectric layer is Hafnium Zirconium Oxide.
15. The integrated circuit according to claim 1, wherein a coercive voltage of the ferroelectric layer is between -3 Volts to 3 Volts.
16. The integrated circuit according to claim 1, wherein an off-state current of the ferroelectric layer is less than 10^{-7} amps per centimeter cubed.
17. The integrated circuit according to claim 1, wherein an on-state current of the ferroelectric layer is greater than 10^{-7} amps per centimeter cubed.
18. The integrated circuit according to claim 1, wherein a crystallization anneal temperature of the ferroelectric layer is less than or equal to 500 degrees Celsius.
19. The integrated circuit according to claim 1, wherein a remanent polarization of the ferroelectric layer is greater than 10 microcoulombs per square centimeter.
20. The integrated circuit according to claim 1, wherein an anneal temperature of the channel layer is less than 450 Celsius.
21. The integrated circuit according to claim 1, wherein a channel mobility of the channel layer is less than 100 centimeters squared per Volt-second.

22. The integrated circuit according to claim 1, wherein a subthreshold swing of the channel layer is less than 0.3 volts per decade.
23. The integrated circuit according to claim 1, wherein the channel layer is configured to have an off-state current of less than 10^{-7} amps per micrometer.
24. The integrated circuit according to claim 1, wherein the channel layer is configured to have a channel bandgap of greater than 2.5 electron-volts.
25. The integrated circuit according to claim 1, wherein the channel layer is configured to have a post-anneal threshold voltage between -1.5 Volts to 1.5 Volts.
26. The integrated circuit according to claim 1, wherein the first transistor has a width of less than 200nm and a length of 50 nano meters.