

CLAIMS:

1. A semiconductor package, comprising:

a package substrate having a first side and a second side opposite the first side, the package substrate comprising:

- a first layer of dielectric material adjacent the first side of the package substrate;
- a second layer of dielectric material on the first layer of dielectric material, the first layer of dielectric material being between the second layer of dielectric material and the first side of the package substrate;
- a ground solder ball pad adjacent the first side of the package substrate;
- a first via above and electrically coupled to the ground solder ball pad, the first via being in the first layer of dielectric material of the package substrate;
- a second via above and electrically coupled to the ground solder ball pad, the second via being in the first layer of dielectric material of the package substrate, the second via laterally spaced apart from the first via;
- a third via above and electrically coupled to the first via and being in the second layer of dielectric material of the package substrate;
- a fourth via above and electrically coupled to the second via and being in the second layer of dielectric material of the package substrate, the fourth via laterally spaced apart from the third via;
- wherein a first line perpendicular to the first side of the package substrate intersects the ground solder ball pad, the first via, and the third via; and
- wherein a second line perpendicular to the first side of the package substrate intersects the ground solder ball pad, the second via, and the fourth via;

a die coupled to the second side of the package substrate; and

a solder ball disposed on the ground solder ball pad.

2. The semiconductor package of claim 1, wherein the first layer of dielectric material comprises epoxy and silica.

3. The semiconductor package of claim 1, further comprising:

- a third layer of dielectric material on the second layer of dielectric material;
- a fifth via above and electrically coupled to the third via and being in the third layer of dielectric material of the package substrate;
- a sixth via above and electrically coupled to the fourth via and being in the third layer of dielectric material of the package substrate, the sixth via laterally spaced apart from the fifth via;

wherein the first line perpendicular to the first side of the package substrate intersects the ground solder ball pad, the first via, the third via, and the fifth via; and
wherein the second line perpendicular to the first side of the package substrate intersects the ground solder ball pad, the second via, the fourth via, and the sixth via.

4. The semiconductor package of claim 1, further comprising a seventh via above and electrically coupled to the ground solder ball pad, the seventh via being in the first layer of dielectric material of the package substrate, the seventh via laterally spaced apart from the first via and from the second via.

5. The semiconductor package of claim 1, further comprising a plurality of signal ball pads surround the ground ball pad.

6. The semiconductor package of claim 5, wherein the plurality of signal ball pads surrounding the ground ball pad are in a hexagonal arrangement.

7. The semiconductor package of claim 1, further comprising a second die.

8. The semiconductor package of claim 7, wherein the die is a processor die and the second die is a memory die.

9. A method of making a semiconductor package, comprising:

forming a package substrate having a first side and a second side opposite the first side, wherein forming the package substrate comprises:

forming a first layer of dielectric material adjacent the first side of the package substrate;
forming a second layer of dielectric material on the first layer of dielectric material, the first layer of dielectric material being between the second layer of dielectric material and the first side of the package substrate;

forming a ground solder ball pad adjacent the first side of the package substrate;

forming a first via above and electrically coupled to the ground solder ball pad, the first via being in the first layer of dielectric material of the package substrate;

forming a second via above and electrically coupled to the ground solder ball pad, the second via being in the first layer of dielectric material of the package substrate, the second via laterally spaced apart from the first via;

forming a third via above and electrically coupled to the first via and being in the second layer of dielectric material of the package substrate;

forming a fourth via above and electrically coupled to the second via and being in the second layer of dielectric material of the package substrate, the fourth via laterally spaced apart from the third via;
wherein a first line perpendicular to the first side of the package substrate intersects the ground solder ball pad, the first via, and the third via; and
wherein a second line perpendicular to the first side of the package substrate intersects the ground solder ball pad, the second via, and the fourth via;
coupling a die to the second side of the package substrate; and
disposing a solder ball on the ground solder ball pad.

10. The method of making the semiconductor package of claim 9, wherein the first layer of dielectric material comprises epoxy and silica.

11. The method of making the semiconductor package of claim 9, further comprising a fifth via above and electrically coupled to the ground solder ball pad, the fifth via being in the first layer of dielectric material of the package substrate, the fifth via laterally spaced apart from the first via and from the second via.

12. The method of making the semiconductor package of claim 9 further comprising a plurality of signal ball pads surround the ground ball pad.

13. The method of making the semiconductor package of claim 12, wherein the plurality of signal ball pads surrounding the ground ball pad are in a hexagonal arrangement.

14. A computing device, comprising:

a touchscreen display;

a battery;

a motherboard;

a package substrate coupled to the motherboard, the package substrate comprising:

a first layer of dielectric material;

a second layer of dielectric material on the first layer of dielectric material;

a ground solder ball pad between the first layer of dielectric material and the motherboard;

a first via electrically coupled to the ground solder ball pad, the first via being in the first layer of dielectric material of the package substrate;

a second via electrically coupled to the ground solder ball pad, the second via being in the first layer of dielectric material of the package substrate, the second via laterally spaced apart from the first via;

a third via electrically coupled to the first via and being in the second layer of dielectric material of the package substrate;

a fourth via electrically coupled to the second via and being in the second layer of dielectric material of the package substrate, the fourth via laterally spaced apart from the third via;

wherein the ground solder ball pad, the first via, and the third via are in a first vertical interconnect stack; and

wherein the ground solder ball pad, the second via, and the fourth via are in a second vertical interconnect stack; and

a processor die coupled to the package substrate, the package substrate being between the processor die and the motherboard.

15. The computing device of claim 14, wherein the first layer of dielectric material comprises epoxy.

16. The computing device of claim 14, further comprising:

a third layer of dielectric material on the second layer of dielectric material;

a fifth via electrically coupled to the third via and being in the third layer of dielectric material of the package substrate;

a sixth via electrically coupled to the fourth via and being in the third layer of dielectric material of the package substrate, the sixth via laterally spaced apart from the fifth via;

wherein the first vertical interconnect stack includes the fifth via; and

wherein the second vertical interconnect stack includes the sixth via.

17. The computing device of claim 14, further comprising a seventh via above and electrically coupled to the ground solder ball pad, the seventh via being in the first layer of dielectric material of the package substrate, the seventh via laterally spaced apart from the first via and from the second via.

18. The computing device of claim 14, further comprising a plurality of signal ball pads surround the ground ball pad.

19. The computing device of claim 18, wherein the plurality of signal ball pads surrounding the ground ball pad are in a hexagonal arrangement.

20. The computing device of claim 14, further comprising a wireless communication chip and a memory chip.