G00002

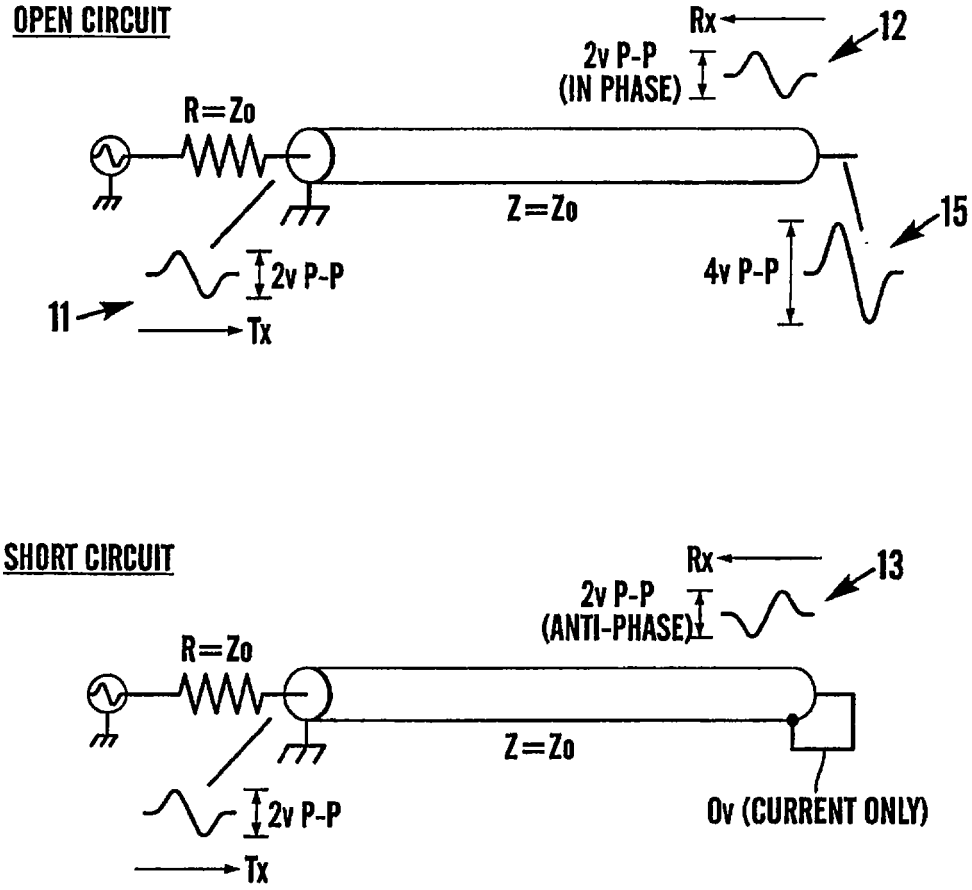
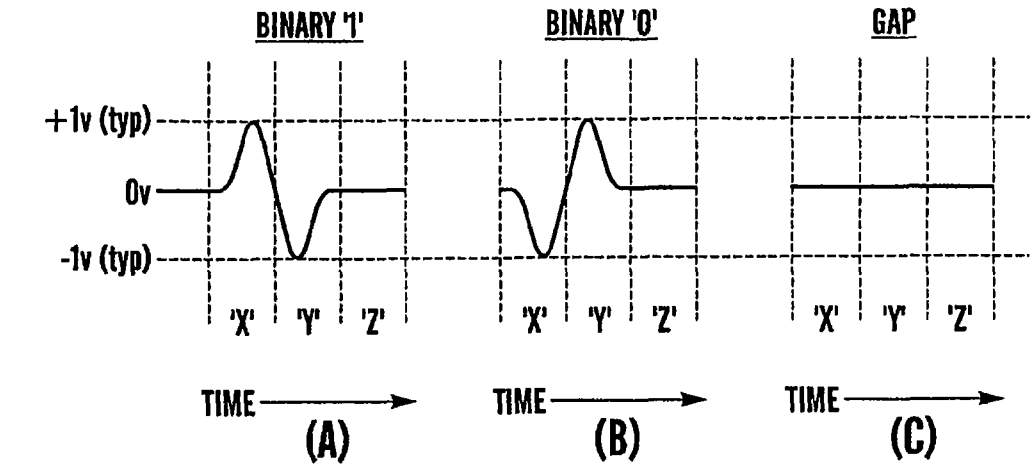
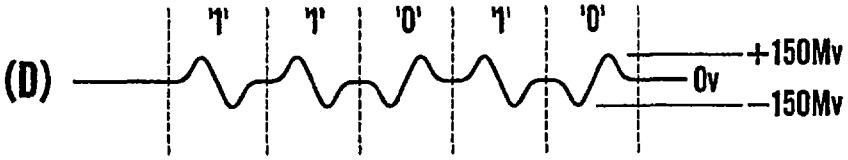
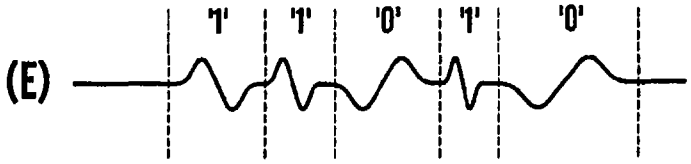


Fig. 1

163163


BINARY '1'
BINARY '0'
GAP
+1v (typ)
0v
-1v (typ)
'X' 'Y' 'Z'
TIME
(A)
(B)
(C)


(D)
'1' '1' '0' '1' '0'
+150Mv
0v
-150Mv


(E)
'1' '1' '0' '1' '0'

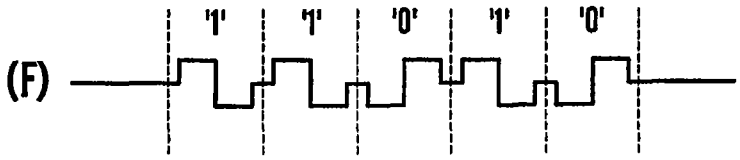
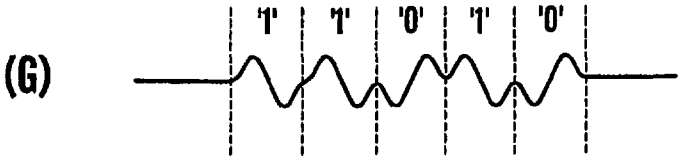
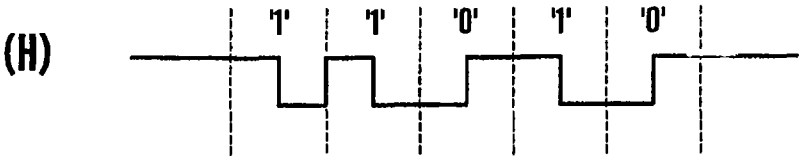
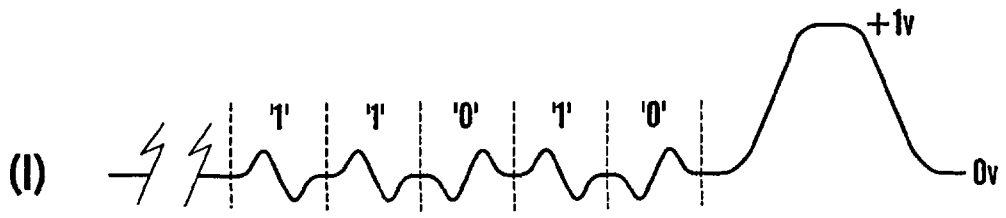

(F)
'1' '1' '0' '1' '0'

Fig.2


(G)
'1' '1' '0' '1' '0'


(H)
'1' '1' '0' '1' '0'


(I)
'1' '1' '0' '1' '0'
+1v
0v

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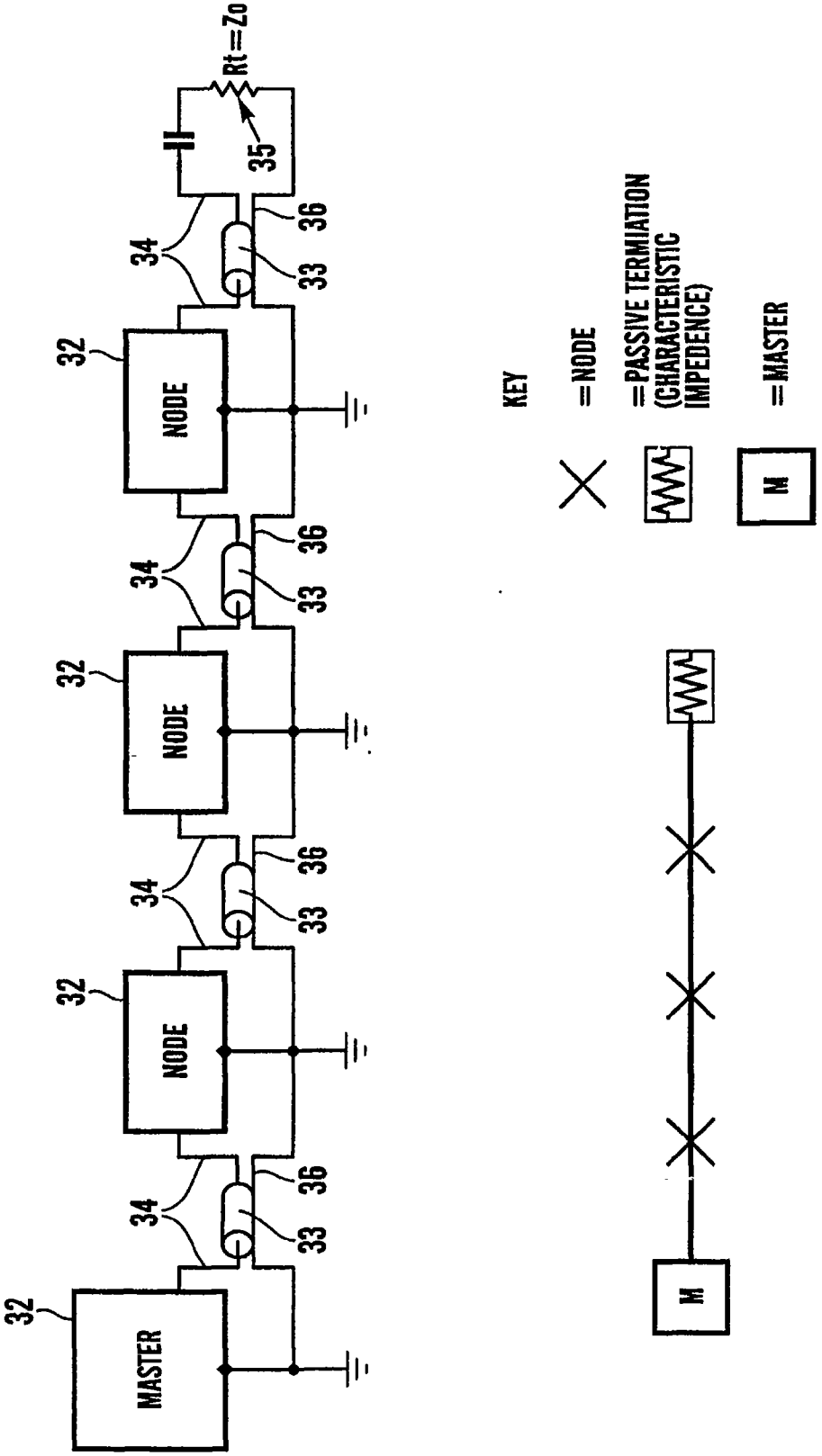


Fig.3

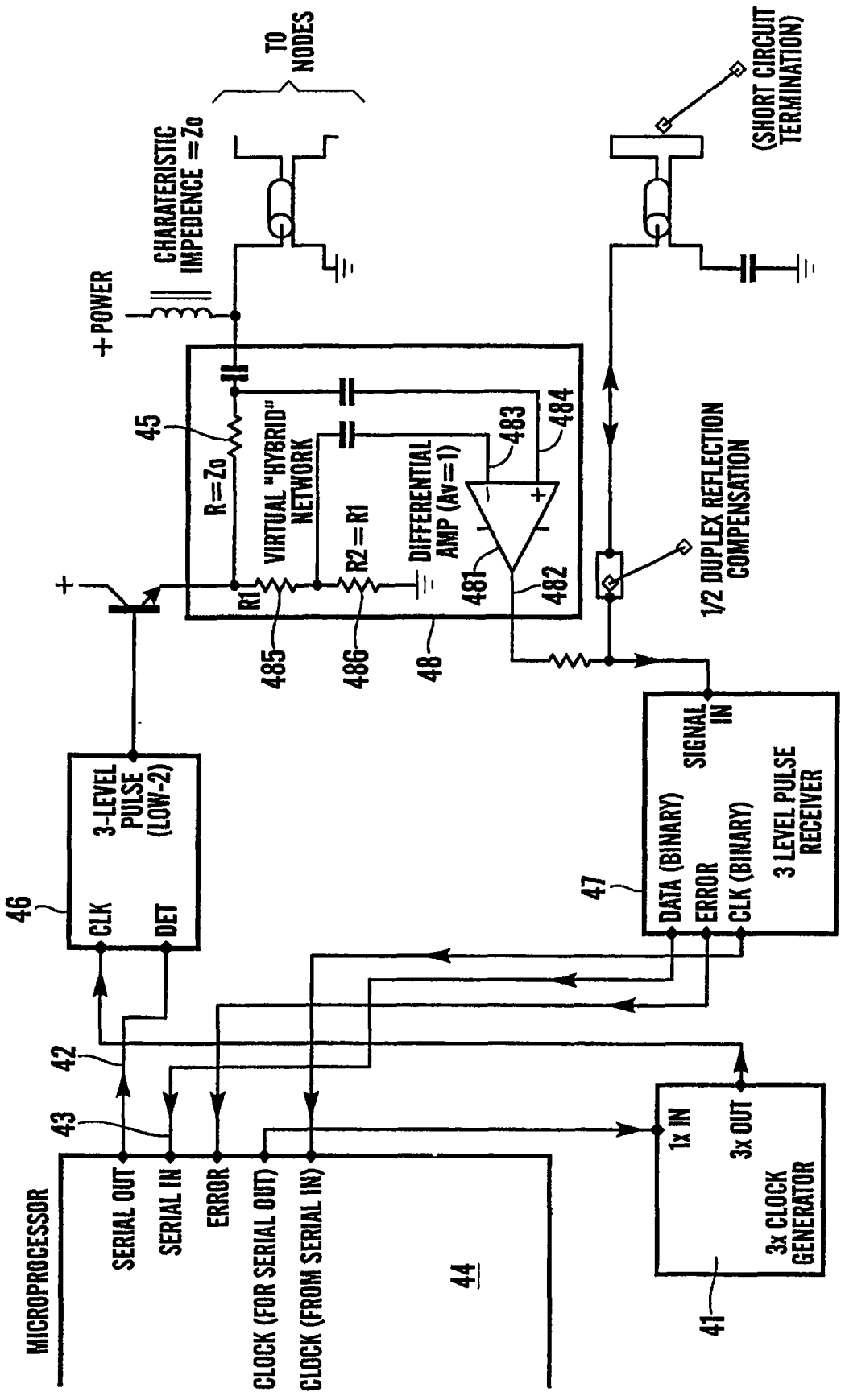

MICROPROCESSOR
SERIAL OUT
SERIAL IN
ERROR
CLOCK (FOR SERIAL OUT)
CLOCK (FROM SERIAL IN)
44
42
43
41
1x IN
3x OUT
3x CLOCK GENERATOR
46
CLK
DET
3-LEVEL PULSE (LOW-2)
47
DATA (BINARY)
ERROR
CLK (BINARY)
SIGNAL IN
3 LEVEL PULSE RECEIVER
1/2 DUPLEX REFLECTION COMPENSATION
(SHORT CIRCUIT TERMINATION)
TO NODES
CHARATERISTIC IMPEDENCE = Zo
+ POWER
45
R=Zo
VIRTUAL "HYBRID" NETWORK
R2=R1
DIFFERENTIAL AMP (Av=1)
R1
481
482
483
484
485
486
48

Fig.4

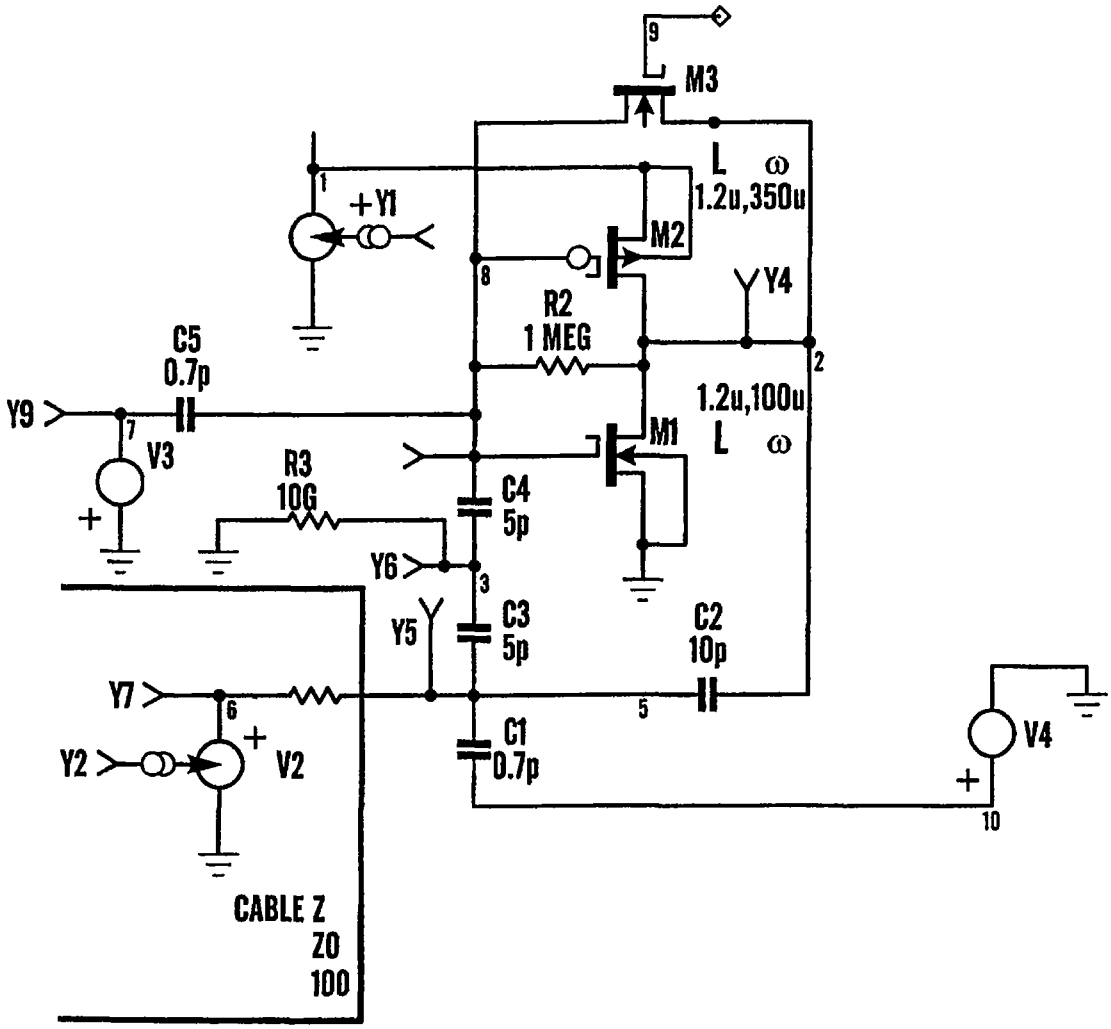

9
M3
L ω
1.2u,350u
1
+Y1
M2
8
Y4
R2
1 MEG
C5
0.7p
2
Y9
7
V3
1.2u,100u
M1
L ω
R3
10G
C4
5p
Y6
3
Y5
C3
5p
C2
10p
Y7
6
5
V4
Y2
V2
C1
0.7p
10
CABLE Z
Z0
100

Fig.4A

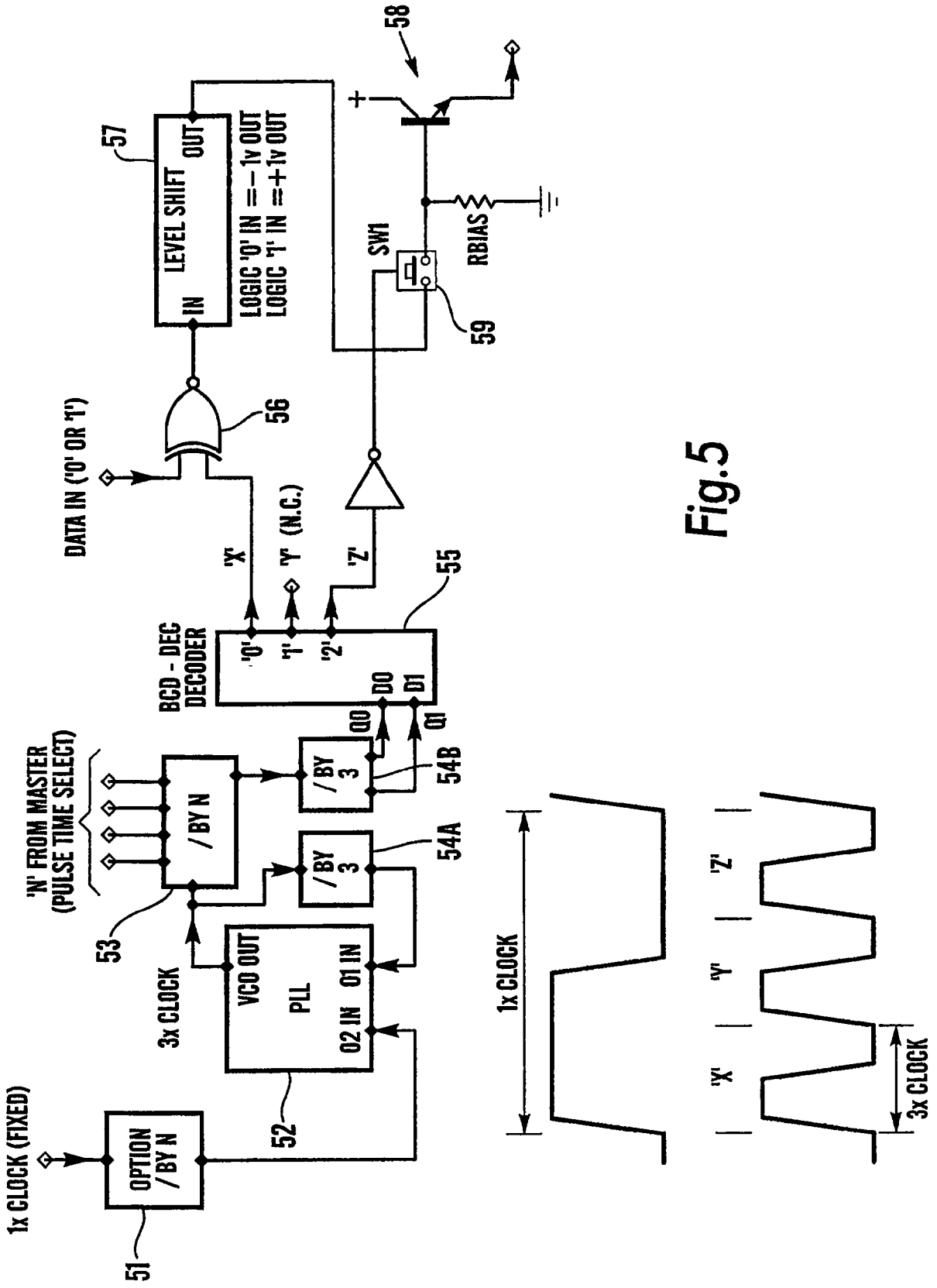

1x CLOCK (FIXED)
OPTION / BY N
51
52
PLL
VCO OUT
01 IN
02 IN
3x CLOCK
53
'N' FROM MASTER (PULSE TIME SELECT)
/ BY N
/ BY 3
54A
/ BY 3
54B
BCD - DEC DECODER
'0'
'1'
'2'
D0
D1
Q0
Q1
55
DATA IN ('0' OR '1')
56
'X'
'Y' (N.C.)
'Z'
57
LEVEL SHIFT
IN
OUT
LOGIC '0' IN = -1v OUT
LOGIC '1' IN = +1v OUT
58
SW1
59
RBIAS
1x CLOCK
'X'
'Y'
'Z'
3x CLOCK

Fig.5

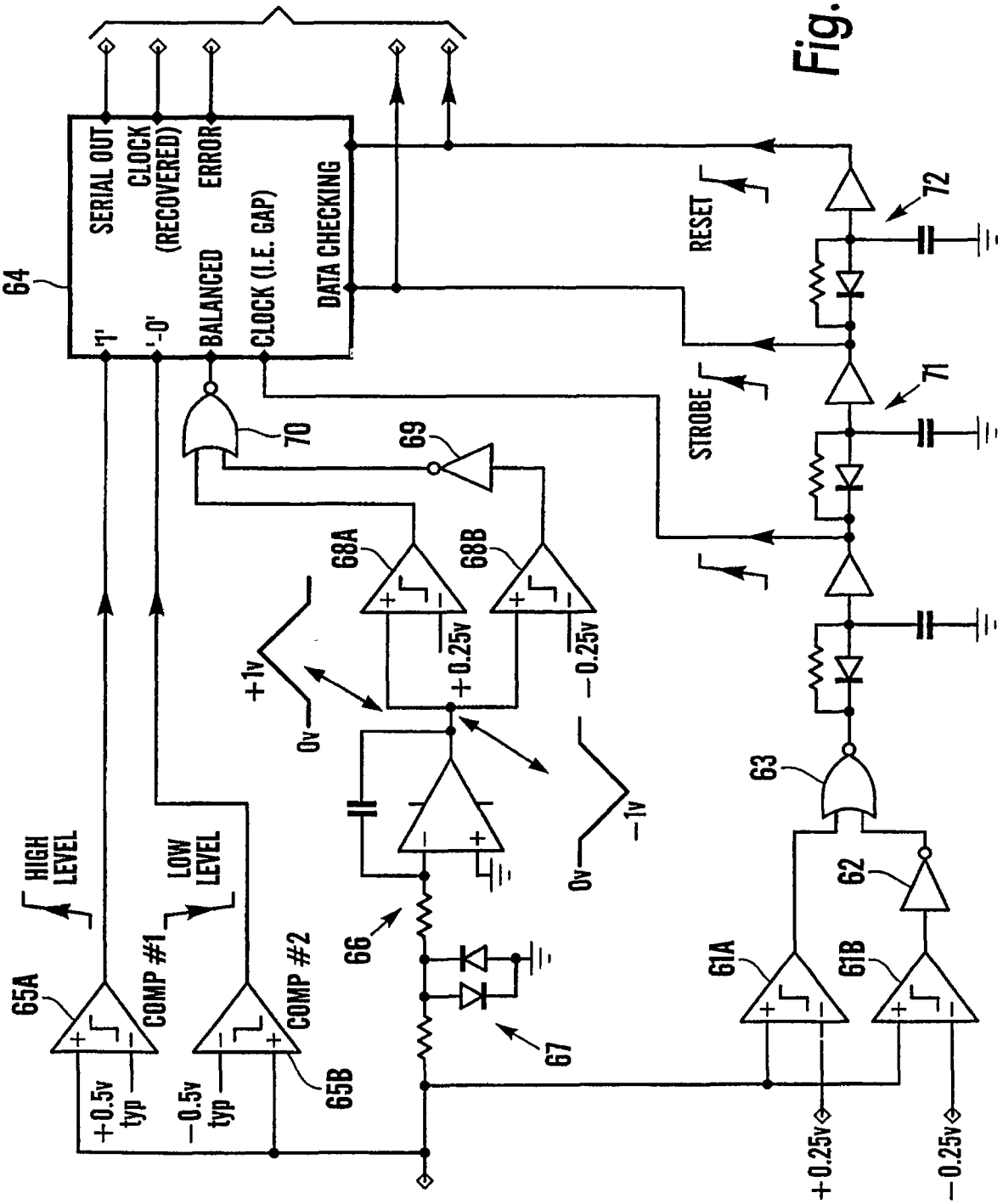

64
SERIAL OUT
CLOCK (RECOVERED)
ERROR
BALANCED
CLOCK (I.E. GAP)
DATA CHECKING
'1'
'-0'
70
69
68A
68B
+0.25v
-0.25v
+1v
0v
-1v
0v
66
67
65A
65B
COMP #1
COMP #2
HIGH LEVEL
LOW LEVEL
+0.5v typ
-0.5v typ
63
62
61A
61B
+0.25v
-0.25v
RESET
STROBE
72
71

Fig.6

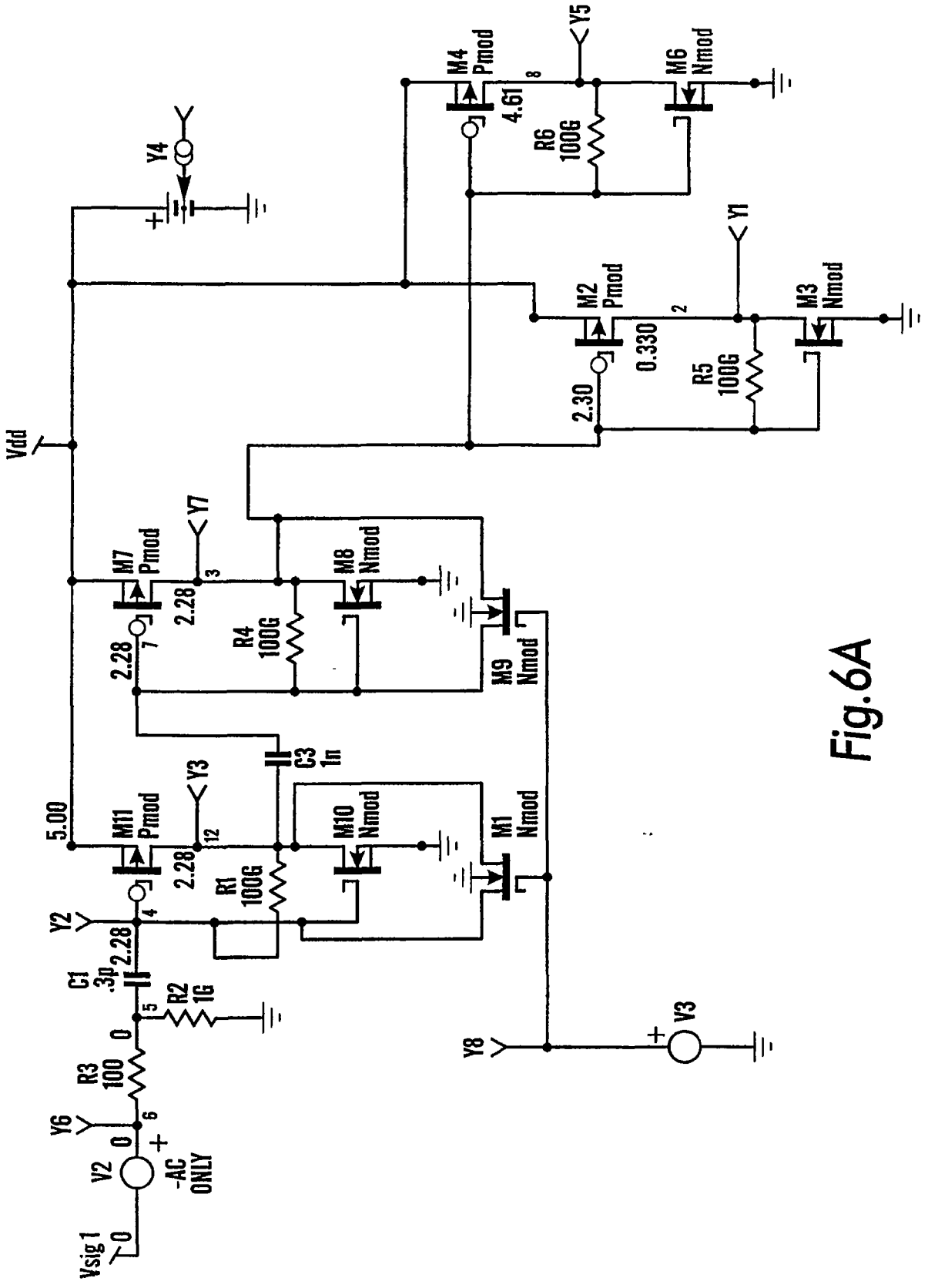

Vdd
5.00
Y4
Y5
M4 Pmod
4.61
8
M6 Nmod
R6 100G
Y1
M2 Pmod
2
M3 Nmod
0.330
2.30
R5 100G
Y7
M7 Pmod
3
2.28
M8 Nmod
2.28
7
R4 100G
M9 Nmod
C3 1n
Y3
M11 Pmod
12
2.28
M10 Nmod
M1 Nmod
R1 100G
Y2
4
2.28
C1 .3p
R2 1G
5
0
R3 100
Y6
6
0
V2
-AC
ONLY
Vsig1
0
Y8
V3

Fig.6A

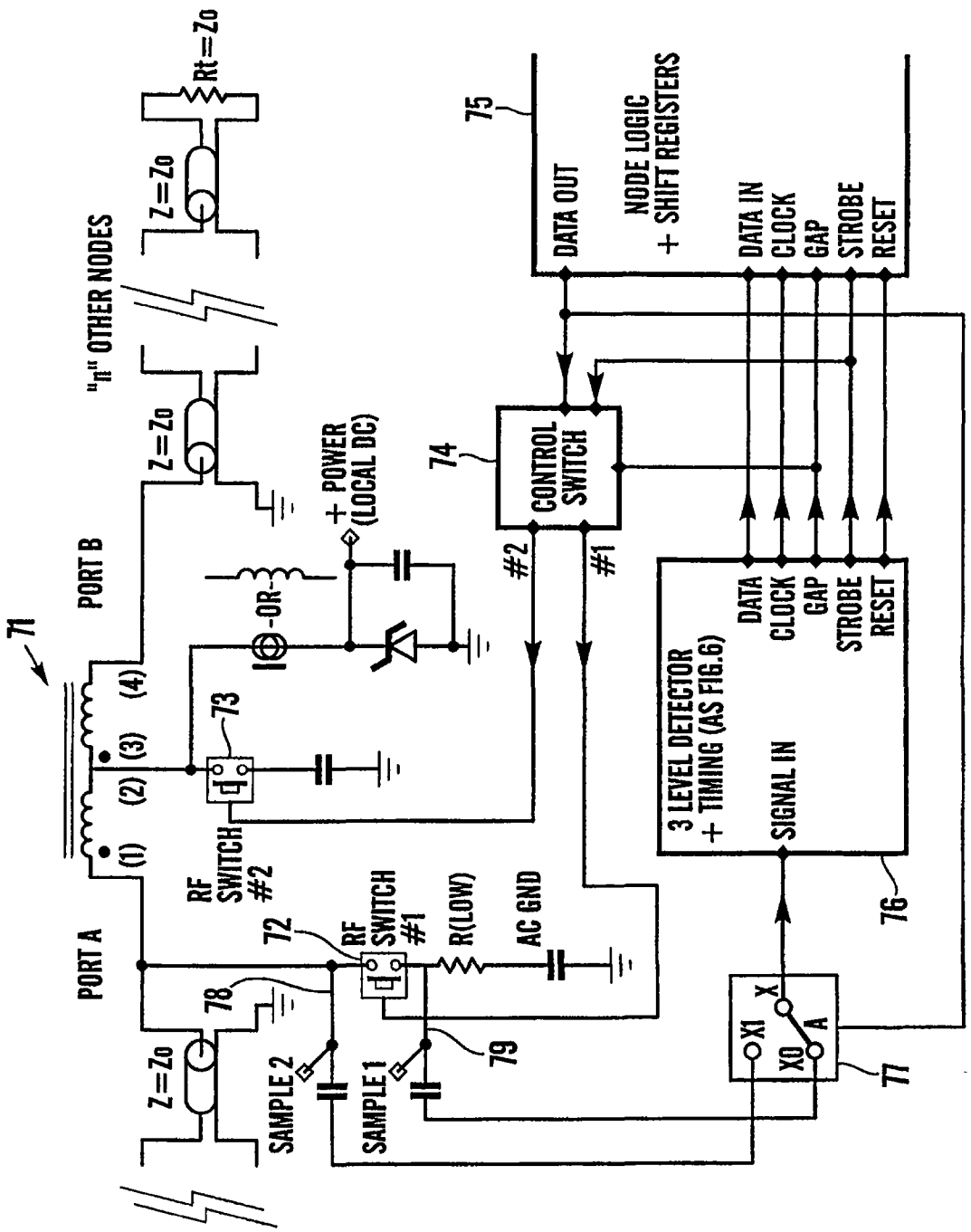

71
PORT B
PORT A
(1)
(2)
(3)
(4)
"n" OTHER NODES
Z=Zo
Rt=Zo
+ POWER (LOCAL DC)
-OR-
73
RF SWITCH #2
72
RF SWITCH #1
R(LOW)
AC GND
78
79
SAMPLE 2
SAMPLE 1
74
CONTROL SWITCH
#2
#1
75
DATA OUT
NODE LOGIC + SHIFT REGISTERS
DATA IN
CLOCK
GAP
STROBE
RESET
3 LEVEL DETECTOR + TIMING (AS FIG.6)
SIGNAL IN
DATA
CLOCK
GAP
STROBE
RESET
76
77
X
A
X1
X0

Fig.7

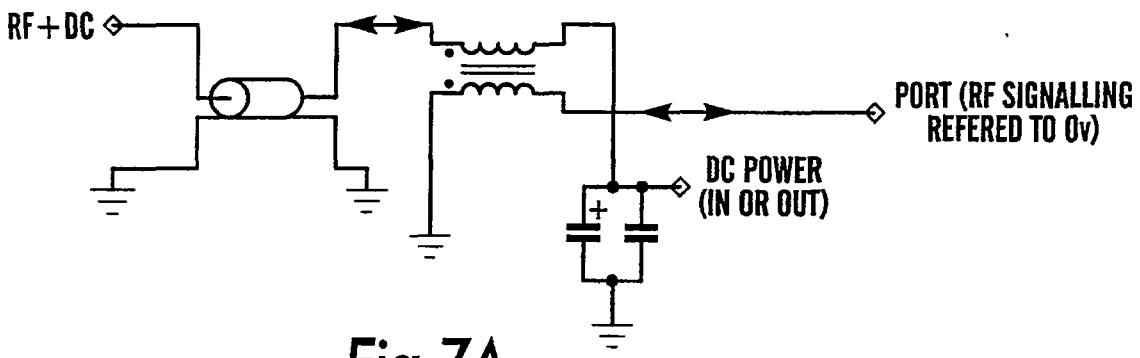


Fig.7A

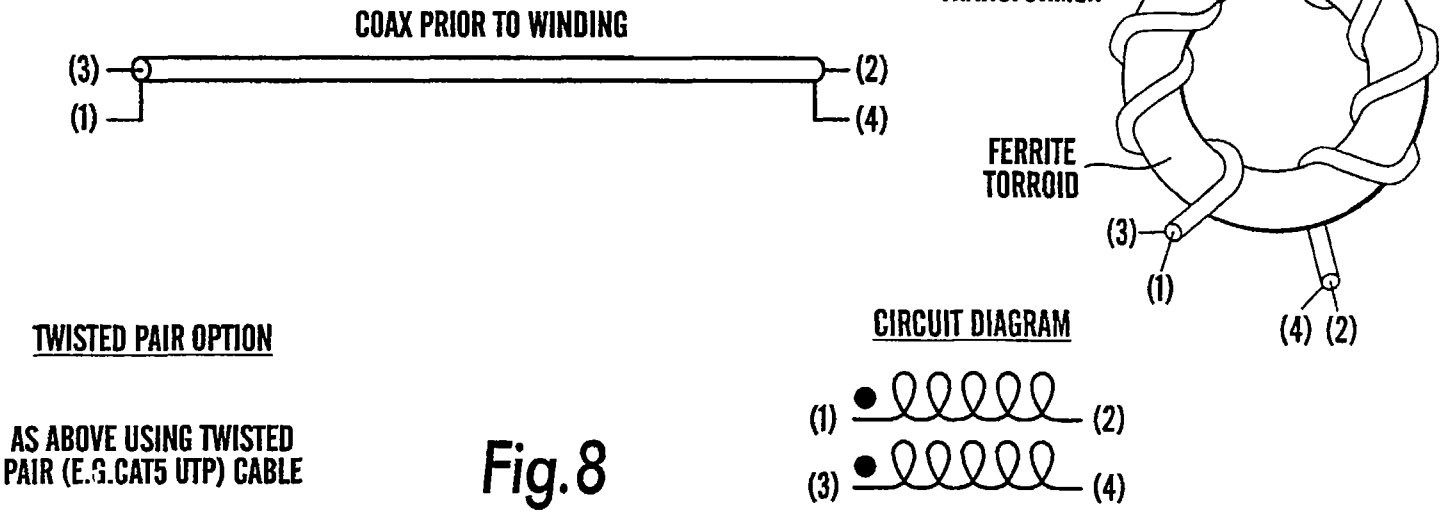


Fig.8

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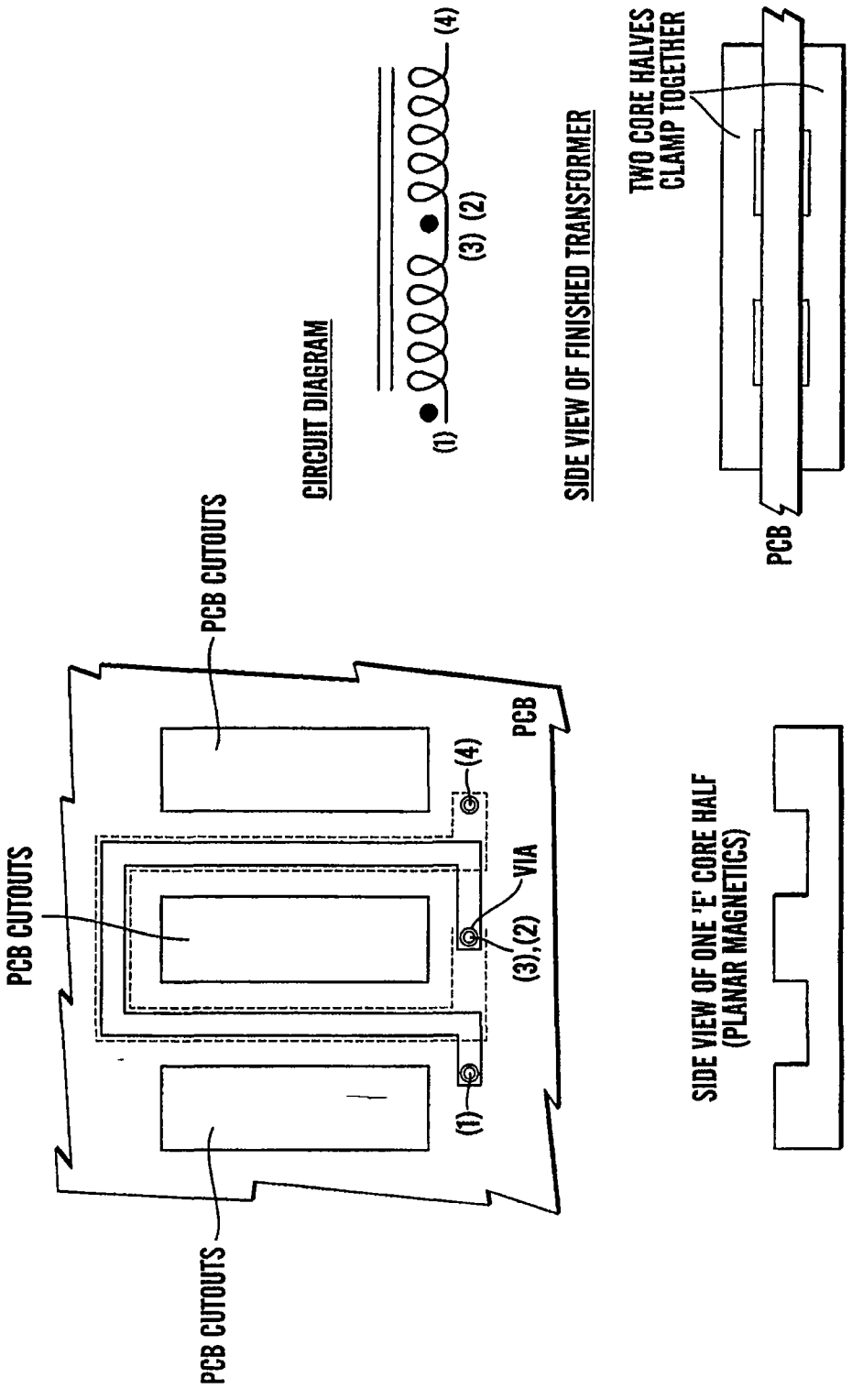

PCB CUTOUTS
PCB CUTOUTS
PCB CUTOUTS
PCB
(4)
VIA
(3),(2)
(1)
CIRCUIT DIAGRAM
(1)
(3) (2)
(4)
SIDE VIEW OF FINISHED TRANSFORMER
TWO CORE HALVES CLAMP TOGETHER
PCB
SIDE VIEW OF ONE 'E' CORE HALF (PLANAR MAGNETICS)

Fig.9

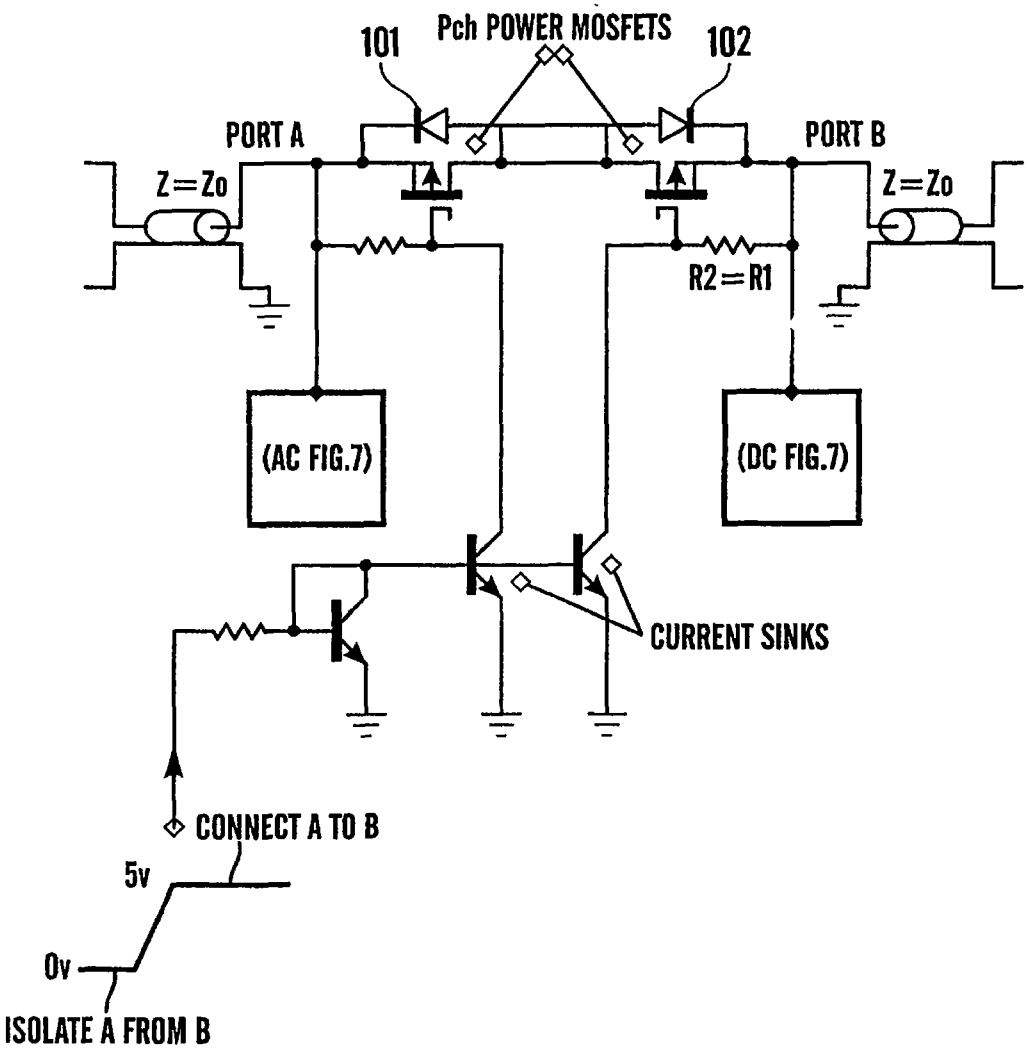

101
Pch POWER MOSFETS
102
PORT A
PORT B
Z=Zo
Z=Zo
R2=R1
(AC FIG.7)
(DC FIG.7)
CURRENT SINKS
CONNECT A TO B
5v
0v
ISOLATE A FROM B

Fig. 10

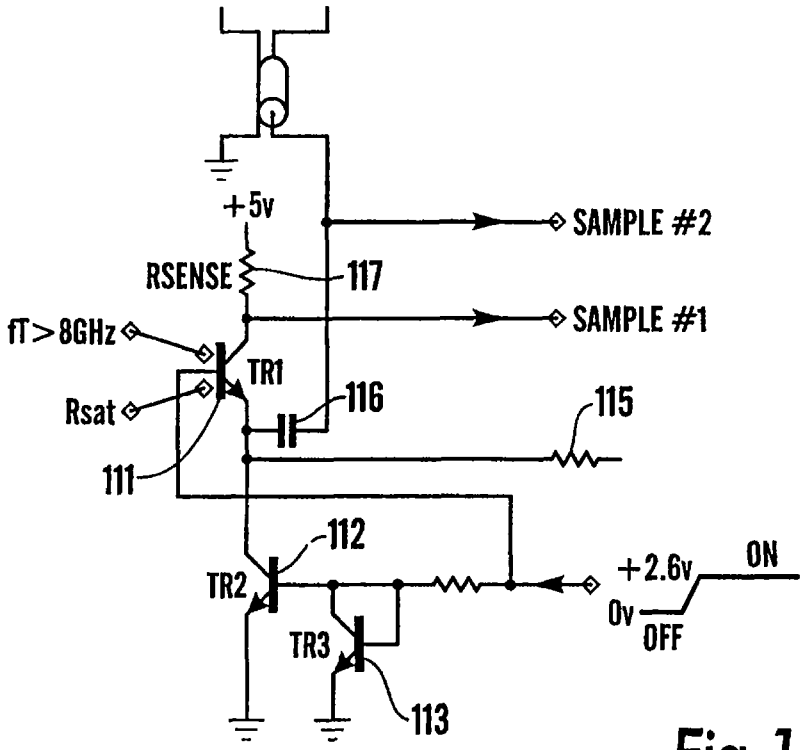

+5v
SAMPLE #2
RSENSE
117
SAMPLE #1
fT>8GHz
TR1
Rsat
116
115
111
112
TR2
+2.6v
ON
0v
OFF
TR3
113

Fig. 11

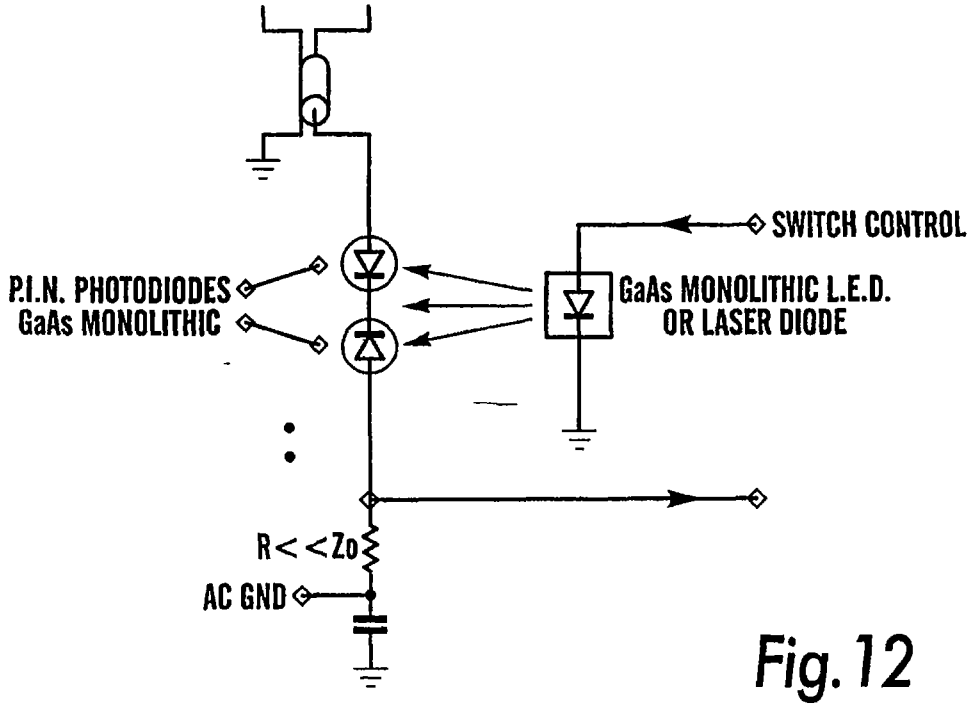

SWITCH CONTROL
P.I.N. PHOTODIODES
GaAs MONOLITHIC
GaAs MONOLITHIC L.E.D.
OR LASER DIODE
R<<Zo
AC GND

Fig. 12

2 2 APR 2002

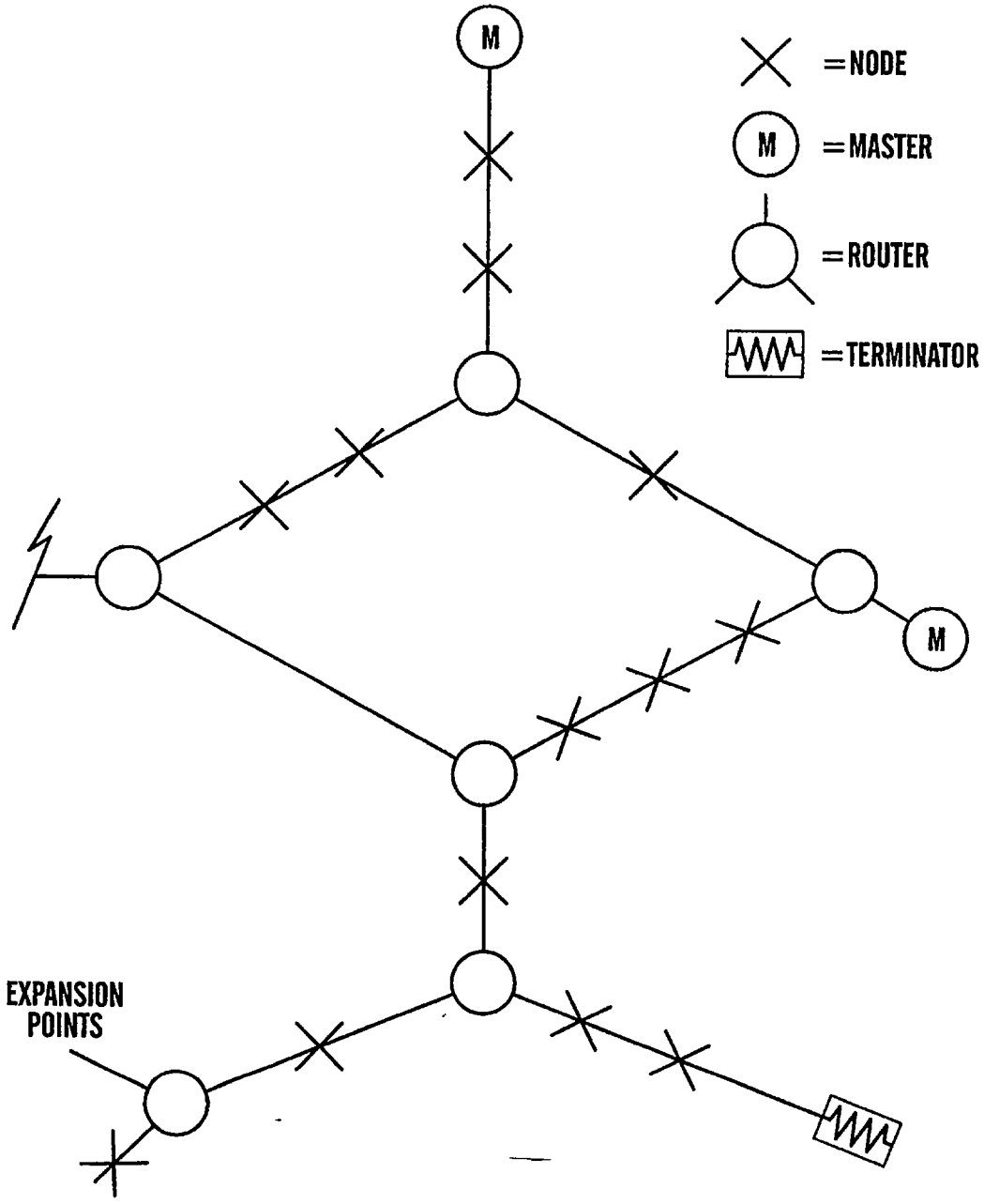


Fig. 13

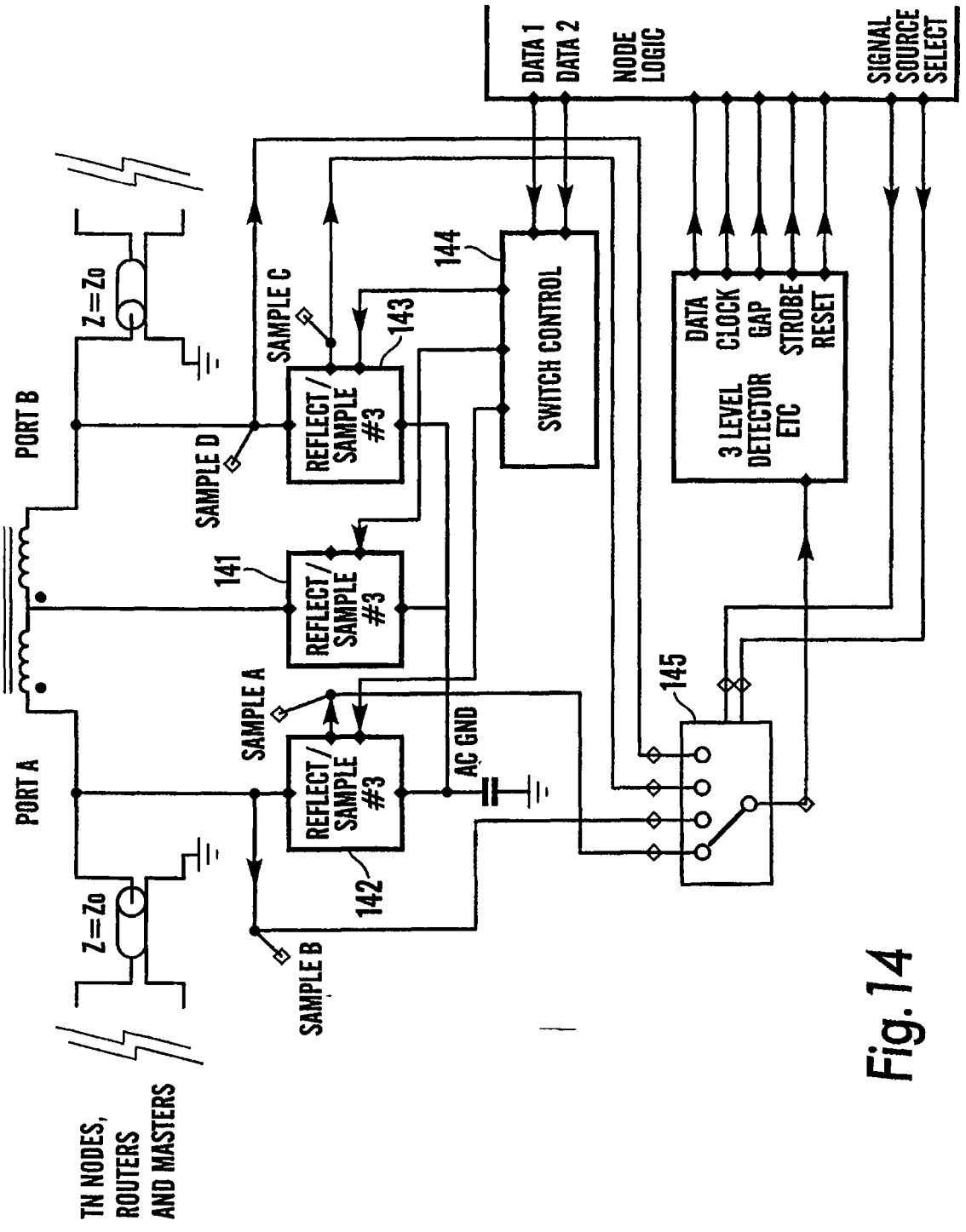

TN NODES, ROUTERS AND MASTERS
Z=Zo
Z=Zo
PORT A
PORT B
SAMPLE A
SAMPLE B
SAMPLE C
SAMPLE D
141
142
143
144
145
REFLECT/ SAMPLE #3
REFLECT/ SAMPLE #3
REFLECT/ SAMPLE #3
AC GND
SWITCH CONTROL
3 LEVEL DETECTOR ETC
DATA
CLOCK
GAP
STROBE
RESET
DATA 1
DATA 2
NODE LOGIC
SIGNAL SOURCE SELECT

Fig. 14

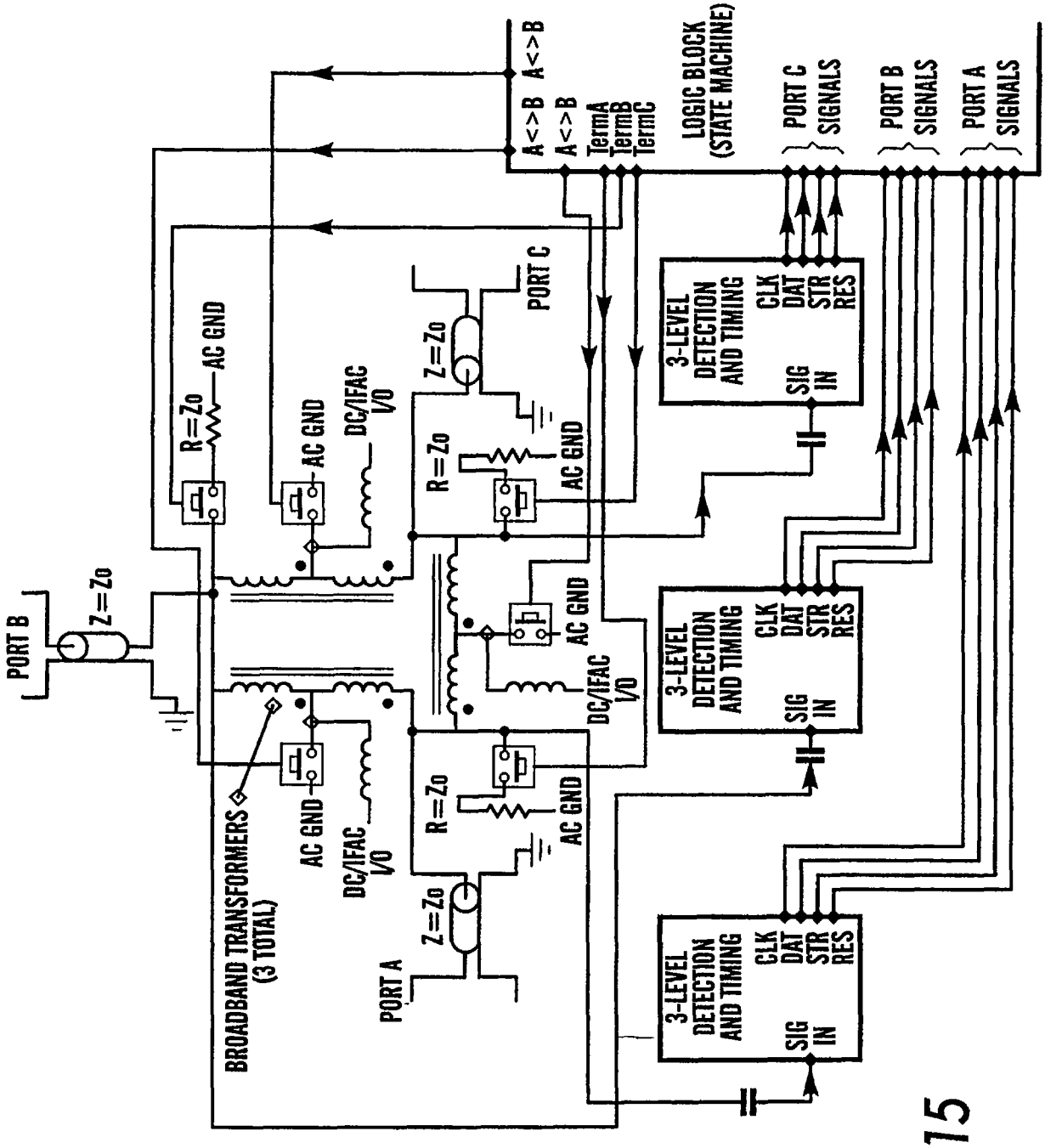

A<>B
A<>B
TermA
TermB
TermC
LOGIC BLOCK (STATE MACHINE)
PORT C SIGNALS
PORT B SIGNALS
PORT A SIGNALS
3-LEVEL DETECTION AND TIMING
CLK
DAT
STR
RES
SIG IN
PORT C
PORT B
PORT A
Z=Zo
R=Zo
AC GND
DC/IFAC I/O
BROADBAND TRANSFORMERS (3 TOTAL)

Fig. 15

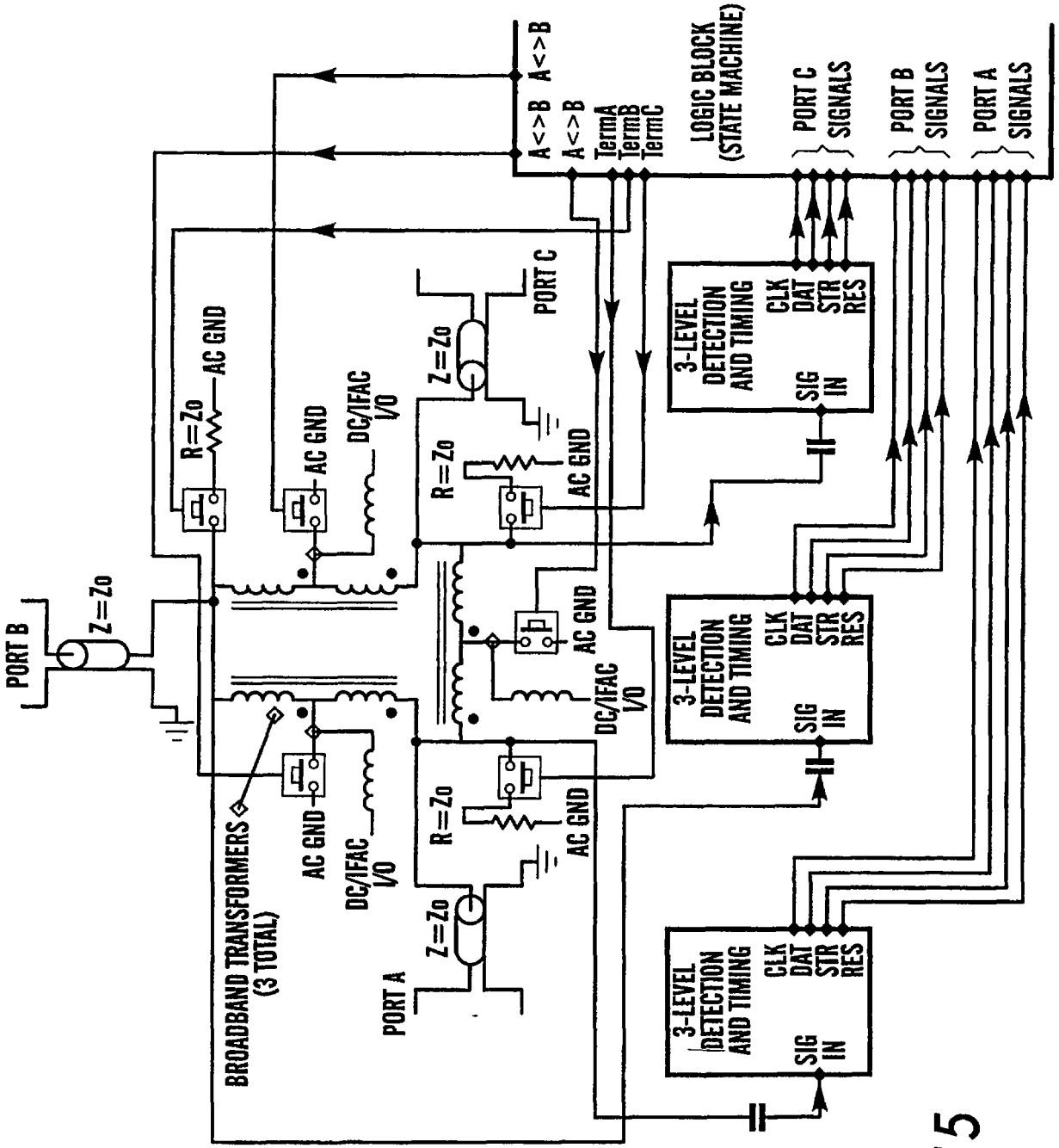

A<>B
A<>B
TermA
TermB
TermC
LOGIC BLOCK (STATE MACHINE)
PORT C SIGNALS
PORT B SIGNALS
PORT A SIGNALS
3-LEVEL DETECTION AND TIMING
CLK
DAT
STR
RES
SIG IN
PORT C
PORT B
PORT A
Z=Zo
R=Zo
AC GND
DC/IFAC I/O
BROADBAND TRANSFORMERS (3 TOTAL)

Fig. 15

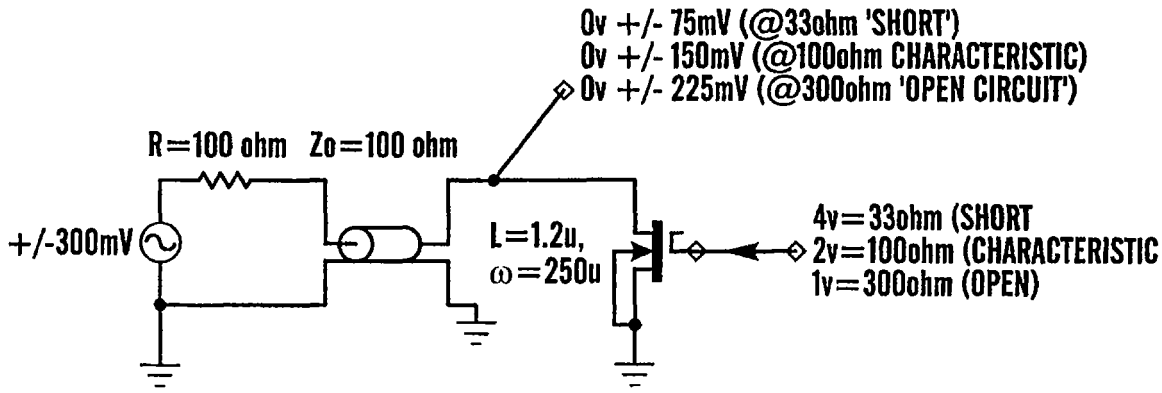


Fig. 15A

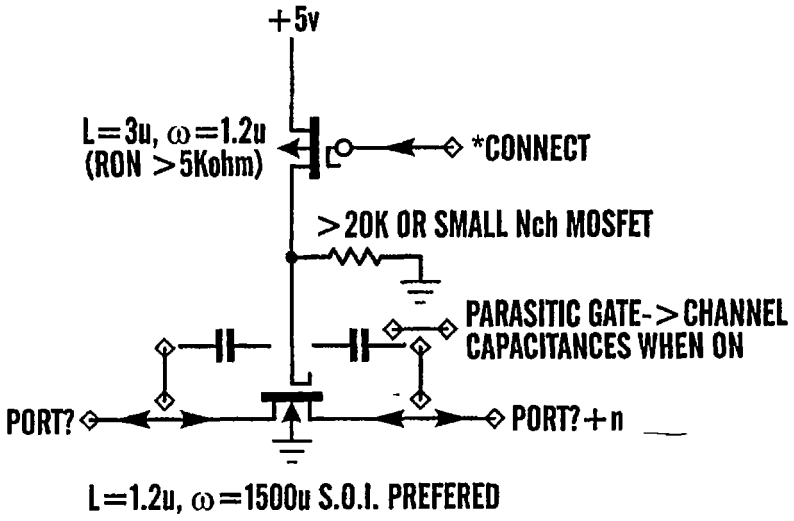


Fig. 15B

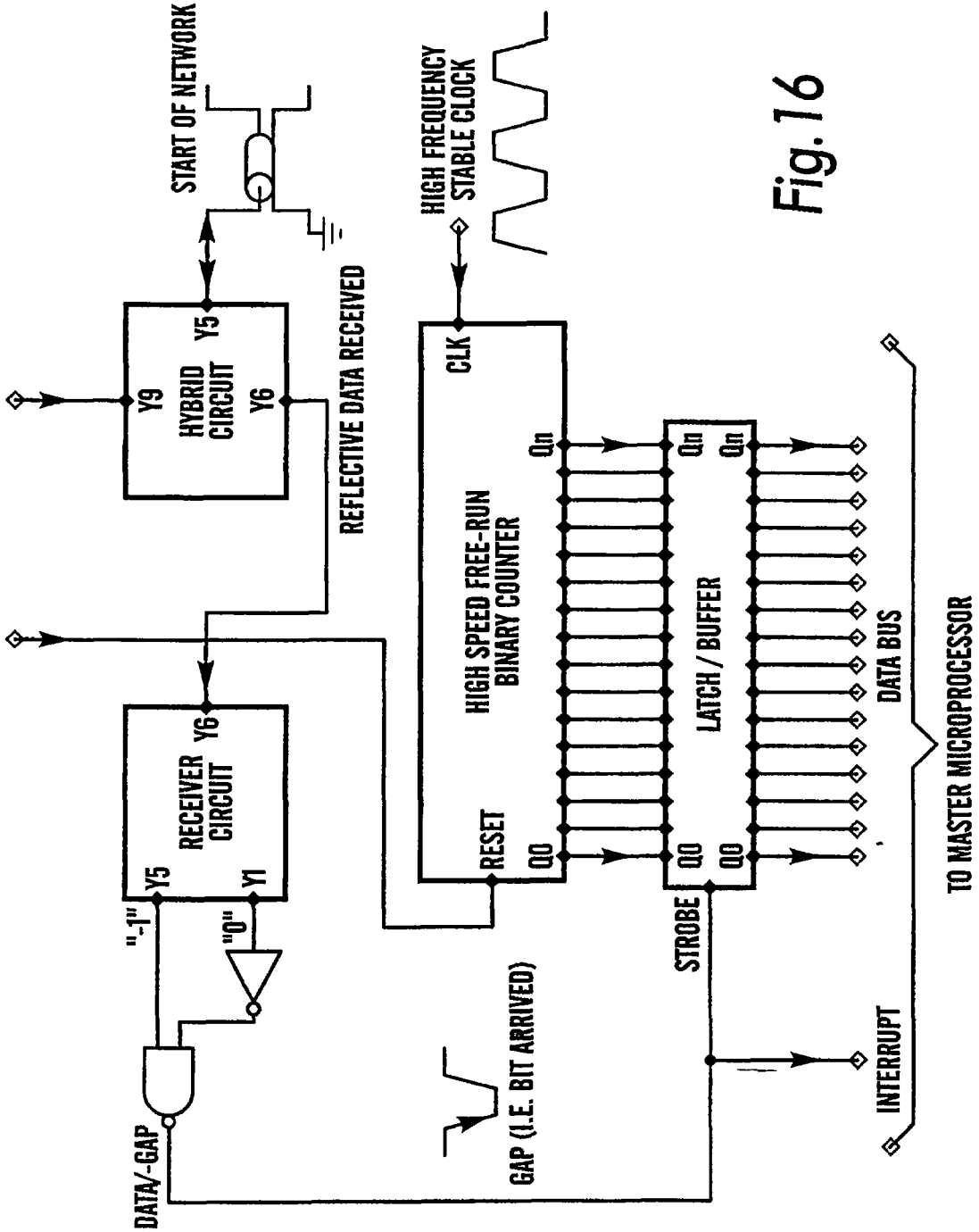
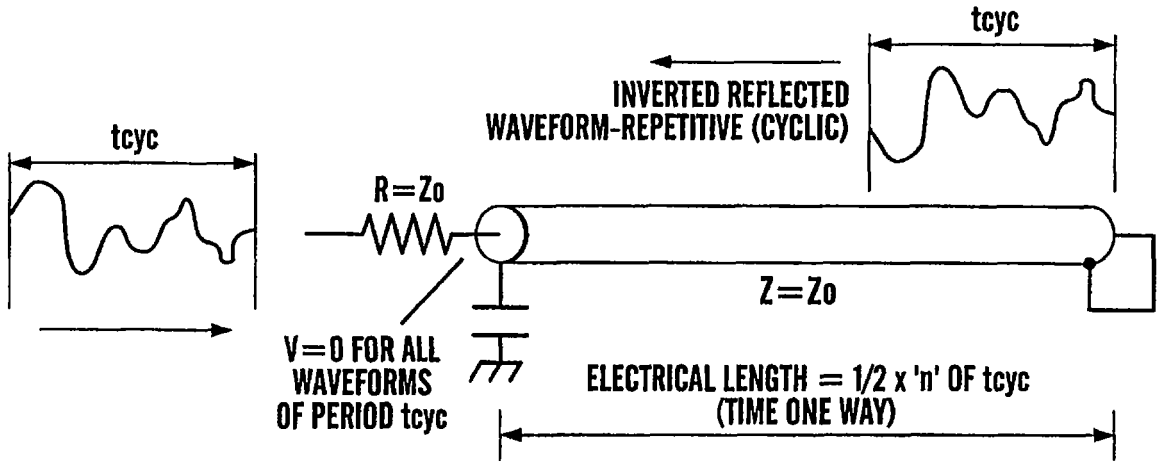

START OF NETWORK
HIGH FREQUENCY STABLE CLOCK
Y9
HYBRID CIRCUIT
Y5
Y6
REFLECTIVE DATA RECEIVED
CLK
Qn
HIGH SPEED FREE-RUN BINARY COUNTER
RESET
Q0
LATCH / BUFFER
STROBE
DATA BUS
TO MASTER MICROPROCESSOR
RECEIVER CIRCUIT
"-1"
"0"
DATA/-GAP
GAP (I.E. BIT ARRIVED)
INTERRUPT

Fig. 16



MEMORY EFFECT ON WANTED SIGNALS WHEN THEN COMBINED AT THE COAX ENTRANCE
(SPURIOUS SIGNALS HAVING BEEN MOVED)



Fig. 17

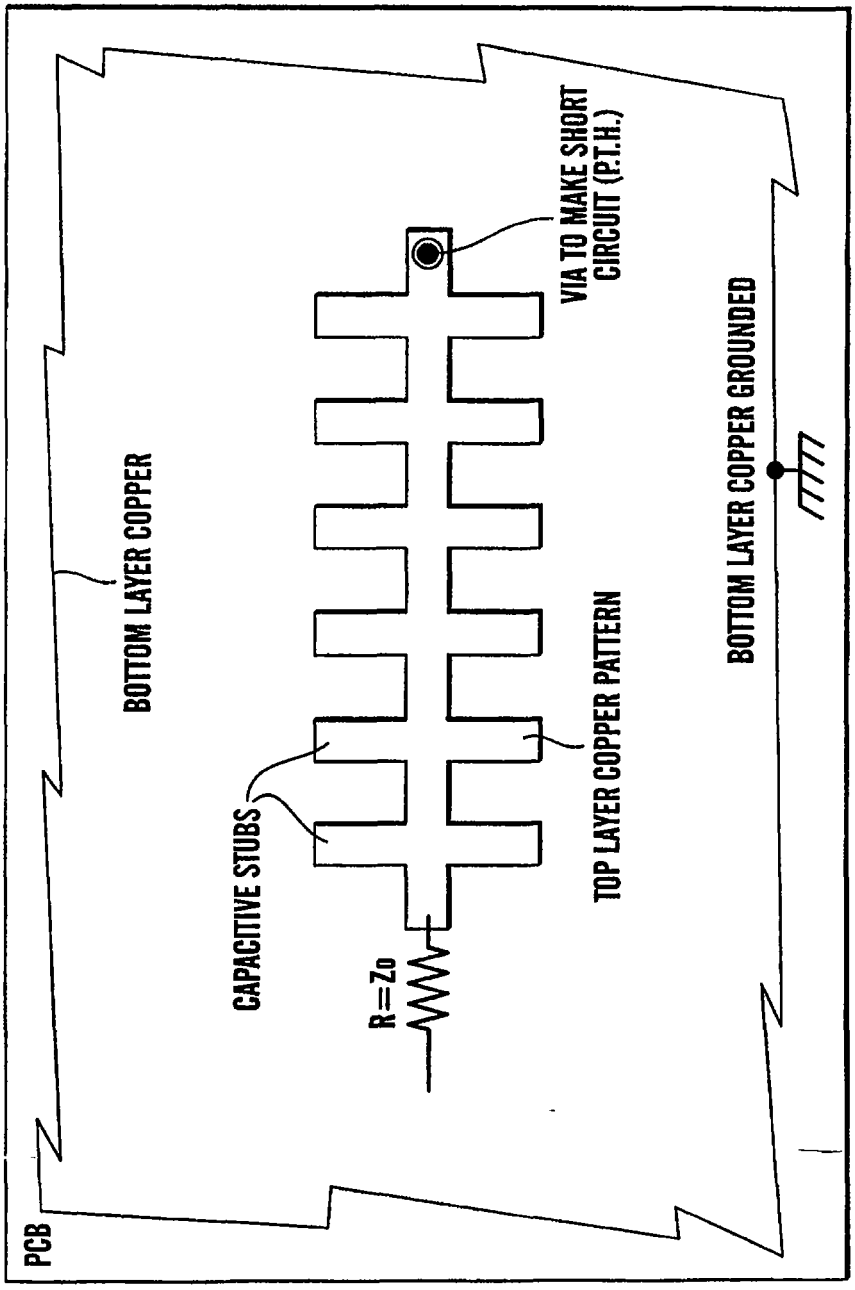

PCB
BOTTOM LAYER COPPER
CAPACITIVE STUBS
R=Z0
TOP LAYER COPPER PATTERN
VIA TO MAKE SHORT CIRCUIT (P.T.H.)
BOTTOM LAYER COPPER GROUNDED

Fig. 18