CLAIMS

1. An exclusive-or logic circuit, comprising:

a first input node;

a second input node;

an output node;

a pass gate connected to be controlled by a logic state present at the second input node, the pass gate connected to pass through a version of a logic state present at the first input node to the output node when controlled to transmit by the logic state present at the second input node;

a transmission gate connected to be controlled by the logic state present at the first input node, the transmission gate connected to pass through a version of the logic state present at the second input node to the output node when controlled to transmit by the logic state present at the first input node; and

pullup logic connected to be controlled by both the logic state present at the first input node and the logic state present at the second input node, the pullup logic connected to drive a state present at the output node low when both the logic state present at the first input node and the logic state present at the second input node are high.

2. The exclusive-or logic circuit as recited in claim 1, further comprising:

a first input inverter having an input connected to the first input node and an output connected to the pass gate;

a second input inverter having an input connected to the second input node and an output connected to the transmission gate; and

an output inverter having an input connected to each of the pass gate, transmission gate, and the pullup logic, the output inverter also having an output connected to the output node.

3. The exclusive-or logic circuit as recited in claim 2, wherein the pass gate is defined as an NMOS transistor having a gate connected to the output of the second input inverter such that an inverted version of the logic state present at the second input node is received at the gate of the NMOS transistor, and

wherein the NMOS transistor has a first terminal connected to the output of the first input inverter and a second terminal connected to the input of the output inverter.

4. The exclusive-or logic circuit as recited in claim 3, wherein the NMOS transistor is connected to transmit when the logic state at the second input node is low, such that the logic state at the output node is made to match the logic state at the first input node.

5. The exclusive-or logic circuit as recited in claim 2, wherein the transmission gate is defined by an NMOS transistor and a PMOS transistor which each has a respective first terminal connected to the output of the second input inverter, and which each has a respective second terminal connected to the input of the output inverter, and

wherein the PMOS transistor has a gate connected to the first input node, and wherein the NMOS transistor has a gate connected to the output of the first input inverter.

6. The exclusive-or logic circuit as recited in claim 5, wherein both the PMOS and NMOS transistors are connected to transmit when the logic state at the first input node is low, such that the logic state at the output node is made to match the logic state at the second input node.

7. The exclusive-or logic circuit as recited in claim 2, wherein the pullup logic is defined by a first PMOS transistor and a second PMOS transistor, wherein the first and second PMOS transistors are serially connected between a power supply and the input of the output inverter.

8. The exclusive-or logic circuit as recited in claim 7, wherein a gate of the first PMOS transistor is connected to the output of the second input inverter, and wherein a gate of the second PMOS transistor is connected to the output of the first input inverter.

9. The exclusive-or logic circuit as recited in claim 7, wherein a gate of the first PMOS transistor is connected to the output of the first input inverter, and wherein a gate of the second PMOS transistor is connected to the output of the second input inverter.

10. The exclusive-or logic circuit as recited in claim 7, wherein both the first and second PMOS transistors are connected to transmit when the logic states at the first and second input nodes are both high, such that the logic state at the output node is driven low.

11. The exclusive-or logic circuit as recited in claim 1, wherein the exclusive-or logic circuit is defined within a semiconductor chip.

12. An exclusive-or logic circuit layout, comprising:

six PMOS transistors; and

five NMOS transistors,

wherein the five NMOS transistors are respectively paired with five of the six PMOS transistors such that each pair of NMOS and PMOS transistors is defined to share a contiguous gate electrode structure placed along a respective one of five gate electrode tracks,

wherein a sixth of the six PMOS transistors is defined by a gate electrode structure placed along a sixth gate electrode track, such that the sixth PMOS transistor does not share the sixth gate electrode track with another transistor within the exclusive-or logic circuit layout, and

wherein the six gate electrode tracks are oriented parallel to each other.

13. The exclusive-or logic circuit layout as recited in claim 12, wherein the exclusive-or logic circuit layout is devoid of co-linearly placed gate electrodes having and end-to-end spacing therebetween.

14. The exclusive-or logic circuit layout as recited in claim 12, wherein each gate electrode structure is defined an a linear structure having a substantially rectangular cross-section when viewed in an as-drawn state.

15. The exclusive-or logic circuit layout as recited in claim 12, wherein the six gate electrode tracks are equally spaced apart.

16. The exclusive-or logic circuit layout as recited in claim 12, wherein the exclusive-or logic circuit layout is recorded in a digital format on a computer readable medium.

17. The exclusive-or logic circuit layout as recited in claim 16, wherein the digital format is a data file format for storing and communicating one or more semiconductor device layouts.

18. The exclusive-or logic circuit layout as recited in claim 16, wherein the computer readable medium includes program instructions for accessing and retrieving the exclusive-or logic circuit layout in the digital format from the computer readable medium.

19. The exclusive-or logic circuit layout as recited in claim 18, wherein the program instructions for accessing and retrieving include program instructions for selecting a library, a cell, or both library and cell including the exclusive-or logic circuit layout in the digital format.

20. An exclusive-nor logic circuit, comprising:

a first input node;

a second input node;

an output node;

a pass gate connected to be controlled by a logic state present at the second input node, the pass gate connected to pass through a version of a logic state present at the first input node to the output node when controlled to transmit by the logic state present at the second input node;

a transmission gate connected to be controlled by the logic state present at the first input node, the transmission gate connected to pass through a version of the logic state present at the second input node to the output node when controlled to transmit by the logic state present at the first input node; and

pulldown logic connected to be controlled by both the logic state present at the first input node and the logic state present at the second input node, the pulldown logic connected to drive a state present at the output node high when both the logic state present at the first input node and the logic state present at the second input node are low.

21. The exclusive-nor logic circuit as recited in claim 20, further comprising:

a first input inverter having an input connected to the first input node and an output connected to the pass gate;

a second input inverter having an input connected to the second input node and an output connected to the transmission gate; and

an output inverter having an input connected to each of the pass gate, transmission gate, and the pulldown logic, the output inverter also having an output connected to the output node.

22. The exclusive-nor logic circuit as recited in claim 21, wherein the pass gate is defined as a PMOS transistor having a gate connected to the output of the second input inverter such that an inverted version of the logic state present at the second input node is received at the gate of the PMOS transistor, and

wherein the PMOS transistor has a first terminal connected to the output of the first input inverter and a second terminal connected to the input of the output inverter.

23. The exclusive-nor logic circuit as recited in claim 22, wherein the PMOS transistor is connected to transmit when the logic state at the second input node is high, such that the logic state at the output node is made to match the logic state at the first input node.

24. The exclusive-nor logic circuit as recited in claim 21, wherein the transmission gate is defined by a PMOS transistor and an NMOS transistor which each has a respective first terminal connected to the output of the second input inverter, and which each has a respective second terminal connected to the input of the output inverter, and

wherein the NMOS transistor has a gate connected to the first input node, and wherein the PMOS transistor has a gate connected to the output of the first input inverter.

25. The exclusive-nor logic circuit as recited in claim 24, wherein both the NMOS and PMOS transistors are connected to transmit when the logic state at the first input node is high, such that the logic state at the output node is made to match the logic state at the second input node.

26. The exclusive-nor logic circuit as recited in claim 21, wherein the pulldown logic is defined by a first NMOS transistor and a second NMOS transistor, wherein the first and second NMOS transistors are serially connected between a reference ground potential and the input of the output inverter.

27. The exclusive-nor logic circuit as recited in claim 26, wherein a gate of the first NMOS transistor is connected to the output of the second input inverter, and wherein a gate of the second NMOS transistor is connected to the output of the first input inverter.

28. The exclusive-nor logic circuit as recited in claim 26, wherein a gate of the first NMOS transistor is connected to the output of the first input inverter, and wherein a gate of the second NMOS transistor is connected to the output of the second input inverter.

29. The exclusive-nor logic circuit as recited in claim 26, wherein both the first and second NMOS transistors are connected to transmit when the logic states at the first and second input nodes are both low, such that the logic state at the output node is driven high.

30. The exclusive-or logic circuit as recited in claim 20, wherein the exclusive-nor logic circuit is defined within a semiconductor chip.

31. An exclusive-nor logic circuit layout, comprising:

five PMOS transistors; and

six NMOS transistors,

wherein the five PMOS transistors are respectively paired with five of the six NMOS transistors such that each pair of PMOS and NMOS transistors is defined to share a contiguous gate electrode structure placed along a respective one of five gate electrode tracks,

wherein a sixth of the six NMOS transistors is defined by a gate electrode structure placed along a sixth gate electrode track, such that the sixth NMOS transistor does not share the sixth gate electrode track with another transistor within the exclusive-nor logic circuit layout, and

wherein the six gate electrode tracks are oriented parallel to each other.

32. The exclusive-nor logic circuit layout as recited in claim 31, wherein the exclusive-nor logic circuit layout is devoid of co-linearly placed gate electrodes having and end-to-end spacing therebetween.

33. The exclusive-nor logic circuit layout as recited in claim 31, wherein each gate electrode structure is defined an a linear structure having a substantially rectangular cross-section when viewed in an as-drawn state.

34. The exclusive-nor logic circuit layout as recited in claim 31, wherein the six gate electrode tracks are equally spaced apart.

35. The exclusive-or logic circuit layout as recited in claim 31, wherein the exclusive-or logic circuit layout is recorded in a digital format on a computer readable medium.

36. The exclusive-or logic circuit layout as recited in claim 35, wherein the digital format is a data file format for storing and communicating one or more semiconductor device layouts.

37. The exclusive-or logic circuit layout as recited in claim 35, wherein the computer readable medium includes program instructions for accessing and retrieving the exclusive-or logic circuit layout in the digital format from the computer readable medium.

38. The exclusive-or logic circuit layout as recited in claim 37, wherein the program instructions for accessing and retrieving include program instructions for selecting a library, a cell, or both library and cell including the exclusive-or logic circuit layout in the digital format.

CLAIMS

1. A circuit, comprising:

a first input node;

a second input node;

a common node;

a pass gate connected to be controlled by a logic state present at the second input node, the pass gate connected to pass through a version of a logic state present at the first input node to the common node when controlled to transmit by the logic state present at the second input node;

a transmission gate connected to be controlled by the logic state present at the first input node, the transmission gate connected to pass through a version of the logic state present at the second input node to the common node when controlled to transmit by the logic state present at the first input node; and

pullup logic connected to be controlled by both the logic state present at the first input node and the logic state present at the second input node, the pullup logic connected to drive a state present at the common node when both the logic state present at the first input node and the logic state present at the second input node are high.

2. The circuit as recited in claim 1, further comprising:

a first input inverter having an input connected to the first input node and an output connected to the pass gate; and

a second input inverter having an input connected to the second input node and an output connected to the transmission gate.

3. The circuit as recited in claim 2, wherein the pass gate is defined as an NMOS transistor having a gate connected to the output of the second input inverter such that an inverted version of the logic state present at the second input node is received at the gate of the NMOS transistor, and

wherein the NMOS transistor has a first terminal connected to the output of the first input inverter and a second terminal connected to the common node.

4. The circuit as recited in claim 3, wherein the NMOS transistor is connected to transmit when the logic state at the second input node is low, such that the logic state at the common node is opposite the logic state at the first input node.

5. The circuit as recited in claim 2, wherein the transmission gate is defined by an NMOS transistor and a PMOS transistor which each has a respective first terminal connected to the output of the second input inverter, and which each has a respective second terminal connected to the common node, and

wherein the PMOS transistor has a gate connected to the first input node, and wherein the NMOS transistor has a gate connected to the output of the first input inverter.

6. The circuit as recited in claim 5, wherein both the PMOS and NMOS transistors are connected to transmit when the logic state at the first input node is low, such that the logic state at the common node is opposite the logic state at the second input node.

7. The circuit as recited in claim 2, wherein the pullup logic is defined by a first PMOS transistor and a second PMOS transistor, wherein the first and second PMOS transistors are serially connected between a power supply and the common node.

8. The circuit as recited in claim 7, wherein a gate of the first PMOS transistor is connected to the output of the second input inverter, and wherein a gate of the second PMOS transistor is connected to the output of the first input inverter.

9. The circuit as recited in claim 7, wherein a gate of the first PMOS transistor is connected to the output of the first input inverter, and wherein a gate of the second PMOS transistor is connected to the output of the second input inverter.

10. The circuit as recited in claim 7, wherein both the first and second PMOS transistors are connected to transmit when the logic states at the first and second input nodes are both high, such that the logic state at the common node is driven high.

11. The circuit as recited in claim 1, wherein the circuit is defined within a semiconductor chip.

12. An exclusive-or logic circuit layout, comprising:

six PMOS transistors; and

five NMOS transistors,

wherein the five NMOS transistors are respectively paired with five of the six PMOS transistors such that each pair of NMOS and PMOS transistors is defined to share a contiguous gate electrode structure placed along a respective one of five gate electrode tracks,

wherein a sixth of the six PMOS transistors is defined by a gate electrode structure placed along a sixth gate electrode track, such that the sixth PMOS transistor does not share the sixth gate electrode track with another transistor within the exclusive-or logic circuit layout, and

wherein the six gate electrode tracks are oriented parallel to each other.

13. The exclusive-or logic circuit layout as recited in claim 12, wherein the exclusive-or logic circuit layout is devoid of co-linearly placed gate electrodes having an end-to-end spacing therebetween.

14. The exclusive-or logic circuit layout as recited in claim 12, wherein each gate electrode structure is defined as a linear structure having a substantially rectangular cross-section when viewed in an as-drawn state.

15. The exclusive-or logic circuit layout as recited in claim 12, wherein the six gate electrode tracks are equally spaced apart.

16. The exclusive-or logic circuit layout as recited in claim 12, wherein the exclusive-or logic circuit layout is recorded in a digital format on a computer readable medium.

17. The exclusive-or logic circuit layout as recited in claim 16, wherein the digital format is a data file format for storing and communicating one or more semiconductor device layouts.

18. The exclusive-or logic circuit layout as recited in claim 16, wherein the computer readable medium includes program instructions for accessing and retrieving the exclusive-or logic circuit layout in the digital format from the computer readable medium.

19. The exclusive-or logic circuit layout as recited in claim 18, wherein the program instructions for accessing and retrieving include program instructions for selecting a library, a cell, or both library and cell including the exclusive-or logic circuit layout in the digital format.

20. The circuit as recited in claim 1, further comprising:

an output inverter having an input connected to the common node, the output inverter also having an output connected to an output node of the circuit.

21. A circuit, comprising:

five PMOS transistors; and

four NMOS transistors,

wherein the four NMOS transistors are respectively paired with four of the five PMOS transistors such that each of the four pairs of NMOS and PMOS transistors is formed from a different one of four contiguous gate electrode structures,

wherein a fifth of the five PMOS transistors is formed from a first single-transistor gate electrode structure that forms only one transistor device,

wherein each of the four contiguous gate electrode structures and the first single-transistor gate electrode structure are oriented parallel to each other,

wherein a first of the four NMOS transistors and a first of the five PMOS transistors forms a first pair of the four pairs of NMOS and PMOS transistors and forms a first input inverter of the circuit, and

wherein a second of the four NMOS transistors and a second of the five PMOS transistors forms a second pair of the four pairs of NMOS and PMOS transistors and forms a second input inverter of the circuit.

22. The circuit as recited in claim 21, wherein the circuit is devoid of co-linearly placed gate electrode structures having and end-to-end spacing therebetween.

23. The circuit as recited in claim 21, wherein each of the four contiguous gate electrode structures and the first single-transistor gate electrode structure is defined as a respective linear-shaped structure.

24. The circuit as recited in claim 21, wherein each of the four contiguous gate electrode structures and the first single-transistor gate electrode structure is placed in accordance with a fixed centerline pitch.

25. The circuit as recited in claim 21, wherein the circuit is defined as part of an exclusive-or logic function circuit.

26. The circuit as recited in claim 21, wherein a third NMOS transistor of the four NMOS transistors and a third PMOS transistor of the five PMOS transistors forms a transmission gate connected to the second input inverter.

27. The circuit as recited in claim 26, wherein a fourth NMOS transistor of the four NMOS transistors forms a pass gate connected to the first input inverter.

28. The circuit as recited in claim 27, wherein a fourth PMOS transistor of the five PMOS transistors and a fifth PMOS transistor of the five PMOS transistors forms pullup logic connected to outputs of both the pass gate and the transmission gate.

29. The circuit as recited in claim 28, further comprising:

a sixth PMOS transistor; and

a fifth NMOS transistor,

wherein both the sixth PMOS transistor and fifth NMOS transistor are formed by a fifth contiguous gate electrode structure.

30. The circuit as recited in claim 29, wherein the fifth contiguous gate electrode structure is oriented parallel to each of the four contiguous gate electrode structures and the first single-transistor gate electrode structure.

31. The circuit as recited in claim 29, wherein the sixth PMOS transistor and the fifth NMOS transistor form an output inverter having an input connected to outputs of each of the transmission gate, the pass gate, and the pullup logic.