SEMICONDUCTOR STRUCTURE ON AN EXTREMELY ROUGH SUBSTRATE

Field of the invention and prior art

The invention relates to the field of substrates or structures for producing electronic components, and to methods of producing said substrates or structures.

It also relates to techniques for assembling layers or substrates on rough layers or rough substrates.

It is applicable to semiconductor structures, in particular silicon on insulator (SOI) type structures.

As illustrated in Figure 1, said structures comprise a layer 4 of silicon in which the components proper are located, and beneath which a buried oxide layer 2 is formed. This oxide layer constitutes insulation from stray currents and charges deriving from ionized particles. It also provides good insulation between neighboring components formed in the same silicon layer, and in particular it substantially reduces stray capacitance between said neighboring components. The silicon layer resides on a silicon substrate 6 which acts as a mechanical support.

Typically, the superficial silicon layer 4 is about 10 nanometers (nm) to 1000 nm thick, while the oxide layer 2 is of the order of several hundred nanometers thick, for example 400 nm.

That type of structure can be obtained by a "SIMOX" type process or by a "wafer bonding" technique that relies on molecular bonding.

After producing an assembly such as that shown in Figure 1, electronic components can be produced in the superficial silicon layer 4. It thus constitutes the active layer; the oxide layer 2 is an insulation layer; the substrate 6 acts as a mechanical support and allows the assembly to be processed.

Proper operation of a component produced in layer 4 is linked to various parameters, one of which is heating,

which can substantially limit the performance of the component.

Thus, there is a problem with finding a semiconductor on insulator type structure, and a method of producing such a structure, in which the performance of the components subsequently produced in the layer of semiconductor is not limited by heating, or is less limited by heating than in known structures.

In another aspect of the invention, known techniques for assembling materials do not allow bonding of substrates or layers which have roughness of more than a certain limiting value of the order of 0.5 nm root mean square (rms), or which are difficult to polish, or which have chemistry which is not conducive to bonding by molecular bonding.

Thus, there is an occasional need to bond materials each having roughness above said limiting value, or at least one of which is difficult to polish or has chemistry that is not conducive to bonding by molecular bonding, or to bond such a material with a layer or substrate of a material that may itself be compatible with direct bonding or molecular bonding.

Description of the invention

In a first aspect, the invention provides a semiconductor structure, comprising:

- a substrate or a base layer on a substrate, said substrate or said base layer having a surface with roughness of more than 0.5 nm rms, or having chemistry that is incompatible with molecular bonding;
- a layer of material selected from semiconductor materials;
- a layer termed the bonding layer located between the substrate or base layer and the layer of semiconductor material.

Said layer of semiconductor material and the bonding layer can be bonded by molecular bonding even if the substrate or the base layer formed over it has roughness that is above the accepted limiting roughness for molecular bonding (which is about 0.5 nm rms) or if said substrate or base layer formed over it is difficult to polish or has chemistry that is incompatible with bonding by molecular bonding.

Thus, it is possible to use a substrate or a base layer formed from a material such as diamond or aluminum nitride (AlN), for example, which is chemically inert, very difficult to polish and which, even after mechanical and chemical treatment, has roughness that is much higher than the accepted limit for bonding by molecular bonding.

Further, said materials have high thermal conductivity of more than 1 watts per centimeter per kelvin (W/cm/K) or 10 W/cm/K.

Components can thus be produced in the layer of semiconductor material, in particular power components, high power components or radiofrequency (RF) type components, since the heat released can be evacuated by the substrate, which acts as a heat sink.

Preferably, the surface of the bonding layer facing the semiconductor material is located at a distance of at most 10 nm from the maximum peaks or bumps on the surface of the substrate or the base layer, which optimizes exploitation of the heat transfer properties of the upper layer of silicon towards the substrate.

An intermediate layer can also be provided between the substrate and the bonding layer. Such an intermediate layer has a thermal conductivity coefficient that is in the range from that of the bonding layer to that of the substrate or the base layer or is higher than that of the substrate or the base layer.

Said intermediate layer is formed from silicon nitride, for example.

A structure in accordance with the invention, as defined above, is compatible with molecular bonding of the layer of semiconductor material to the bonding layer.

The invention also provides a method of producing a semiconductor structure on a substrate or on a base layer on a substrate, said substrate or said base layer being difficult to polish or having roughness of more than 0.5 nm rms, or having chemistry that is incompatible with molecular bonding, said method comprising the following steps:

- forming a layer termed the bonding layer directly on the substrate or base layer or on an intermediate layer with a thermal conductivity coefficient that is in the range from that of the bonding layer to that of the substrate or base layer or is higher than that of the substrate or the base layer;
- smoothing said bonding layer;
- bonding a layer or substrate formed from a semiconductor material to the bonding layer by molecular bonding.

The structure of the invention is an SOI structure, for example, the semiconductor material being silicon, and the bonding layer being a layer of silicon dioxide.

The invention also provides a method of joining or assembling two substrates or layers each with roughness of more than 0.5 nm rms, or being difficult to polish or having chemistry that is incompatible with molecular bonding, said method comprising:

- forming a layer termed the bonding layer directly on the first substrate on each layer to be assembled;
- bonding said bonding layers together by molecular bonding.

The invention also concerns a method of joining or assembling two substrates or layers with one of which has roughness of more than 0.5 nm rms or is difficult to

polish, or which has chemistry that is incompatible with molecular bonding, and the other having roughness of less than 0.5 nm rms or is easy to polish or has chemistry that is compatible with molecular bonding, said method comprising:

- forming a layer termed the bonding layer directly on the substrate or layer having roughness of more than 0.5 nm rms or which is difficult to polish or which has chemistry that is incompatible with molecular bonding;
- bonding said bonding layers to the substrate or layer having roughness of less than 0.5 nm rms or which is easy to polish or which has chemistry that is compatible with molecular bonding, by molecular bonding.

Brief description of the figures

- Figure 1 shows a known SOI structure;
- Figures 2 to 4 show various structures in accordance with the invention;
- Figures 5A to 5D show various steps in a method of producing a structure of the invention;
- Figures 6 and 7 show other structures in accordance with the invention.

Detailed description of embodiments

Figure 2 shows a first example of a structure in accordance with the invention.

In this figure, reference 10 designates a substrate (preferably formed from an electrically insulating material), reference 14 designates a layer or substrate formed from a material selected from semiconductors, for example silicon or germanium (Ge) or gallium arsenide (GaAs) or silicon-germanium (SiGe) or III-V semiconductor components or II-VI semiconductor components, and reference 12 designates a bonding layer located between the substrate 10 and the layer or substrate 14.

The substrate 10 is a substrate with a rough surface 15, or has roughness of more than 0.4 nm rms or 0.5 nm rms. It can also be a surface with chemistry that does not accept molecular bonding or with chemical properties that are incompatible with molecular bonding. Said substrate can, for example, be in the range 100 micrometers (μm) to 2 millimeters (mm) thick.

In principle, bonding by molecular bonding cannot be carried out, or is very difficult to carry out, on a substrate or a surface with such roughness (see in particular Q.Y. Tong and U. Gösele, Semiconductor Molecular bonding: Science and Technology, Wiley-Interscience, p 86, 1999).

The substrate 10 can also be formed from a material that is difficult to polish, i.e., roughness of less than 0.4 nm rms or 0.5 nm rms can only be obtained after polishing for a very long period: in practice, then, such a material can never be used with roughness of less than 0.4 nm rms or 0.5 nm rms.

The mechanical strength of an assembly comprising, for example, such a substrate and a layer or substrate formed from a semiconductor material, assembled by molecular bonding, can be measured by means of the bonding wave, for example by infrared transmission through silicon, or by transparency in the case of transparent materials, or by acoustic microscopy in the presence of metallic layers. It can also be determined by measuring the bonding energy using the blade technique (described by W.P. Maszara et al., J Appl Phys Vol 64, p 4943, 1988, for example): at ambient temperature and in the hydrophilic case, said energy is greater than 60 millijoules per square meter (mJ/m^2), for example greater than 70 mJ/m^2 or 100 mJ/m^2, if bonding is effective.

Thus, the achievement or otherwise of bonding by molecular bonding can be determined by measuring the mechanical strength.

Diamond or aluminum nitride (AlN) are examples of materials that can be used for the substrate 10: their roughness is well above the value of 0.5 nm rms; the roughness of diamond is in the range 30 nm rms to 100 nm rms; that of aluminum nitride is of the order of 1 nm rms, or in the range 0.5 nm rms to 10 nm rms.

Said materials are chemically inert, in particular when using products such as "caro" (a mixture based on sulfuric acid and hydrogen peroxide) and Sc1 (a mixture based on ammonium hydroxide, hydrogen peroxide and water).

Preferably, the substrate 10 is formed from a material with a high thermal conductivity, for example more than 1 W/cm/K, as is the case for diamond or aluminum nitride AlN (3.2 W/cm/K).

A layer or base layer, itself on a substrate, can also be used in place of the substrate 10. It can then have a thickness of several tens of nm, for example in the range 50 nm to 300 nm. The material for said layer has the same properties as those described above in the case of a substrate alone: this material is difficult to polish, or has roughness of more than 0.4 nm rms or 0.5 nm rms, or has a surface with chemistry that is incompatible with or which will not accept molecular bonding, or wherein the chemical properties are incompatible with molecular bonding.

As an example, diamond or aluminum nitride can either be in the form of the substrate or in the form of a layer on a substrate, which substrate is formed from silicon, for example. The diamond or aluminum nitride can be deposited by a CVD type technique.

The expression "substrate" will hereinafter designate these two alternatives.

The layer 12 is termed the bonding layer, and after mechanical and chemical treatment, or polishing, has roughness that is less than 5 nm rms. This enables the material of the substrate 10 to be bonded with the layer

or the substrate 14 formed form a semiconductor material. The substrate layer 14 is preferably connected to the bonding layer 12 by molecular bonding.

In one example, the layer 12 is formed from silicon dioxide. It can also be formed from a material of the "high K coefficient" type such as those described in the MRS Bulletin, March 2002, vol 27, n° 3 "Alternative Gate Dielectrics for Microelectronics": examples of such materials are hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), and yttrium oxide (Y_2O_3).

A further embodiment is shown in Figure 3, having references which are identical to those of Figure 2 when designating identical or corresponding elements. The structure shown in this figure includes a further layer 16 intermediate between the bonding layer and the substrate 10. The thermal conductivity coefficient of this intermediate layer is in the range from that of the bonding layer to that of the substrate or is higher than that of the substrate.

As an example, for a bonding layer formed from silicon dioxide (SiO_2), with a thermal conductivity coefficient of 0.01 W/cm/K, and for a diamond substrate with thermal conductivity of 20 W/cm/K, an intermediate layer of silicon nitride (Si_3N_4) is sufficient, as this material has a thermal conductivity coefficient of 0.3 W/cm/K.

With a layer 12 formed from a high K coefficient type material, silicon nitride Si_3N_4 can also be used as the intermediate layer.

Preferably, the material of the layer 16 is far more resistant or selective than that of the layer 12 as regards physico-chemical treatments or as regards polishing such as mechanical and chemical polishing. However, for the material of the layer 16, it is preferable to select a material with properties as regards bonding by molecular bonding that are similar to

those of the material of the layer 12, whether for hydrophilic or hydrophobic molecular bonding.

Figure 4A shows a structure similar to that of Figure 3, but the roughness in the upper surface of the substrate 30 has been exaggerated.

The bonding layer 22 has been polished to skim the upper peaks 32, 36 of the surface of the substrate 30. These peaks create heat conduction channels which will encourage heat transfer between the silicon layer 24 and the substrate 30.

In a variation, shown in Figure 4B, the surface 25 of the bonding layer 22 is located at a maximum of 10 nm from the maximum peaks or bumps of the substrate to optimize heat transfer by the peaks or bumps then by the substrate.

Such a thickness or distance can be measured at any time, for example by ellipsometry, even while the bonding layer is being prepared.

Thus, the roughness of the substrate is exploited so as to encourage heat transfer between the upper layers of the structure, which contain electronic components, and the base of the substrate.

In the case of diamond, heat transfer between the upper layer of silicon and the diamond substrate is improved by a factor of about 60.

The result is that the function of components formed in the layer 24 is improved. Such components can thus be power components, which release a large amount of heat energy such as insulated gate bipolar transistors (IGBTs) and/or metal oxide on silicon field effect transistors (MOSFETs) and/or RF components (for high speed operation).

Typically, after polishing, the thickness of the bonding layer 12, 22 is in the range 5 nm to 50 nm, for example, and the thickness of the intermediate layer 16, 26 is in the range 5 nm to 20 nm.

A method of producing a component of the invention is described below with reference to Figures 5A to 5D.

Figure 5A shows a substrate 10: its roughness has been greatly exaggerated. Such a substrate has not undergone polishing, or cannot be polished, and has surface roughness or micro-roughness that is greater than the accepted limit for bonding by molecular bonding, for example a surface roughness or micro-roughness in the range 5 nm rms (or 20 or 30 nm rms) to 100 nm rms.

An intermediate layer 26, in this case formed from SI_3N_4, is formed on the substrate.

This layer follows the roughness of the upper surface of the substrate. It is deposited by plasma enhanced chemical vapor deposition (PECVD) or low-pressure CVD (LPCVD), for example.

A bonding layer is subsequently formed, for example a layer of silicon dioxide SiO_2. Preferably, the initial thickness of this layer is over 2.8 to 3 times the value of the surface roughness of the substrate 30, in order to obtain a flat layer after polishing.

As an example, said layer initially has a thickness in the range 0.5 micrometers (μm) to 1 μm, or in the range 0.5 μm to 10 μm.

Said bonding layer then undergoes polishing, for example by mechanical and chemical polishing. Certain processes such as the shallow trench isolation (STI) process (described, for example, in the article by C.P. Chang et al, "A Highly Manufacturable Corner Rounding Solution for 0.18 μm Shallow Trench Isolation", IEDM 97- p 661), have high selectivity between the nitride 26 and the oxide layer 22. Said selectivity enables the layer 22 to be smoothed until the layer 26 is reached, which layer then acts as the stop layer for the smoothing process.

A silicon layer or substrate 24 can then be attached or bonded to the layer 22 by molecular bonding, using

known techniques, for example those described by Tong and Gösele cited above.

It is possible to bond a silicon substrate then to form a thin layer by thinning and polishing the substrate, or to use the "SMART CUT" technique as described, for example, in the article by A.J. Auberton-Hervé et al, "Why can Smart Cut change the future of microelectronics?" published in the Journal of High-Speed Electronics and Systems, vol 10, n° 1 (2002), p 131-146.

In yet another technique, formation of a porous layer of silicon forming a plane of weakness is exploited, for example as described in the article by K. Sataguchi et al., "Eltran by Splitting Porous Si Layers", Proceedings of the 9th International Symposium on Silicon-on-Insulator Tech and Device, 99-3, The Electrochemical Society, Seattle, p 117-121, 1999.

Thus, a structure such as that shown in Figure 5D is obtained, which is similar to that of Figure 4A.

Components can then be produced in the layer 24, in particular power or RF components, and the substrate 10 can eliminate the heat produced by them during their operation.

A further implementation of the invention is shown in Figure 6.

It concerns connecting a substrate 40 or a layer 40 with high roughness (more than 0.4 nm rms or 0.5 nm rms, for example in the range 1 nm rms to 100 nm rms), or which is difficult to polish or has chemistry that is incompatible with bonding by molecular bonding, to a substrate 50 or a layer 50 with the same properties. As an example, the substrate 40 is formed from diamond while the substrate 50 is formed from diamond or AlN (aluminum nitride).

A bonding layer 42, 52 is formed on each substrate as explained above, directly or with an intermediate layer, also as described above. Each of the bonding layers is formed from silicon dioxide, for example. It

is then possible to establish a bond by molecular bonding between said two bonding layers.

This method is advantageous when at least one of the two materials is difficult to polish and is chemically inert, in the sense indicated above.

The foregoing description remains applicable if the layer of silicon or semiconductor material is replaced by a rough substrate-bonding layer assembly.

More generally, as illustrated in Figure 7, the invention also relates to connecting a substrate 40 or a layer 40 that is difficult to polish or has very high roughness, and is in any case more than 0.5 nm rms, for example in the range 1 nm rms to 100 nm rms, or has chemistry that is incompatible with bonding by molecular bonding, to a substrate 60 or a layer 60 with chemistry and roughness that are compatible with bonding by molecular bonding, the roughness being below 0.5 nm rms.

A bonding layer 42 is formed on the substrate 40, directly or with an intermediate layer as explained above. The bonding layer is silicon dioxide, for example. It is then possible to establish a bond by molecular bonding between this bonding layer and the layer or substrate 60.

The foregoing description remains applicable if the layer of silicon or semiconductor material is replaced by the layer or the substrate 60.

In the last two cases, the material of each substrate that is difficult to polish or has roughness of more than 0.5 nm rms or has chemistry that is incompatible with bonding by molecular bonding, can be selected from the materials mentioned above (diamond, aluminum nitride AlN), for example.

CLAIMS

1. A semiconductor structure, comprising:

- a substrate (10, 30) or a base layer, having a surface with roughness of more than 0.5 nm rms or having chemistry that is incompatible with molecular bonding, and having thermal conductivity of more than 1 W/cm/K;
- a layer (14, 24) of material selected from semiconductor materials;
- a layer (12, 22) termed the bonding layer located between the substrate or base layer and the layer of material selected from semiconductor materials.

2. A structure according to claim 1, wherein the substrate or base layer is formed from diamond or aluminum nitride.

3. A structure according to claim 1 or claim 2, further comprising an intermediate layer (16, 26) between the substrate or base layer and the bonding layer, having thermal conductivity in the range between that of the bonding layer and that of the substrate or base layer, or higher than that of the substrate or base layer.

4. A structure according to claim 3, wherein the intermediate layer is silicon nitride.

5. A structure according to any one of claims 1 to 4, wherein the bonding layer (12, 22) and the layer (14, 24) of semiconductor material are bonded by molecular bonding.

6. A structure according to any one of claims 1 to 5, wherein the thickness of the bonding layer is in the range 5 nm to 20 nm.

7. A structure according to any one of claims 1 to 6, wherein the bonding layer is formed from silicon dioxide (SiO_2), silicon nitride (Si_3N_4), hafnium oxide, zirconium oxide, alumina, or yttrium oxide.

8. A structure according to any one of claims 1 to 7, wherein the semiconductor material is silicon, germanium, gallium arsenide, silicon-germanium, or a semiconductor III-V or II-VI compound.

9. A structure according to claim 8, wherein the structure is of the SOI type.

10. A structure according to any one of claims 1 to 9, wherein the surface of the bonding layer facing the semiconductor material is located at a distance of at most 10 nm from the surface or the maximum peaks or bumps of the substrate or base layer.

11. A structure according to any one of claims 1 to 10, wherein at least one power component and/or at least one RF component is formed in the layer of material selected from semiconductor materials.

12. A structure according to any one of claims 1 to 11, comprising at least one IGBT or MOSFET type component in the layer of material selected from semiconductor materials.

13. A structure comprising two substrates or layers (40, 50, 60) wherein the first substrate (40) or first layer has roughness of more than 0.5 nm rms or has chemistry that is incompatible with molecular bonding, and having thermal conductivity of more than 1 W/cm/K said structure comprising a layer (42, 52) termed the bonding layer located between the first substrate (40) or first layer and the second substrate (50, 60) or second layer.

14. A structure according to claim 13, the first substrate or first layer being formed from diamond or aluminum nitride.

15. A structure according to claim 13 or claim 14, wherein the bonding layer is formed from silicon dioxide, silicon nitride, hafnium oxide, zirconium oxide, alumina, or yttrium oxide.

16. A structure according to any one of claims 13 to 15, wherein the second substrate (50) or second layer has roughness of more than 0.5 nm rms, or has chemistry that is incompatible with molecular bonding.

17. A method of producing a semiconductor structure on a substrate (10, 30) or base layer having roughness of more than 0.5 nm rms or having chemistry that is incompatible with molecular bonding, and having thermal conductivity of more than 1 W/cm/K, comprising the following steps:

- forming a layer (12, 22) termed the bonding layer directly on the substrate or base layer or on an intermediate layer (16, 26) with a thermal conductivity coefficient that is in the range from that of the bonding layer to that of the substrate or base layer or is higher than that of the substrate or the base layer;
- smoothing said bonding layer;
- bonding a layer or substrate (14, 24) formed from a semiconductor material to the bonding layer by molecular bonding.

18 method according to claim 17, wherein the substrate or base layer is formed from diamond or aluminum nitride.

19. A method according to claim 17 or claim 18, wherein the intermediate layer is formed from silicon nitride.

20. A method according to any one of claims 17 to 19, wherein the bonding layer is formed from silicon dioxide, silicon nitride, hafnium oxide, zirconium oxide, alumina or yttrium oxide.

21. A method according to any one of claims 17 to 19, wherein prior to smoothing, the thickness of the bonding layer is more than 2.8 times the value of the roughness of the substrate or the base layer.

22. A method according to any one of claims 17 to 21, further comprising a step for producing at least one power component and/or at least one RF component in the semiconductor substrate or layer.

23. A method of joining or assembling two substrates or layers (40, 60), wherein the first substrate (40) or first layer has roughness of more than 0.5 nm rms or has chemistry that is incompatible with molecular bonding, and having thermal conductivity of more than 1 W/cm/K, and the second substrate (60) or second layer having roughness of less than 0.5 nm rms, said method comprising:

- forming a layer (42) termed the bonding layer directly on the first substrate or the first layer having roughness of more than 0.5 nm rms;
- bonding said bonding layer to said second substrate (60) or second layer having roughness of less than 0.5 nm rms, by molecular bonding.

24. A method of joining or assembling two substrates (40, 50) or layers having roughness of more than 0.5 nm rms or having chemistry that is incompatible with molecular bonding, said method comprising:

- forming a layer (42, 52) termed the bonding layer directly on each substrate or on each layer to be assembled;
- bonding said bonding layers together by molecular bonding.

25. A method according to claim 23 or claim 24, wherein the material of each of the substrates or layers with roughness of more than 0.5 nm rms is selected from diamond or aluminum nitride.