

(19) World Intellectual Property Organization
International Bureau



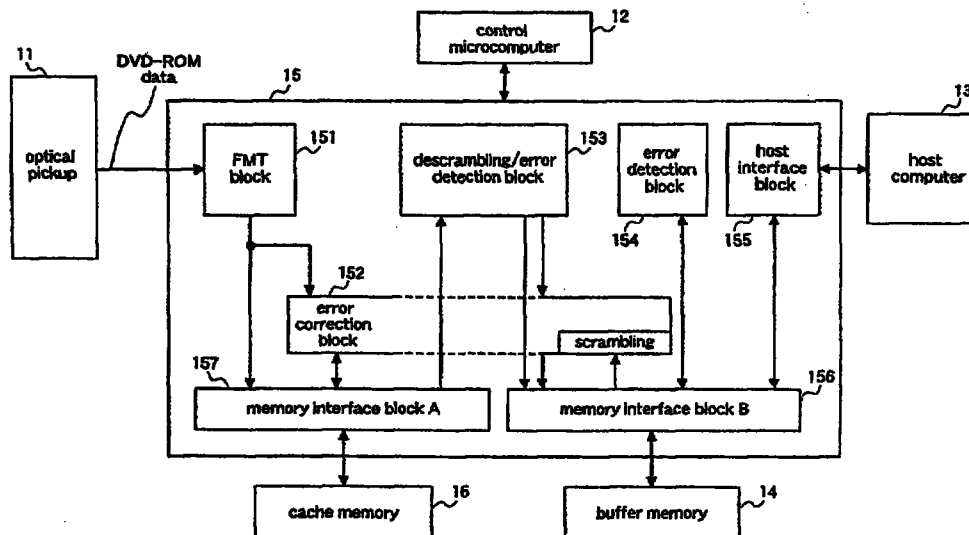
(43) International Publication Date
22 March 2001 (22.03.2001)

PCT

(10) International Publication Number
WO 01/20607 A1

- (51) International Patent Classification⁷: G11B 20/18, H03M 13/15
- (21) International Application Number: PCT/JP00/06122
- (22) International Filing Date:
8 September 2000 (08.09.2000)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
11/256736 10 September 1999 (10.09.1999) JP
- (71) Applicant (for all designated States except US): MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 (JP).
- (72) Inventor; and
(75) Inventor/Applicant (for US only): AOKI, Toru [JP/JP]; Ko 2003-51, Shimoshimayama, Saijo-shi, Ehime 793-0006 (JP).
- (74) Agent: HAYASE, Kenichi; Hayase & Co. Patent Attorneys, 8F, Esaka ANA Bldg., 17-1, Enoki-cho, Suita-shi, Osaka 564-0053 (JP).
- (81) Designated States (national): CN, ID, JP, KR, SG, US.
- Published:
— With international search report.
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SIGNAL PROCESSOR FOR CORRECTING AND DETECTING ERRORS



(57) Abstract: In a signal processor according to the present invention, error correction is performed on data which has been subjected to predetermined signal processing, for each predetermined block unit, by an error correction block (152), in parallel with the operation of sequentially storing the data in a cache memory (16). Then, error detection is performed on the data for each predetermined block unit by a descrambling/error detection block (153), and the data is stored in a buffer memory (14). Based on the results of the error detection and the error correction, when there exists some error in the data, the data with the error, which is stored in the buffer memory (14), is read out to be subjected to error correction again. When there is no error, the data corresponding to one block and stored in the buffer memory (14) is transmitted to a host computer (13) without performing error correction again.



WO 01/20607 A1