What is claimed is:

1. A method of manufacture of an integrated circuit system comprising:

forming reticle data;

detecting a sub-geometry, a singularity, or a combination thereof in the reticle data;

applying a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data; and

fabricating an integrated circuit from the reticle data.

2. The method as claimed in claim 1 further comprising setting a width and a height of the unit cell based on the sub-geometry size.

3. The method as claimed in claim 1 wherein applying the patch cell includes:

bridging lines between rectangular shapes; and

intersecting, a measurement from the singularity, the lines and the rectangular shapes.

4. The method as claimed in claim 1 wherein fabricating the integrated circuit includes:

providing a substrate;

coating a photoresist material on the substrate;

focusing a set of projection optics on the photoresist material; and

providing a reticle system for projecting the reticle data.

5. The method as claimed in claim 1 wherein detecting the singularity includes locating two rectangular shapes meeting at a corner.

6. A method of manufacture of an integrated circuit system comprising:

forming reticle data having a first shape and a second shape;

detecting a sub-geometry, a singularity, or a combination thereof in the reticle data including locating vertices of the first shape and the second shape;

applying a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data including forming a new shape by performing a Boolean operation on the first shape, the second shape, the unit cell, the patch cell, or the combination thereof; and

fabricating an integrated circuit from the reticle data including forming the new shapes on the integrated circuit.

7. The method as claimed in claim 6 further comprising setting a width and a height of the unit cell based on the sub-geometry size including providing a tab measurement having a fixed value.

8. The method as claimed in claim 6 wherein applying the patch cell includes:

bridging lines between rectangular shapes including forming the lines parallel to each other; and

intersecting, a measurement from the singularity, the lines and the rectangular shapes including forming a bridge region between the rectangular shapes.

9. The method as claimed in claim 6 wherein fabricating the integrated circuit includes:

providing a substrate including providing a stepper for mounting the substrate;

coating a photoresist material on the substrate including applying a super fine pattern forming material;

focusing a set of projection optics on the photoresist material including converging radiation beams; and

providing a reticle system for projecting the reticle data for forming the integrated circuit layer by layer.

10. The method as claimed in claim 6 wherein detecting the singularity includes locating two rectangular shapes meeting at a corner including failing a mask rules check.

11. An integrated circuit system comprising:

reticle data on a photomask;

a sub-geometry, a singularity, or a combination thereof detected in the reticle data;

a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data; and

an integrated circuit fabricated from the reticle data.

12. The system as claimed in claim 11 further comprising a width and a height of the unit cell based on the sub-geometry size.

13. The system as claimed in claim 11 wherein the patch cell includes lines, between rectangular shapes, spaced a measurement from the singularity on a reticle system.

14. The system as claimed in claim 11 wherein the integrated circuit includes a substrate having the reticle data formed thereon.

15. The system as claimed in claim 11 wherein the singularity includes two rectangular shapes with a corner collocated.

16. The system as claimed in claim 11 further comprising:

a first shape and a second shape in the reticle data;

vertices of the first shape and the second shape located to detect the sub-geometry, the singularity, or the combination thereof; and

a new shape formed by a Boolean operation on the first shape, the second shape, the unit cell, the patch cell or the combination thereof includes the new shapes formed on the integrated circuit.

17. The system as claimed in claim 16 further comprising a width and a height of the unit cell based on the sub-geometry size includes a tab measurement with a fixed value.

18. The system as claimed in claim 16 wherein the patch cell includes lines, between rectangular shapes, spaced a measurement from the singularity on a reticle system includes a bridge region between the rectangular shapes.

19. The system as claimed in claim 16 wherein the integrated circuit includes a substrate having the reticle data formed thereon includes the integrated circuit diced from the substrate.

20. The system as claimed in claim 16 wherein the singularity includes two rectangular shapes with a corner collocated including determining a single point of contact of the rectangular shapes.

What is claimed is:

1. A method of manufacture of an integrated circuit comprising:

forming reticle pattern having at least a first shape and a second shape for fabricating an integrated circuit from the reticle pattern;

detecting a sub-geometry, a singularity, or a combination thereof in the reticle pattern between the first shape and the second shape;

applying a unit cell, a patch cell, or a combination thereof to the reticle pattern for removing the sub-geometry, the singularity, or the combination thereof from the reticle pattern including forming a new shape by performing a Boolean operation on the first shape, the second shape, the unit cell, the patch cell, or the combination thereof; and

fabricating the integrated circuit from the reticle pattern having at least the first shape, the second shape, and including the new shapes on the integrated circuit.

2. The method as claimed in claim 1 further comprising setting a width and a height of the unit cell based on the sub-geometry size.

3. The method as claimed in claim 1 wherein applying the patch cell includes:

bridging lines between rectangular shapes; and

intersecting, a measurement from the singularity, the lines and the rectangular shapes.

4. The method as claimed in claim 1 wherein fabricating the integrated circuit includes:

providing a substrate;

coating a photoresist material on the substrate;

focusing a set of projection optics on the photoresist material; and

providing a reticle system for projecting the reticle pattern.

5. The method as claimed in claim 1 wherein detecting the singularity includes locating two rectangular shapes meeting at a corner.

6. A method of manufacture of an integrated circuit system comprising:

forming reticle data having a first shape and a second shape;

detecting a sub-geometry, a singularity, or a combination thereof in the reticle data including locating vertices of the first shape and the second shape;

applying a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data including forming a new shape by performing a Boolean operation on the first shape, the second shape, the unit cell, the patch cell, or the combination thereof; and

fabricating an integrated circuit from the reticle data including forming the new shapes on the integrated circuit.

7. The method as claimed in claim 6 further comprising setting a width and a height of the unit cell based on the sub-geometry size including providing a tab measurement having a fixed value.

8. The method as claimed in claim 6 wherein applying the patch cell includes:

bridging lines between rectangular shapes including forming the lines parallel to each other; and

intersecting, a measurement from the singularity, the lines and the rectangular shapes including forming a bridge region between the rectangular shapes.

9. The method as claimed in claim 6 wherein fabricating the integrated circuit includes:

providing a substrate including providing a stepper for mounting the substrate;

coating a photoresist material on the substrate including applying a super fine pattern forming material;

focusing a set of projection optics on the photoresist material including converging radiation beams; and

providing a reticle system for projecting the reticle data for forming the integrated circuit layer by layer.

10. The method as claimed in claim 6 wherein detecting the singularity includes locating two rectangular shapes meeting at a corner including failing a mask rules check.