

DELAYED DETECTION MRC DIVERSITY CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a delayed detection maximum ratio composition (hereinafter referring to MRC) diversity circuit for use in a mobile radio base station and so forth.

Description of the Prior Art

There exists various kinds of MRC diversity circuits. The conventional circuit of this kind is shown in Fig. 1 (hereinafter referring to the first prior art).

The MRC diversity circuit employs maximum ratio composition controllers 25 to 28 as a controller for controlling diversity signal. The controller has no compensation function in terms of time base direction. For this reason, multipath difference of received diversity signal is large. There is the problem that when time base diffusion of signal is increased, effective control can not be implemented.

Fig. 2 is a block diagram showing another conventional MRC diversity circuit (hereinafter referring to the second prior art) disclosed in the Japanese Patent Application Laid-Open HEI 4-150320. In Fig. 2, reference numerals 35 to 38 represent adaptive matching filter, reference numeral 39 represents composition unit, and reference numeral 40 represents modulator.

A signal received by an antenna (not illustrated) is subjected to frequency conversion, before being converted into a signal of intermediate frequency band, thus being applied to input terminals 21 to 24 in every diversity. At this section, each signal is divided into two-branched signals. One of two-

branched signals is inputted to the adaptive matching filters 35 to 38 which have the constitution of transversal filter, being subjected to required signal processing, before being composed by the composition unit 39. Inter-symbol interference caused by the multipath is removed by the automatic equalizer 30, before being modulated to be judged by the modulator 31, thus being outputted from the output terminal 32 after coming into base band signal.

On the other hand, individual clock regenerative circuit is composed of maximum ratio composition controllers 25 to 28, composition unit 29, and a clock regenerator 34. The adaptive matching filters 35 to 38 have a constitution of transversal filter, thus correlating diffused signal with reference signal at each tap of the transversal filter. The adaptive matching filters 35 to 38 behave such that it picks up the signal from correlated tap, correction of time base using the adaptive matching filters 35 to 38 is capable of being performed.

In the above described conventional MRC diversity circuit, there is the problem that the MRC diversity circuit has no compensation function in terms of time base direction, thereby multipath difference becomes large so that time base diffusion of signal is increased, thus resulting in impossibility of effective control in the first prior art.

Also, there is the problem that although correction of the time base is implemented using the adaptive matching filter with the constitution of transversal filter, circuit constitution comes into complicated and expensive in the second prior art.

It is necessary to modulate all of the reception branches in case of MRC diversity as is generally known. At this case it becomes problem how to adjust bit synchronization. When all of

reception branches are provided with respective base band circuit such as synchronous circuit and so forth, the circuit becomes large-scale one, and interface between base band circuits of each system becomes complicated.

Furthermore, as described in the invention of the Japanese Patent Application Laid-Open No. HEI 4-207821, when the sub received signal is composed with the main received signal such that phase of the sub received signal corresponds with phase of the main received signal with the signal adjusted each other, there are problems that when receiving field strength (hereinafter referring to RSSI) of the main received signal deteriorates, synchronization achievement comes into difficult.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present invention to provide a delayed detection MRC diversity circuit which has superior receiving characteristics such as fading characteristics and so forth with simple circuit constitution without adjustment of synchronization in every reception branch independently.

According to one aspect of the present invention, for achieving the above-mentioned object, there is provided a delayed detection MRC diversity circuit which composes a signal received by a plurality of reception branches with required bit synchronous timing to demodulate, comprises means for detecting a reception branch with maximum RSSI, means for regenerating clock while adjusting the signal received by the reception branch, means for composing to demodulate said signal received by said plurality of reception branches with synchronous timing of said clock.

In the delayed detection MRC diversity circuit according to the above aspect, the means for detecting a reception branch with maximum RSSI compares to detect RSSI in every symbol which is received by the plurality of reception branches.

Furthermore, the delayed detection MRC diversity circuit according to the above aspect further comprises means for detecting always a reception branch with maximum RSSI, means for regenerating clock while adjusting the signal received by the reception branch, means for composing to demodulate the signal received by the plurality of reception branches with synchronous timing of the clock, whereby bit synchronization is ensured without another operation.

As described above, the delayed detection MRC diversity circuit according to the invention is capable of adjusting the reception branch of maximum RSSI with timing of bit synchronization. Even if the RSSI of the reception branch which is adjusted with the timing of bit synchronization is weakened by fading or the like, it becomes possible to adjust the bit synchronization properly.

It is proper that only MRC diversity circuit section is connected to all of the reception branches. Consequently, the greater part of base band circuit such as the synchronous circuit and so forth can do with only one circuit for the reception branch with maximum RSSI. The delayed detection MRC diversity circuit with proper receiving characteristic can be realized without enlarging circuit scale.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with the accompanying drawings. It should be expressly understood,

however, that the drawings are for purpose of illustration only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an example of this kind of conventional MRC diversity circuit;

Fig. 2 is a block diagram showing another example of this kind of conventional MRC diversity circuit;

Fig. 3 is a block diagram showing an outline of an embodiment of a delayed detection MRC diversity circuit according to the present invention;

Fig. 4 is a timing chart showing bit synchronous timing between respective reception branches 1 to 4 and regenerative clock; and

Fig. 5 is a block diagram showing an outline of another embodiment of a delayed detection MRC diversity circuit according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will now be described in detail referring to the accompanying drawings. Fig. 3 is a block diagram showing an outline of an embodiment of a delayed detection MRC diversity circuit according to the present invention. In Fig. 3, reference numerals 1 to 4 represent reception branch each. Diversities with four reception branches are constituted in the embodiment. Reference numeral 5 represents a comparison circuit for selecting a reception branch with maximum RSSI in every symbol while always comparing RSSI of respective reception branches. Reference numeral 6 represents a

selector for outputting while selecting only signal of intermediate frequency (IF) band from the reception branch selected by the comparison circuit 5. Reference numeral 7 represents a synchronous phase sampling counter for phase-sampling intermediate frequency (IF) signal outputted from the selector 6. Reference numeral 8 represents a bit synchronous circuit for outputting regenerative clock while adjusting bit synchronous timing with output from the synchronous phase sampling counter.

Furthermore, reference numeral 15 represents a MRC diversity circuit section. The MRC diversity circuit section 15 of this embodiment comprises synchronous phase sampling counters 9 to 12 for phase-sampling signal of intermediate frequency band from the reception branches 1 to 4 respectively, a composition circuit 13 for composing phase value from the phase sampling counter 9 to 12 respectively, and a demodulation circuit 14 for demodulating on the basis of composed phase value. The regenerative clock from the bit synchronous circuit 8 is inputted to each of the phase sampling counters 9 to 12, the composition circuit 13, and the demodulation circuit 14, thus the MRC diversity section 15 operates on the reference of the clock.

Next, operation thereof will be described. Fig. 4 is a timing chart showing bit synchronous timing between respective reception branches 1 to 4 and regenerative clock. The comparison circuit 5 always compares RSSI from respective reception branches 1 to 4 with one another in every symbol, thus outputting the information to the selector 6 while always detecting the reception branch with the maximum RSSI. In Fig. 4, the reception branch 1 with maximum RSSI is selected to synchronize.

The selector 6 selects only signal of intermediate

frequency band from the reception branch having maximum RSSI in virtue of the information from the comparison circuit 5 to input to the phase sampling counter 7, before adjusting the signal of intermediate frequency band with the bit synchronous timing at the bit synchronous circuit 8, thus outputting the regenerative clock, before inputting the outputted regenerative clock to the MRC diversity circuit section 15. The MRC diversity circuit section 15 implements a phase sampling of signal of the intermediate frequency band from the respective reception branches 1 to 4, a MRC operation, and a demodulating operation to output using the timing of the regenerative clock.

Consequently, it is not necessary to adjust synchronization independently in every reception branch. It is capable of composing the signal of intermediate frequency band into the phase difference information with maximum RSSI and more positive bit-timing. The delayed detection MRC diversity circuit with superior receiving characteristics is obtained.

Fig. 5 is a block diagram showing an outline of another embodiment of a delayed detection MRC diversity circuit according to the present invention. A MRC diversity circuit section 16 comprises N radices of diversities, a counter, a composition unit and so forth. The MRC diversity circuit section 16 is different from the MRC diversity circuit section 15 which is shown in Fig. 3.

Namely, a delayed detection MRC diversity circuit according to the invention is capable of implementing not only four radices shown in Fig. 3 but also any number of diversities. The MRC diversity circuit section is capable of implementing in relation to any circuit which performs this kind of composing operation and demodulating operation with required timing, which

does not employ the phase sampling counter.

As described above, according to the invention, the delayed detection MRC diversity circuit has the constitution that it causes timing of bit-synchronization to always adjust to the reception branch with the maximum RSSI. The signal of intermediate frequency band from all of the reception branches always can be converted into the phase difference information with more positive bit-timing to be composed. As a result, the circuit with better receiving characteristics and high reliability can be realized.

Furthermore, it is proper that only MRC diversity circuit section is connected to all of the reception branches. Consequently, the greater part of base band circuit such as the synchronous circuit and so forth can do with only one circuit for the reception branch with maximum receiving electric field intensity even if any number of radices of diversities exist. There is the effect that simple and inexpensive circuit is capable of being realized.

While preferred embodiments of the invention have been described using specific terms, such description is for illustrative purpose only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.



WHAT IS CLAIMED IS:

1. A delayed detection MRC diversity circuit which composes a signal received by a plurality of reception branches with required bit synchronous timing to demodulate, comprising:

means for detecting a reception branch with maximum RSSI (receiving field strength);

means for regenerating clock while adjusting said signal received by said reception branch with bit synchronization;

means for composing to demodulate said signal received by said plurality of reception branches with synchronous timing of said clock.

2. A delayed detection MRC diversity circuit according to claim 1, wherein said means for detecting a reception branch with maximum RSSI compares to detect RSSI in every symbol received by said plurality of reception branches.

3. A delayed detection MRC diversity circuit according to claim 1, further comprising:

means for detecting always a reception branch with maximum RSSI;

means for regenerating clock while adjusting said signal received by said reception branch with bit synchronization;

means for composing to demodulate said signal received by said plurality of reception branches with synchronous timing of said clock,

whereby bit synchronization is ensured without another operation.

4. A method of the delayed detection MRC diversity



circuit which composes a signal received by a plurality of reception branches with required bit synchronous timing to demodulate, comprising the steps of:

- detecting a reception branch with maximum RSSI;
- regenerating clock while adjusting said signal received by said reception branch with bit synchronization;
- composing to demodulate said signal received by said plurality of reception branches with synchronous timing of said clock.

5. A method of the delayed detection MRC diversity circuit according to claim 4, wherein the step for detecting a reception branch with maximum RSSI is the step for comparing to detect RSSI in every symbol which is received by said plurality of reception branches.

6. A method of the delayed detection MRC diversity circuit according to claim 4, further comprising the steps of:

- detecting always a reception branch with maximum RSSI;
- regenerating clock while adjusting said signal received by said reception branch with bit synchronization; and
- composing to demodulate said signal received by said plurality of reception branches with synchronous timing of said clock,

whereby bit synchronization is ensured without another operation.