

PATENT SPECIFICATION

DRAWINGS ATTACHED

L193.310

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Date of Application (No. 30326/67) and filing Complete Specification: 30 June, 1967.

Application made in United States of America (No. 562,178) on 1 July, 1966.

Complete Specification Published: 28 May, 1970.

Index at acceptance:—H1 K(211, 21Y, 217, 225, 243, 273, 277, 287, 288, 306, 312, 34Y, 341, 353, 358, 36Y, 361, 41Y, 415, 422, 511, 51Y, 517, 52Y, 530, 578, 579, 581, 583, 59Y 61Y, 611, 618, 619, 616, 63Y, 638, 650); Cl A13

International Classification:—H 01 17/00

COMPLETE SPECIFICATION

Process for Fabricating Planar Semiconductor Devices

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to the fabrication of semiconductor devices, and more particularly relates to an improved process for fabricating planar semiconductor devices and to the improved product.

In the conventional planar process, particularly the silicon planar process, high temperature thermally grown silicon oxides are extensively used for diffusion masking, junction passivation, and insulation. For example, in the fabrication of a silicon transistor, a layer of thermal silicon dioxide is first formed on the surface of a substrate by raising the substrate to a high temperature of about 1200° C in an ambient atmosphere of steam or wet oxygen. A diffusion window is then cut in the silicon dioxide layer using photolithographic and etching techniques. The slice is then placed in a deposition reactor and an impurity, such as phosphorous or boron, is diffused into the exposed surface. During the deposition of the impurity, a glass-like film is formed over the surface of the silicon. Unless an unlimited source of impurities is desired for the diffusion step, this layer is removed using a deglazing technique. Then the slice is again raised to a high temperature in excess of 900° C, typically at about 1200° C, in an ambient atmosphere of oxygen and water for a considerable period of time during which an oxide layer is formed over the diffusion window and the original oxide layer is increased slightly in thickness. A second diffusion window is then

formed in the second formed oxide layer and the diffusion process repeated as many times as required to complete the device. In the final device, the composite of oxide layers formed during the various steps of the fabrication process are retained to passivate and protect the junctions emerging at the surface of the silicon. Thus, a transistor, for example, has three distinct layers of oxide, which are of varying thickness and which are doped differently, the initial oxide being doped with the collector impurity, the second oxide being doped with the base impurity, and the third oxide layer being doped with the emitter impurity.

A number of disadvantages are inherent in the conventional planar process using the thermally grown oxide layers. During the initial oxidation, out diffusion from the substrate occurs due to the very high temperature used for oxidation. This results in a change in the thickness and impurity profile of any epitaxial layer that may be present at the surface of the substrate. Also, the thermally grown oxide has a deficiency of oxygen which gives rise to positive charges within the oxide. Under the subsequent influence of high voltage and high temperature, the positive charges migrate, resulting in gradual changes in the electrical characteristics of the device. Further, at the elevated temperatures used for thermal oxidation and diffusion, silicon itself acts as a reducing agent for the silicon dioxide. Consequently, oxygen vacancies are created in the oxide near the silicon dioxide-silicon interface, giving rise to positively charged regions in the vicinity of the interface. The use of an ambient atmosphere of oxygen and water to grow a thermal oxide over the base-collector junction and then over the emitter-base junction during the base and emitter diffusion steps tends to cause many undesirable effects, such as soft junctions, pipes, etc.

Further, the thermal oxides grown during

[Price 5s. 0d.]

the base and emitter diffusions are doped with impurities such as phosphorous and boron, which contribute to instability of the device. The multiple oxide layers resulting from the conventional planar process also cause considerable problems in the photo-resist masking, particularly when small geometry devices are being fabricated, due both to the varying thicknesses of the several oxide layers and the differences in doping of the oxide layers which tend to result in different etch rates.

In many instances, an extremely high surface concentration is desirable in certain regions, such as the emitter of a transistor. However, the growing of the high temperature silicon oxide during the conventional planar process tends to reduce the surface concentration and change the impurity profile from an error function to a gaussian function. Also, in the thermally grown oxides it is difficult to eliminate sodium and other contaminants, because the furnace tube and boat become sources of contamination at the high temperatures necessary for the formation of the oxides.

An object of this invention is to produce an improved semiconductor device.

According to one aspect of the present invention there is provided a process for fabricating a semiconductor device, the process including at least one diffusion step, the or each diffusion being effected through a low temperature silicon dioxide diffusion mask, and in which following completion of the diffusion step or steps all remaining silicon dioxide is removed from the device and replaced by a final low temperature silicon dioxide layer through which electrical contact can be made with the underlying active regions to complete the device.

According to a second aspect the invention provides a semiconductor device comprising a body of semiconductor material having a substantially planar face and at least one diffused region formed in the face, the entire periphery of the or each diffused region terminating at the planar face, a passivating layer of low temperature silicon dioxide formed over the planar face having at least one contact window formed therein, the passivating layer of silicon dioxide having no oxygen vacancies therein and being substantially homogeneous and of uniform thickness, and a metallized contact extending through the or each contact window into contact with the planar face.

In this Specification a low temperature oxide layer is defined as an oxide layer formed by deposition of reagents from a gaseous stream at substrate temperatures less than about 600° C, and is contrasted to a high temperature oxide layer of the type formed at temperatures generally in excess of 900° C by the reaction of oxygen with the substrate material. The low temperature silicon dioxide layers may be formed by the reaction of silicon tetrahydride (SiH₄) and oxygen for use as

diffusion masks. During the diffusion step, the formation of a high temperature oxide is retarded by using dry reagent streams and ambient atmospheres. All low temperature oxide layers used as diffusion masks are removed after the completion of all diffusion steps and replaced by a final, low temperature silicon dioxide layer. In the preferred form of the invention, each silicon dioxide layer is at least partially removed, and preferably completely removed, after each diffusion step and a new silicon dioxide layer deposited prior to the next diffusion step.

The invention may best be understood by reference to the following detailed description of an illustrative embodiment, when read in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a schematic drawing illustrating a reactor which may be used in carrying out the process of the present invention;

FIGURES 2—12 are somewhat schematic sectional views of a transistor during various stages of fabrication using the process of the present invention; and

FIGURE 13 is a somewhat schematic sectional view of a completed transistor fabricated in accordance with the present invention.

Referring now to the drawings, an apparatus for depositing a low temperature oxide in accordance with this invention is indicated generally by the reference numeral 10 in FIGURE 1. The device 10 is comprised of a thermostatically controlled heater plate 12 on which a bell jar 14 is disposed. The bell jar 14 has four oxygen inlets 16 and a silicon tetrahydride (SiH₄) inlet 18. The four oxygen inlets 16 direct oxygen horizontally and radially into the bell jar, thus tending to focus the incoming gas at a central point within the bell jar. The silicon tetrahydride inlet 18 directs a stream of silicon tetrahydride and a carrier gas vertically downwardly within the bell jar and has a nozzle 20 which tends to uniformly distribute the silicon tetrahydride into the incoming oxygen streams. A plurality of small notched openings 22 are provided in the bottom rim of the bell jar to form outlets, so that the mixture of gases must flow downwardly toward the surface of the heater 12 to exit from the outlets. A plurality of semiconductor slices 24 on which an oxide layer is to be formed are positioned on the heater 12 and heated to a controlled temperature of from about 300° C to about 400° C.

The process is useful in preparing a variety of semiconductor devices having planar geometries. By planar geometry, it is meant a semiconductor device wherein the peripheral boundary of a junction formed by a diffused region emerges at a plane surface of a semiconductor body. Also, the process is applicable to the fabrication of planar devices from silicon, germanium, gallium arsenide and most other semiconductor materials. However, the

process is particularly applicable to the fabrication of silicon devices and therefore the process used to fabricate a double diffused silicon transistor having an epitaxial collector is selected as an illustrative embodiment of the invention.

Referring now to FIGURES 2-13, the slices 24 are typically p-type silicon material having from about 0.008 to about 0.009 ohm-centimeter resistivity, with an epitaxial layer 32 about 0.011 inch thick and having a resistivity of about 6.5 to about 10 ohm-centimeters. The slice is first thoroughly cleaned by first immersing it in trichloroethylene and acetone, then rinsing it in distilled water. The slice is then immersed in concentrated hydrofluoric acid and rinsed in distilled water. Then the slice is rinsed in hot water and cleaned in hot nitric acid at about 80°C, then rinsed in hot distilled water. Finally, the slice is rinsed in high purity 18 megohm-cm, distilled water.

After cleaning, the slice is placed in the reactor 10 and a thin silicon dioxide layer 34, typically about 7000 angstroms in thickness, is deposited on the epitaxial layer 32, as illustrated in FIGURE 2. This is accomplished by heating the slice 24 to a temperature between about 300°C and about 600°C, preferably about 350°C, and introducing a mixture of about 1% to 5% by volume silicon tetrahydride (SiH_4) in an inert carrier gas, such as argon or helium, through the inlet 18 at a rate of about 30 cc per minute, which is mixed with pure oxygen introduced through the inlets 16 at a rate of about 200 cc per minute. The gases react in the near vicinity of the slices 24 and result in the formation of a uniform silicon dioxide layer over the surface of the slice. Although the process just described for producing the low temperature silicon dioxide is preferred, the low temperature silicon dioxide can be produced by the pyrolytic decomposition of tetraethyl orthosilicate, although this has been found to produce an oxide layer significantly inferior to the layer produced by the above described reaction.

Next, a base diffusion window 36 is cut in the silicon oxide layer 34, as illustrated in FIGURE 3, using conventional photolithographic and etching techniques so as to expose the surface of the epitaxial layer 32 in the area where a base region is to be formed by diffusion. Next, the slice is placed in a deposition furnace, heated to about 765°C, and a gaseous stream containing phosphorus oxychloride (POCl_3) and a suitable carrier gas, such as nitrogen and oxygen, without any water, passed through the reactor so that a phosphorus glass film 38 is formed on the exposed surface of the epitaxial layer 32 and a high concentration of phosphorus impurities 40 diffused into the surface of the epitaxial layer to a very shallow depth. The slice is then removed and deglazed to remove the phosphorus

glass 38 by placing the slice in a 10% hydrofluoric acid solution for about eight minutes to give a sheet resistivity of from about 500 to about 700 ohms per square. The slice is then placed in an oven and heated to about 1200°C in a dry ambient atmosphere of oxygen and nitrogen for about 4.5 hours so that the impurities 40 will be diffused to form the profile substantially as illustrated in FIGURE 4. It is important to note that no steam or water is used during this diffusion process. Although some oxygen is necessary to provide an oxidizing atmosphere and prevent etching of the silicon at diffusion temperatures, the rate of oxide growth is very slow and only a very thin oxide layer is formed during the diffusion step. The diffused impurities 40 then form the base region of the transistor.

After the base diffusion, all oxide is preferably stripped from the slice. This is desirable because during the high temperature of the base diffusion, the silicon oxide layer 34, which is in a molten state, tends to gather impurities from the silicon, and the oxide layer tends to get contaminated. Also, during the high temperature diffusion, oxide deficiencies are created in the oxide layer 34, which is an undesirable condition in the final product. The oxide layer 34 can be completely stripped by etching in concentrated hydrofluoric acid, then rinsing first in distilled water and finally in high purity distilled water. If desired, however, a substantial portion of the impurities can be removed by subjecting the oxide layer to the etching solution only for a period of time necessary to remove the top of the oxide layer. Since the impurities tend to concentrate at the surface of the oxide layer as it solidifies upon cooling after the diffusion step, the major portion of the impurities will be removed. This procedure has the advantage of not exposing the substrate during subsequent processing, and the remaining oxide layer can be completely removed at a later point in the process if desired.

After the oxide layer 34 is stripped from the slice, a completely new oxide layer 42 is deposited, as illustrated in FIGURE 5, using the process heretofore described in connection with the formation of the oxide layer 34. An emitter diffusion window 44 is then cut in the oxide layer 42, substantially as illustrated in FIGURE 6, using conventional photolithographic and etching techniques. Boron is then diffused through the window 44 by heating the substrate to about 1150°C in a deposition furnace and passing a carrier gas containing boron tribromide (BBr_3) over the substrate in the conventional manner, except that all of the gases are dry so that again no oxide is intentionally grown during the emitter diffusion, although a very thin layer of oxide may be formed as a result of maintaining an oxidizing atmosphere. The complete emitter diffusion is carried out in the presence of the impurity

source material so as to provide the necessary high concentration of boron in the emitter region 46, as illustrated in FIGURE 7.

After the emitter diffusion, the boron glaze 48 resulting from the diffusion step is removed by treating the slices first in concentrated hydrofluoric acid followed by a de-ionized water rinse, and then in hot nitric acid followed by a de-ionized water rinse. Then all of the remaining oxide is completely removed by treating the slices in concentrated hydrofluoric acid as heretofore described to produce a clean surfaced slice as illustrated in FIGURE 8.

The slice is then cleaned in hot nitric acid and rinsed in hot de-ionized water, then in high purity distilled water. A new layer 49 of silicon dioxide is then formed using the process heretofore described, and diffusion windows 50 and 52 are cut in the oxide layer using conventional photolithographic and etching techniques. The slice as illustrated in FIGURE 10 is then placed in a diffusion reactor, heated to about 950° C, and a stream containing phosphorus oxychloride (POCl_3) passed over the substrate for about five minutes to form the heavily doped diffused base contact regions 54 and 56. During this diffusion process, the gases are again dry so that no oxide is purposely grown over the diffused contact regions 54 and 56. During this phosphorus diffusion, the silicon oxide layer 49 is liquified and doped with phosphorus and this together with the phosphorus glaze formed over the diffused regions 54 and 56 tends to gather the impurities from the silicon and harden the junctions between the diffused regions.

After the diffusion of the regions 54 and 56, the doped and contaminated oxide layer 49 is removed completely by etching as heretofore described, leaving a slice substantially as illustrated in FIGURE 11. The slice is then cleaned very carefully, using the procedures heretofore described, and a final layer 58 of silicon dioxide deposited using the process heretofore described. The silicon dioxide layer 58 may be doped with appropriate impurities such as phosphorus or boron to further passivate the semiconductor device if desired.

Contact windows are then formed in the oxide layer 58 over the emitter region 46, and the base contact regions 54 and 56. A metallized layer is then deposited over both surfaces of the slice and patterned using photolithographic and etching techniques to form expanded base contacts 60 and 62, and expanded emitter contact 64. The metallized film 66 on the bottom side of the slice forms the collector contact which is in good ohmic contact with the epitaxial collector region 32 through the low resistivity substrate 30.

The resulting transistor illustrated in FIGURE 13 has a uniform and homogeneous layer of silicon dioxide over the base and emit-

ter junctions. The final oxide layer has no oxygen deficiency at its surfaces because it has never been subjected to a high temperature, and may be doped to a controlled level to stabilize the device. During each diffusion step, the oxide layer over the substrate that is used for a diffusion mask is in an essentially liquid state. The silicon dioxide tends to attract and gather any impurities in the adjacent silicon material, and these impurities tend to concentrate at the surface of the silicon dioxide layer as the slice is cooled. Also, as a result of the high temperature, the silicon tends to reduce the silicon dioxide resulting in oxygen vacancies in the silicon dioxide layer adjacent to the silicon. For this reason, it is desirable to completely remove the silicon dioxide after each diffusion and then redeposit a new silicon dioxide layer prior to the next diffusion. If desired, however, the silicon dioxide layer may be only partially removed after each diffusion so that the impurities concentrated at the surface of the silicon dioxide will be removed. The remaining portion of the oxide layer will then protect the junction during handling, and the collection of silicon oxide layers can be simultaneously removed after the device is completely fabricated and prior to the deposition of the final layer 58 of silicon dioxide in order to remove the oxygen deficient silicon oxide layer from the final product.

It is also advantageous to at least partially remove the silicon oxide layer after each diffusion step, and preferably to totally remove the oxide layer, so that a more uniform and nearly planar surface will be provided upon which the new silicon dioxide layer can be deposited. The resulting smooth and uniform surface simplifies the following photolithographic and etching steps. This is particularly important in small geometry devices where an uneven surface creates significant problems during the photolithographic step.

The process of the present invention is generally applicable to the formation of all silicon planar devices such as silicon planar transistors, mesa transistors, diodes, SCR's, solar cells, solid state radiation detectors, and also to similar devices made from germanium, gallium arsenide, and other semiconductor materials.

WHAT WE CLAIM IS:—

1. A process for fabricating a semiconductor device, the process including at least one diffusion step, the or each diffusion being effected through a low temperature silicon dioxide diffusion mask, and in which following completion of the diffusion step or steps all remaining silicon dioxide is removed from the device and replaced by a final low temperature silicon dioxide layer through which electrical contact can be made with the underlying active regions to complete the device.

2. A process according to Claim 1 wherein the final low temperature silicon dioxide layer

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source material so as to provide the necessary high concentration of boron in the emitter region 46, as illustrated in FIGURE 7.

After the emitter diffusion, the boron glaze 48 resulting from the diffusion step is removed by treating the slices first in concentrated hydrofluoric acid followed by a de-ionized water rinse, and then in hot nitric acid followed by a de-ionized water rinse. Then all of the remaining oxide is completely removed by treating the slices in concentrated hydrofluoric acid as heretofore described to produce a clean surfaced slice as illustrated in FIGURE 8.

The slice is then cleaned in hot nitric acid and rinsed in hot de-ionized water, then in high purity distilled water. A new layer 49 of silicon dioxide is then formed using the process heretofore described, and diffusion windows 50 and 52 are cut in the oxide layer using conventional photolithographic and etching techniques. The slice as illustrated in FIGURE 10 is then placed in a diffusion reactor, heated to about 950°C, and a stream containing phosphorus oxychloride (POCl_3) passed over the substrate for about five minutes to form the heavily doped diffused base contact regions 54 and 56. During this diffusion process, the gases are again dry so that no oxide is purposely grown over the diffused contact regions 54 and 56. During this phosphorus diffusion, the silicon oxide layer 49 is liquified and doped with phosphorus and this together with the phosphorus glaze formed over the diffused regions 54 and 56 tends to gather the impurities from the silicon and harden the junctions between the diffused regions.

After the diffusion of the regions 54 and 56, the doped and contaminated oxide layer 49 is removed completely by etching as heretofore described, leaving a slice substantially as illustrated in FIGURE 11. The slice is then cleaned very carefully, using the procedures heretofore described, and a final layer 58 of silicon dioxide deposited using the process heretofore described. The silicon dioxide layer 58 may be doped with appropriate impurities such as phosphorus or boron to further passivate the semiconductor device if desired.

Contact windows are then formed in the oxide layer 58 over the emitter region 46, and the base contact regions 54 and 56. A metallized layer is then deposited over both surfaces of the slice and patterned using photolithographic and etching techniques to form expanded base contacts 60 and 62, and expanded emitter contact 64. The metallized film 66 on the bottom side of the slice forms the collector contact which is in good ohmic contact with the epitaxial collector region 32 through the low resistivity substrate 30.

The resulting transistor illustrated in FIGURE 13 has a uniform and homogeneous layer of silicon dioxide over the base and emit-

ter junctions. The final oxide layer has no oxygen deficiency at its surfaces because it has never been subjected to a high temperature, and may be doped to a controlled level to stabilize the device. During each diffusion step, the oxide layer over the substrate that is used for a diffusion mask is in an essentially liquid state. The silicon dioxide tends to attract and gather any impurities in the adjacent silicon material, and these impurities tend to concentrate at the surface of the silicon dioxide layer as the slice is cooled. Also, as a result of the high temperature, the silicon tends to reduce the silicon dioxide resulting in oxygen vacancies in the silicon dioxide layer adjacent to the silicon. For this reason, it is desirable to completely remove the silicon dioxide after each diffusion and then redeposit a new silicon dioxide layer prior to the next diffusion. If desired, however, the silicon dioxide layer may be only partially removed after each diffusion so that the impurities concentrated at the surface of the silicon dioxide will be removed. The remaining portion of the oxide layer will then protect the junction during handling, and the collection of silicon oxide layers can be simultaneously removed after the device is completely fabricated and prior to the deposition of the final layer 58 of silicon dioxide in order to remove the oxygen deficient silicon oxide layer from the final product.

It is also advantageous to at least partially remove the silicon oxide layer after each diffusion step, and preferably to totally remove the oxide layer, so that a more uniform and nearly planar surface will be provided upon which the new silicon dioxide layer can be deposited. The resulting smooth and uniform surface simplifies the following photolithographic and etching steps. This is particularly important in small geometry devices where an uneven surface creates significant problems during the photolithographic step.

The process of the present invention is generally applicable to the formation of all silicon planar devices such as silicon planar transistors, mesa transistors, diodes, SCR's, solar cells, solid state radiation detectors, and also to similar devices made from germanium, gallium arsenide, and other semiconductor materials.

WHAT WE CLAIM IS:—

1. A process for fabricating a semiconductor device, the process including at least one diffusion step, the or each diffusion being effected through a low temperature silicon dioxide diffusion mask, and in which following completion of the diffusion step or steps all remaining silicon dioxide is removed from the device and replaced by a final low temperature silicon dioxide layer through which electrical contact can be made with the underlying active regions to complete the device.

2. A process according to Claim 1 wherein the final low temperature silicon dioxide layer



is formed by the reaction of silicon tetrahydride (SiH_4) and oxygen at a temperature between 300°C and 600°C .

3. A process according to Claim 1 or 2, including a plurality of diffusion steps wherein each low temperature silicon dioxide diffusion mask is completely removed after each diffusion step and a new low temperature silicon dioxide diffusion mask formed prior to the next diffusion.

4. A process according to any preceding Claim wherein each diffusion is made in a dry ambient atmosphere to restrict the formation of a thermal oxide during the diffusion step.

5. A process for fabricating a planar semiconductor device having at least one diffused region, the or each diffused region being formed by the steps of forming a low temperature silicon dioxide layer over the surface of a semiconductor substrate by the reaction of silicon tetrahydride (SiH_4) and oxygen at a temperature less than 400°C , etching an opening in the silicon dioxide layer to form a diffusion mask, implanting a doping impurity in the substrate through the diffusion mask and diffusing the impurities by heating the substrate to a temperature in excess of 900°C in the presence of a gaseous mixture containing the doping impurity and essentially free of water, after the or all diffusion steps have been completed, entirely removing all remaining silicon dioxide and applying a final layer of said low temperature silicon dioxide to the surface of the substrate, etching contact openings in the final silicon dioxide layer over the active regions, and forming metallized contact pads over the contact openings.

6. A process according to Claim 5 wherein each silicon dioxide diffusion mask is completely removed from the surface of the substrate after each diffusion step.

7. A process for fabricating a diffused semiconductor device, wherein after completion of the diffusion step or steps, the surface of the semiconductor material is completely stripped of all oxides formed on the semiconductor material before or during the diffusion, a new silicon dioxide layer is deposited by heating

the semiconductor material to a temperature of between 300°C and 600°C in the presence of a mixture of silicon tetrahydride (SiH_4) and free oxygen (O_2), contact openings are etched in the silicon dioxide layer over active regions of the device, and metallized contacts are formed in the contact openings.

8. A process according to any preceding claim, in which the final silicon dioxide layer is doped with phosphorous or boron.

9. A process according to any preceding claim, substantially as described herein with reference to and as illustrated by the accompanying drawings.

10. A semiconductor device comprising a body of semiconductor material having a substantially planar face and at least one diffused region formed in the face, the entire periphery of the or each diffused region terminating at the planar face, a passivating layer of low temperature silicon dioxide formed over the planar face having at least one contact window formed therein, the passivating layer of silicon dioxide having no oxygen vacancies therein and being substantially homogeneous and of uniform thickness, and a metallized contact extending through the or each contact window into contact with the planar face.

11. The semiconductor device defined in claim 10 wherein the layer of silicon dioxide is the low temperature silicon dioxide resulting from the reaction of silicon tetrahydride and oxygen at a temperature between 300°C and 600°C .

12. A semiconductor device according to claim 10 or claim 11, in which the passivating layer of silicon dioxide is doped with phosphorous or boron.

13. A semiconductor device according to claim 10, substantially as described herein with reference to and as illustrated by Figures 2 to 13 of the accompanying drawings.

14. A semiconductor device formed by a process according to any of claims 1 to 9.

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