PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 23/00	A2	(11) International Publication Number: WO 99/23699
		(43) International Publication Date: 14 May 1999 (14.05.99)

(21) International Application Number: PCT/US98/22819

(22) International Filing Date: 28 October 1998 (28.10.98)

(30) Priority Data:
08/960,715 30 October 1997 (30.10.97) US

(71)(72) Applicant and Inventor: CHAPMAN, David, C. [US/US]; 2655 Keystone Avenue #41, Santa Clara, CA 95051 (US).

(74) Agents: CARLSON, Stephen, A. et al.; McDermott, Will & Emery, Suite 300, 99 Canal Center Plaza, Alexandria, VA 22314 (US).

(81) Designated States: CA, IL, JP, KR, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: POLYGON REPRESENTATION IN AN INTEGRATED CIRCUIT LAYOUT

(57) Abstract

An approach for representing polygons in an integrated circuit (IC) layout is provided. Polygons are represented by one or more wires, which in turn are each represented by one or more wire segments. Each wire segment is represented by a pair of directed line segments. A data structure hierarchy includes polygon data, wire data, wire segment data and branch data. The polygon data represents a set of IC devices to be represented in the IC layout. The wire data represents the wires that represent the polygons and specifies the associated wire segments and associated polygons. The wire segment data represents the wire segments and specifies the associated directed line segments for each wire segment that represent the wires and references the wire data. The branch data specifies connections between wires by specifying the connecting wire segments in the wires. A spacing check between a first polygon and a second polygon involves determining the canonical direction from the first polygon to the second polygon and testing the two closest faces between the polygons. To satisfy a spacing violation, an exclusion zone is constructed around the first polygon and the second polygon is moved a distance outside the exclusion zone which causes the minimum spacing required by a set of predetermined spacing criteria to be satisfied.