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(54) QUARTZ CRYSTAL TIMEPIECE

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates to quartz crystal time-

pieces. Rapid technological advances in electronic display techniques has made it possible to display a time indication digitally in quartz crystal wristwatches. Such quartz crystal wristwatches may perform additional functions, for example, it is conceivable to provide a stop watch function, a temperature display function, a humidity display function or a body temperature display function. If the wristwatch is provided with a stop watch function it is possible to measure a time period in 100ths or 1,000ths of a second which is not possible with conventional mechanical stop watches. However, conventional quartz crystal wristwatches have a number of disadvantages, among them, being time keeping accuracy and adjustment of the time rate.

According to the present invention, there is provided a quartz crystal timepiece comprising time keeping means including a quartz crystal vibrator arranged to oscillate in the thickness-shear mode at a resonant frequency between 1 MHz and 10 MHz for generating a standard time signal, and a digital display device driven by the time keeping means.

Preferably the timepiece includes logic circuitry for adjusting the time-rate.

The time keeping means may include a frequency divider circuit for producing a relatively low frequency output signal from the standard time signal, said logic circuitry being connected with the divider circuit and including a memory circuit operatively linked to the divider circuit by a gate circuit which, in operation, is controlled by the said relatively

low frequency output signal in dependence upon data stored in the memory circuit.

In the preferred embodiment the divider circuit, the gate circuit and the memory circuit each have the same number of stages, each stage of the memory circuit being connected to write memorised data into the corresponding stage of the divider circuit when the gate circuit is opened, means being provided for writing into the memory circuit a binary code representative of a predetermined period which thus determines the periodicity of said low frequency output signal.

The divider circuit may be a down-count type divider.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of a conventional digital quartz crystal wristwatch;

Figure 2 illustrates graphically the frequency-temperature characteristics of a quartz crystal vibrator of the flexural type and a quartz crystal vibrator of the thickness-shear type;

Figure 3 is a block diagram of a quartz crystal timepiece according to the present invention;

Figure 4 is a perspective view of a quartz crystal vibrator for the timepiece of Figure 3;

Figure 5 illustrates graphically the operation of the timepiece of Figure 3; and

Figure 6 is a block diagram illustrating, in greater detail, part of the timepiece of Figure 3.

Referring first to Figure 1 there is illustrated a conventional digital quartz crystal wristwatch having an oscillator circuit 1 which produces an output signal having a frequency of f_0 . The output signal from the oscillator circuit 1 is fed to a divider circuit 2 whose output signal has a frequency of f_1 . The output signal from the divider circuit 2 is fed to a divider circuit 3 which produces an hours signal, a minutes signal and a seconds signal from which the hours, minutes and seconds of a time indication

are produced. The signals from the divider circuit 3 are fed to a divider circuit 4 which drives a digital display device 5 composed of, for example, light emitting diodes or liquid crystal elements.

This conventional wristwatch has several disadvantages. It is difficult to improve the accuracy of the time keeping because the oscillator circuit 1 includes a quartz crystal vibrator 6 of the flexural type, e.g. a tuning fork type quartz crystal vibrator or a free-free bar type flexural vibrator, and such vibrators have a resonant frequency which is relatively low, e.g. in the several tens of KHz band. The frequency-temperature characteristics of a quartz crystal vibrator of the flexural type are shown by a quadratic curve (b) in Figure 2. It will be appreciated that the frequency-temperature characteristics are only flat over a relatively narrow temperature range. The temperature sensing elements 8 e.g. barium titanate, a varistor or a thermister may be used to compensate for the effect which change of temperature has on the quartz crystal vibrator 6. However, the use of a temperature sensing element itself causes problems, namely, temperature sensing element ages to an unacceptable extent and mass production of the temperature sensing element and the quartz crystal vibrator as a unit is particularly difficult. Furthermore, in order to adjust the time-rate (i.e. the rate of advance of the time indication) of the wristwatch of Figure 1, it is necessary to adjust the frequency f_1 of the output signal of the divider circuit 2 to a predetermined frequency, e.g. 1 Hz exactly. The frequency f_0 of the output signal of the oscillator circuit 1 is adjusted by a trimmer capacitor 7 in a resonant circuit which forms part of the oscillator circuit 1. When the frequency f_1 of the output signal of the divider circuit 2 is exactly 1 Hz and the division ratio of the divider circuit 2 is $\frac{1}{2^{13}}$, the frequency f_0 of the output signal of the oscillator circuit must be maintained accurately at 32768 Hz. However, means must be provided to maintain the frequency f_0 accurately at 32768 Hz and such means lower the stability of oscillation of the vibrator 6. Moreover, because the resonance frequency of the quartz crystal vibrator 6 can be varied only over a relatively narrow range by the trimmer capacitor, the vibrator cannot be produced inexpensively. Moreover, it needs considerable skill to adjust accurately the frequency of the output signal of the oscillator circuit 1 using the trimmer capacitor 7 and this too creates problems when it comes to mass production.

Using a digital display device it is possible to construct a digital quartz crystal chronograph which measures time in 100ths or 1,000ths of a second. Such chronographs however are usually used in districts with great temperature variations, for example, they may be used for time keeping at winter sports, and at athletic

sports meetings in the summer. However, a conventional chronograph using a quartz crystal vibrator of the flexural type will not keep time with a high degree of accuracy if used in both cold and hot climates for the reasons discussed above.

Figure 3 is a block diagram of a quartz crystal timepiece, e.g. a wristwatch according to the present invention having an oscillator circuit 11 which produces an output signal having a frequency of f_0' . This output signal is fed to a presettable divider circuit 21 which produces an output signal having a frequency of f_1' . The output signal from the divider circuit 21 is fed to a divider circuit 13 which produces timing signals from which the seconds, minutes, hours, date, days of the week and other elements of a time indication are produced. The timing signals are fed to a driving circuit 14 which drives a digital display device 15 which may be composed of, for example, light emitting diodes or liquid crystal elements. A time correcting circuit 22 for correcting the time indicated by the display device is connected to the divider circuit 13 and a logic time-rate adjusting circuit, to be described in greater detail hereinafter, is connected to the divider circuit 21.

The oscillator circuit 11 includes a quartz crystal vibrator 9 one possible form of which is illustrated in Figure 4. The vibrator 9 is a quartz crystal vibrator arranged to oscillate in the thickness-shear mode and having a bevel or convex section 30 and a main rectangular vibrating surface 31. Metallic film electrodes 32, 33 for exciting the vibrator are electrically connected to supporting terminals 34, 35 respectively. The vibrator is mounted on a base 36 which also electrically isolates the supporting terminals 34, 35. The vibrator 9 can be made of relatively small size in particular small enough to fit in a wristwatch. The thickness-shear vibrator of Figure 4 has the frequency-temperature characteristics shown by a cubic curve (a) in Figure 2. It will be seen that the frequency-temperature characteristics are flat over a relatively wide temperature range with the result that the use of temperature compensating elements is unnecessary. Thus a timepiece incorporating the vibrator of Figure 4 will be of higher accuracy even when influenced by considerable variations in temperature.

The vibrator of Figure 4 has a frequency of oscillation in a band between 1 MHz and 10 MHz and can be mass produced relatively easily. In the oscillator circuit 11 there are capacitors 37, 38 for controlling the phase of the output signal therefrom, an inverter 39 and a feedback resistor 40. The timerate can be adjusted logically as explained hereinafter so that the frequency of the output signal of the oscillator circuit does not need to be controlled by the capacitors 37, 38. Thus the capacitors 37, 38 can be included in an IC together with the inverter 39 and the resistor 40, so that the

reliability of the oscillator circuit 11 is improved.

Next, the method of adjusting the time-rate of the timepiece of Figure 3 will be described. The divider circuit 21 is a presettable down-count type divider composed of a plurality (n) of flip-flop stages $F/F_1, F/F_2 \dots F/F_n$ and is $\frac{1}{2^n}$ counter. Although the frequency f_1' of the output signal of the divider circuit 21 may be any desirable suitably required frequency it will be assumed, in what follows, to be 1 Hz exactly.

The gate circuit 23 has a plurality (n) of stages $g_1, g_2 \dots g_n$ and is controlled by a preset signal f_p generated from a preset signal generator 24 synchronously with the output signal from the divider circuit 21. When the preset signal f_p is generated, the gate circuit 23 causes data from a memory circuit 25, having a plurality (n) stages $m_1, m_2 \dots m_n$, to be written in the frequency divider 21. Because the divider circuit 21 is a downcount type divider for every pulse of the output signal from the oscillator circuit 11, (1, 0, 0, ... 0) is subtracted from the preset data in the divider circuit 21, and the data in the divider circuit 21 eventually becomes (0, 0, 0, ...). When this occurs an output pulse is generated by the divider circuit 21 and the preset signal f_p is generated by the generator 24. This action is repeated thereafter. The time-rate is adjusted, namely, the frequency f_1' is adjusted to be 1 Hz exactly by pre-setting the data in the memory 25.

Since the divider circuit 21 is $\frac{1}{2^n}$ counter, when the frequency f_0' 2^n Hz, the frequency f_1' is inevitably exactly 1 Hz and the data in the memory 25 is (1, 1 ... 1). When the frequency f_0' is below 2^n Hz the period of the output signal from the divider circuit 21 becomes $(1 + \Delta T)$ seconds as shown in Figure 5. Accordingly, a binary code which is decreased by the equivalent of ΔT is written in the memory circuit 25. For example, if the period of the output signal of the divider circuit 21 is longer by the equivalent of two pulses of the output signal of the oscillator circuit 11, data (1, 0, 1, ... 1) is written into the memory circuit 25.

As illustration in Figure 6 data may be written into the memory 25 in the same manner as time correction, i.e. correction of the contents of the divider circuit 13. For example, suppose that the set value of each bit in the memory is to be 1001, 1000, 0111, the display device 15 is caused to display 987 by means of the correcting circuit 22, four bits corresponding to each digit. Thus the contents of the divider circuit 13 is the same as that which it is desired to set in the memory 25. The output of each bit in the divider circuit 13 is connected to the input of a corresponding bit of the memory, so that the contents of the divider circuit are set into the memory 25 with timing f_1' .

The data in the memory circuit 25 disappears

when the power supply ceases, e.g. when a battery driving the timepiece is changed. The accuracy of adjustment of the time-rate is, it will be appreciated, proportional to the reciprocal of the frequency f_0' so that the higher the frequency f_0' , the greater the accuracy of adjustment of the time-rate. Accordingly, if the frequency f_0' is between 1 MHz and 10 MHz the time-rate can be adjusted to an accuracy of 0.09 seconds to 0.01 seconds a day.

As the time-rate is adjusted by logic circuitry, the resonant frequency of the vibrator 9 is arbitrarily selected as long as it is below 2^n Hz. Consequently, it is possible to construct inexpensive and highly stable wrist-watches.

Since the vibrator 9 is arranged to oscillate in the thickness-shear mode with relatively flat temperature-frequency characteristics over a relatively high temperature range, the timepiece is relatively unaffected by temperature changes and the provision of a trimmer capacitor in the oscillator circuit, which may introduce ageing problems, is not required. Due to the good temperature-frequency characteristics a chronograph may be made which is useable in places with widely differing climates without loss of accuracy. Moreover, since the display device 15 is digital the time indication can be read to 100ths and 1,000ths of a second.

Having regard to the provisions of Section 9 of the Patents Act, 1949, attention is directed to our Patent No. 1,432,513.

WHAT WE CLAIM IS:

1. A quartz crystal timepiece comprising time keeping means including a quartz crystal vibrator arranged to oscillate in the thickness-shear mode at resonant frequency between 1 MHz and 10 MHz for generating a standard time signal, and a digital display device driven by the time keeping means.

2. A timepiece as claimed in claim 1, including logic circuitry for adjusting the time-rate.

3. A timepiece as claimed in claim 2 in which the time keeping means includes a frequency divider circuit for producing a relatively low frequency output signal from the standard time signal, said logic circuitry being connected with the divider circuit and including a memory circuit operatively linked to the divider circuit by a gate circuit which, in operation is controlled by the said relatively low frequency output signal in dependence upon data stored in the memory circuit.

4. A timepiece as claimed in claim 3 in which the divider circuit, the gate circuit and the memory circuit each have the same number of stages, each stage of the memory circuit being connected to write memorize data into the corresponding stage of the divider circuit when the gate circuit is opened, means being provided for setting into the memory circuit a binary code representative of a predetermined



reliability of the oscillator circuit 11 is improved.

Next, the method of adjusting the time-rate of the timepiece of Figure 3 will be described.

The divider circuit 21 is a presettable down-count type divider composed of a plurality (n) of flip-flop stages $F/F_1, F/F_2 \dots F/F_n$ and is $\frac{1}{2^n}$ counter. Although the frequency f_1 of the output signal of the divider circuit 21 may be any desirable suitably required frequency it will be assumed, in what follows, to be 1 Hz exactly.

The gate circuit 23 has a plurality (n) of stages $g_1, g_2 \dots g_n$ and is controlled by a preset signal f_p generated from a preset signal generator 24 synchronously with the output signal from the divider circuit 21. When the preset signal f_p is generated, the gate circuit 23 causes data from a memory circuit 25, having a plurality (n) stages $m_1, m_2 \dots m_n$, to be written in the frequency divider 21. Because the divider circuit 21 is a downcount type divider for every pulse of the output signal from the oscillator circuit 11, (1, 0, 0, ... 0) is subtracted from the preset data in the divider circuit 21, and the data in the divider circuit 21 eventually becomes (0, 0, 0, ...). When this occurs an output pulse is generated by the divider circuit 21 and the preset signal f_p is generated by the generator 24. This action is repeated thereafter. The time-rate is adjusted, namely, the frequency f_1 is adjusted to be 1 Hz exactly by pre-setting the data in the memory 25.

Since the divider circuit 21 is $\frac{1}{2^n}$ counter, when the frequency f_0 is 2^n Hz, the frequency f_1 is inevitably exactly 1 Hz and the data in the memory 25 is (1, 1 ... 1). When the frequency f_0 is below 2^n Hz the period of the output signal from the divider circuit 21 becomes $(1 + \Delta T)$ seconds as shown in Figure 5. Accordingly, a binary code which is decreased by the equivalent of ΔT is written in the memory circuit 25. For example, if the period of the output signal of the divider circuit 21 is longer by the equivalent of two pulses of the output signal of the oscillator circuit 11, data (1, 0, 1, ... 1) is written into the memory circuit 25.

As illustration in Figure 6 data may be written into the memory 25 in the same manner as time correction, i.e. correction of the contents of the divider circuit 13. For example, suppose that the set value of each bit in the memory is to be 1001, 1000, 0111, the display device 15 is caused to display 987 by means of the correcting circuit 22, four bits corresponding to each digit. Thus the contents of the divider circuit 13 is the same as that which it is desired to set in the memory 25. The output of each bit in the divider circuit 13 is connected to the input of a corresponding bit of the memory, so that the contents of the divider circuit 13 are set into the memory 25 with timing f_1 .

The data in the memory circuit 25 disappears

when the power supply ceases, e.g. when a battery driving the timepiece is changed. The accuracy of adjustment of the time-rate is, it will be appreciated, proportional to the reciprocal of the frequency f_0 , so that the higher the frequency f_0 , the greater the accuracy of adjustment of the time-rate. Accordingly, if the frequency f_0 is between 1 MHz and 10 MHz the time-rate can be adjusted to an accuracy of 0.09 seconds to 0.01 seconds a day.

As the time-rate is adjusted by logic circuitry, the resonant frequency of the vibrator 9 is arbitrarily selected as long as it is below 2^n Hz. Consequently, it is possible to construct inexpensive and highly stable wrist-watches.

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2. A timepiece as claimed in claim 1, including logic circuitry for adjusting the time-rate.

3. A timepiece as claimed in claim 2 in which the time keeping means includes a frequency divider circuit for producing a relatively low frequency output signal from the standard time signal, said logic circuitry being connected with the divider circuit and including a memory circuit operatively linked to the divider circuit by a gate circuit which, in operation is controlled by the said relatively low frequency output signal in dependence upon data stored in the memory circuit.

4. A timepiece as claimed in claim 3 in which the divider circuit, the gate circuit and the memory circuit each have the same number of stages, each stage of the memory circuit being connected to write memorize data into the corresponding stage of the divider circuit. The gate circuit is opened, means being provided for setting into the memory circuit a binary code representative of a predetermined

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- period which thus determines the periodicity of said low frequency output signal.
5. A timepiece as claimed in claim 3 or 4 in which the divider circuit is a down-count type divider.
6. A quartz crystal timepiece substantially as herein described with reference to and as shown in Figures 3 to 6 of the accompanying

drawings.

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