CLAIMS

1. A semiconductor storage device comprising:

a memory string including a memory cell;

a bit line electrically connected to one end of the memory string; and

a sense amplifier electrically connected to the bit line, wherein

the sense amplifier comprises:

a first transistor, one end of which is connected to a first node on an electric current path of the bit line, and another end of which is electrically connected to a second node;

a second transistor electrically connected between the second node and a sense node; and

a third transistor, a gate of which is connected to the first node, and the third transistor being electrically connected between the second node and a third node whose voltage can be adjusted.

2. The semiconductor storage device according to claim 1, wherein

an electric current flows to the third node from the bit line through the first transistor and the third transistor, and thereafter, an electric current flows to the third node from the sense node through the second transistor and the third transistor during reading from the memory cell.

3. The semiconductor storage device according to claim 1, wherein

a gate voltage of the first transistor when an electric current flows to the third transistor from the bit line through the first transistor is a voltage obtained by adding a voltage at the third node, a threshold voltage of the first transistor, and a predetermined overdrive voltage, and

a gate voltage of the second transistor when an electric current flows to the third transistor from the sense node through the second transistor is a voltage obtained by adding a voltage at the third node, a threshold voltage of the second transistor, and thea predetermined overdrive voltage.

4. The semiconductor storage device according to claim 1, wherein

the gate of the third transistor in addition to a drain of the first transistor is connected to the first node, and

the third transistor operates as a diode when an electric current flows to the third transistor from the bit line through the first transistor and when an electric current flows to the third transistor from the sense node through the second transistor.

5. The semiconductor storage device according to claim 4, further comprising a fourth transistor connected to the first node on the electric current path of the bit line, wherein

an electric current flows to the third node from the bit line through the first transistor and the third transistor, and thereafter, an electric current flows to the third node from the sense node through the third transistor and the second transistor during reading from the memory cell.

6. The semiconductor storage device according to claim 5, wherein

the memory cell is a NAND-type flash memory cell,

the semiconductor storage device further comprising a NAND string including a~~the~~ plurality of NAND-type flash memories serially connected between the bit line and a first voltage setting node, and a select gate transistor, and

the fourth transistor is the select gate transistor.

7. The semiconductor storage device according to claim 5, wherein

the memory cell is a NAND-type flash memory cell,

the semiconductor storage device further comprising a NAND string including a~~the~~ plurality of NAND-type flash memories serially connected between the bit line and a first voltage setting node, and a select gate transistor, and

the fourth transistor is disposed on an electric current path between the bit line and the first transistor.

8. The semiconductor storage device according to claim 1, further comprising a fifth transistor configured to pass an electric current flowing from the bit line to the third node during data writing to the memory cell without passing through the first and second transistors.

9. The semiconductor storage device according to claim 1, further comprising a sixth transistor disposed between the third node and a second voltage setting node.

10. The semiconductor storage device according to claim 9, wherein

multiple-value data is written in the memory cell, and

in a case where data read from the memory cell by setting a word line of the memory cell to a predetermined read voltage level has predetermined logic, the sixth transistor continues to be turned off until read operation from the memory cell is completed.

11. The semiconductor storage device according to claim 1, wherein

the sense amplifier is capable of arbitrarily selecting between:

a first sensing manner for passing an electric current to the third node from the bit line through the first transistor and the third transistor and thereafter passing an electric current to the third node from the sense node through the second transistor and the third transistor during reading from the memory cell; and

a second sensing manner for making a voltage of the second node stable and thereafter passing an electric current to the bit line from the sense node through the second transistor and the first transistor during reading from the memory cell.

12. The semiconductor storage device according to claim 1, further comprising a voltage adjustment circuitry configured to adjust a voltage at the third node.

13. The semiconductor storage device according to claim 12, wherein

the voltage adjustment circuitry raises the voltage at the third node in a case where an ambient temperature rises.

14. The semiconductor storage device according to claim 12, wherein

the voltage adjustment circuitry lowers~~raises~~ the voltage at the third node ~~higher~~ as a distance from the memory string to be read out and the sense amplifier becomes longer.

15. The semiconductor storage device according to claim 12, wherein

the voltage adjustment circuitry raises the voltage at the third node higher as a threshold of the third transistor becomes lower.

16. The semiconductor storage device according to claim 12, further comprising a reference voltage generation circuitry configured to generate a reference voltage serving as a reference for the voltage at the third node, wherein

the voltage adjustment circuitry controls feedback such that the voltage at the third node matches the reference voltage.

17. The semiconductor storage device according to claim 16, wherein

the reference voltage generation circuitry includes:

an electric current source configured to generate an electric current in accordance with an electric current flowing to the memory string to be read out;

a resistance replica circuitry connected on an electric current path of the electric current source and having a resistance value in accordance with a resistance value of the bit line;

a diode replica circuitry connected between one end of the resistance replica circuitry and an output node of the reference voltage and simulating an electrical property of the third transistor; and

a feedback control circuitry configured to control feedback such that a voltage at a connection node between the electric current source and the resistance replica circuitry matches a predetermined threshold voltage.

18. The semiconductor storage device according to claim 17, wherein

the resistance replica circuitry is a variable resistor capable of changing the resistance value depending on a distance from the memory string to be read out and the sense amplifier.

19. A memory system comprising:

a semiconductor storage device having a memory string including a memory cell; a bit line electrically connected to one end of the memory string; a sense amplifier electrically connected to the bit line; and an internal controller configured to control the operation of the sense amplifier, in which the sense amplifier comprises: a first transistor, one end of which is connected to a first node on an electric current path of the bit line, and another end of which is electrically connected to a second node; a second transistor electrically connected between the second node and a sense node; and a third transistor, a gate of which is connected to the first node, and the~~which~~ third transistor being~~is~~ electrically connected between the second node and a third node whose voltage can be adjusted; and

an external controller configured to control data writing to the semiconductor storage device and data reading from the semiconductor storage device, wherein

based on an instruction from the external controller, the internal controller selects one of a first sensing manner for passing an electric current to the third node from the bit line through the first transistor and the third transistor and thereafter passing an electric current to the third node from the sense node through the second transistor and the third transistor during reading from the memory cell and

a second sensing manner for making a voltage of the second node stable and thereafter passing an electric current to the bit line from the sense

node through the second transistor and the first transistor during reading from the memory cell.

20. The memory system according to claim 19, wherein

the external controller instructs the semiconductor storage device to select the first sensing manner or the second sensing manner using a prefix command, bit value setting through Set Feature, or a parameter set.