WHAT IS CLAIMED IS:

1. A memory module comprising:

a plurality of first memory chips;

a plurality of second memory chips;

a controller configured to control an internal operation mode in which the memory module performs data communication between the plurality of first memory chips and the plurality of second memory chips; and

a plurality of data buffers corresponding to the plurality of second memory chips, respectively,

wherein the controller is configured to control the internal operation mode such that during the internal operation mode, the memory module performs internal data (DQ) termination on an internal data path, connecting the plurality of data buffers with the plurality of second memory chips; and

wherein each of the plurality of data buffers comprise,

a first end for receiving data to be written to a respective second memory chip of the plurality of second memory chips,

a second end for transmitting data to be written to the respective second memory chip, and

an input buffer and an output buffer between the first end and the second end,

wherein the second end is included in the internal data path during the internal operation mode.

2. The memory module of claim 1, wherein

each of the plurality of data buffers comprises an on-die-termination (ODT) circuit connected to the internal data path, and

the ODT circuit is configured to selectively provide the internal DQ termination.

3. The memory module of claim 2, wherein the ODT circuit comprises:

a switch having a first end connected to the internal data path, and the switch is configured to respond to an ODT control signal of the controller; and

a resistor connected between a second end of the switch and a ground voltage.

4. The memory module of any one of claims 1 to 3, wherein the controller is configured to perform the internal operation mode based on an internal operation mode command received from an external device of the memory module.

5. The memory module of any one of claims 1 to 4, wherein the plurality of first memory chips include nonvolatile memory devices.

6. The memory module of any one of claims 1 to 5, wherein the plurality of second memory chips include volatile memory devices.

7. The memory module of any one of claims 1 to 6, wherein the memory module includes a nonvolatile dual inline memory module (NVDIMM).

8. A memory system comprising:

a first memory module connected to a data bus, the first memory module being a target memory module accessible by an external device of the memory system; and

a second memory module connected to the data bus, the second memory module being a non-target memory module not accessed by the external device,

wherein the second memory module is configured to perform internal data (DQ) termination on an internal data path, during an internal operation mode in which the second memory module performs data communication by using the internal data path of the second memory module; and

wherein the second memory module comprises:

a plurality of first memory chips;

a plurality of second memory chips;

a plurality of data buffers corresponding to the plurality of second memory chips, respectively,

wherein each of the plurality of data buffers comprise,

a first end for receiving data to be written to a respective second memory chip of the plurality of second memory chips,

a second end for transmitting data to be written to the respective second memory chip, and

an input buffer and an output buffer between the first end and the second end,

wherein the second end is included in the internal data path during the internal operation mode.

9. The memory system of claim 8, wherein the second memory module is configured to start the internal operation mode based on an internal operation mode enter command received from the external device, and is configured to end the internal operation mode based on an internal operation mode exit command received from the external device .

10. The memory system of claim 9, wherein the second memory module is configured to perform the internal DQ termination between a first time in which the internal operation mode enter command is received and a second time in which the internal operation mode exit command is received.

11. The memory system of any one of claims 8 to 10, wherein the second memory module is configured to perform the internal DQ termination in correspondence to each of read commands issued during the internal operation mode based on an internal operation mode command received from the external device.

12. The memory system of any one of claims 8 to 11, wherein the second memory module further comprises:

a controller configured to control the internal operation mode such that during the internal operation mode, the second memory module is configured to perform the internal DQ termination on the internal data path connecting the plurality of first memory chips with the plurality of second memory chips.

13. The memory system of any one of claims 8 to 12,

wherein each of the plurality of data buffers includes,

a first on-die-termination (ODT) circuit connected to the data bus, and

a second ODT circuit connected to the internal data path,

wherein the second ODT circuit is configured to selectively provide the internal DQ termination.

14. The memory system of claim 13, wherein the first ODT circuit comprises:

a first switch having a first end connected to the data bus, and responding to a first ODT control signal of the controller; and

a first resistor connected between a second end of the first switch and a ground voltage.

15. The memory system of claim 13 or claim 14, wherein the second ODT circuit comprises:

a second switch having an end connected to the internal data path, and responding to a second ODT control signal of the controller; and

a second resistor connected between the other end of the second switch and a ground voltage.

16. The memory system of any one of claims 8 to 15, wherein the plurality of first memory chips include nonvolatile memory devices.

17. The memory system of any one of claims 8 to 16, wherein the plurality of second memory chips include volatile memory devices.

18. The memory system of any one of claims 8 to 17, wherein the first and second memory modules include homogeneous nonvolatile dual inline memory modules (NVDIMMs).

19. The memory system of any one of claims 8 to 18, wherein the first and second memory modules include heterogeneous nonvolatile dual inline memory modules (NVDIMMs).

20. An operating method of a memory system, the operating method comprising:

accessing a first memory module of the memory system through an external device of the memory system;

performing an internal operation mode by using an internal data path, in a second memory module of the memory system, the second memory module not being accessed by the external device; and

performing internal data (DQ) termination on the internal data path, during the internal operation mode of the second memory module;

wherein the second memory module comprises:

a plurality of first memory chips;

a plurality of second memory chips;

a plurality of data buffers corresponding to the plurality of second memory chips, respectively,

wherein each of the plurality of data buffers comprise,

a first end for receiving data to be written to a respective second memory chip of the plurality of second memory chips,

a second end for transmitting data to be written to the respective second memory chip, and

an input buffer and an output buffer between the first end and the second end,

wherein the second end is included in the internal data path during the internal operation mode.