

DYNAMIC RANDOM ACCESS MEMORY ARRAY

This invention relates to a dynamic random access memory (DRAM) cell and more particularly to the bit line array of a DRAM.

Recently, the semiconductor industry has made enormous efforts to fabricate DRAMs of high bit densities and many successes have been achieved. In particular, mass production of the 1 Mbit DRAM is already being achieved, by virtue of the successful development of a new fabrication process.

However, many technical problems emerge as the bit density of memory devices increase. The necessity of fabrication of memory cells of high bit density on a small chip area requires not only that the dimension of the cell be reduced, but also the separation between bit lines connected to the memory cell and the separation between the memory cell array and peripheral circuits also have to be reduced.

The fringing effect of the semiconductor memory system, due to the reduced separation between bit lines and peripheral circuits, has a severe influence on the operation tolerances of the memory because of the capacitive unbalance between bit lines.

There is a possibility that data sensing may fail due to the unbalance between bit lines, because the DRAM system involves the detection of data through the mechanism of charge sharing.

It is possible that minority carriers are generated in the peripheral circuitry and injected into the storage capacitor of the memory cell, thereby discharging the stored data signal.

A protection means for protecting a memory cell array from these phenomena is disclosed in U.S. Patent No. 4,339,766.

This device is composed of a pair of dummy columns for the protection of the memory cell array from the peripheral circuitry. The dummy columns are composed of a plurality of one-transistor cells with capacitors which have alternately large and small capacitances. The memory cells may also have logic 1's and 0's stored alternately.

This device however presents certain complicated disadvantages and also the size of the device has to be taken into consideration.

Referring to Figure 1, there is shown the memory cell array diagram of a conventional DRAM, comprising: well-known sense amplifiers 10, bit line pairs (column lines) $\overline{BLo}$, $\overline{BLo}$ to BLi , $\overline{BLi}$ connected to respective sense amplifiers, word lines WLo to WLi , and integrated memory cells 11 connected between said bit lines and

word lines. The memory cells are of the 1-transistor memory cell type, comprising a transistor and a storage capacitor.

The bit line is a long conducting layer connected to many memory cells and has its own parasitic capacitance developed between the semiconductor substrate and the bit line itself.

There is also a parasitic capacitance due to the fringing effect developed between each bit line and adjacent bit lines. For example, all of bit lines $\overline{BLo}$ to $\overline{BLi}$ except the outermost bit lines $\overline{BLo}$ and $\overline{BLi}$ have a self capacitance C_B constituted by the bit line itself and a mutual capacitance C_f caused by the fringing effects, as shown in Figure 1.

Therefore the total capacitance of each bit line $\overline{BLo}$ to $\overline{BLi}$ is $C_B + 2C_f$. But, since the outermost bit lines $\overline{BLo}$ and $\overline{BLi}$ have only one adjacent bit line, their total capacitance is, in both cases, $C_B + C_f$.

In these circumstances, there is the possibility that the sense amplifier which detects the data through the difference of the stored charges between a bit line pair (such as $\overline{BLo}$ and $\overline{BLo}$, $\overline{BLl}$ and $\overline{BLl}$ or $\overline{BLi}$ and $\overline{BLi}$) may malfunction when it senses data for the outermost bit lines. That is to say, the outermost sense amplifier may not be able to detect data properly due to the capacitive unbalance between the bit lines. That is, because of the fact that the outermost bit lines $\overline{BLo}$

and $\overline{\text{BLi}}$ each have a capacitance of $C_B + C_f$ and in contrast, the bit lines $\overline{\text{BLo}}$ and BLi each have a capacitance of $C_B + 2C_f$. This potential data detection problem can be easily understood when one considers that the sense amplifier is composed of a bistable flip-flop. The inner sense amplifiers, that is all except the outermost sense amplifiers, do not exhibit this failure in data detection, because all associated bit lines have an equal capacitance value namely, $C_B + 2C_f$.

In reality, a single power supply voltage V_{cc} of 5 volts is used in recent DRAM systems, for TTL compatibility. The sense amplifier 10 precharges the bit lines to 5 volts and senses the voltage difference between bit lines resulting from charge sharing with the storage capacitor of the memory cell selected by the addressed word line during an active cycle.

For a DRAM which operates at this low voltage level a high performance sense amplifier, which can detect a difference of the order of several tens of milli-volts between bit lines, should be used in order to achieve successful read-out of the data stored in the memory cell. Therefore since the value of said mutual capacitance C_f increases as the separation between the bit lines is reduced, for the higher density DRAMs the memory cells associated with the outermost bit lines malfunction due to the unbalance of the aforesaid capacitances.

Thus, the present invention seeks to provide an improved memory cell array which can avoid the problems in the known memory cells resulting from the outermost bit lines and the fringing effect.

In addition, the present invention seeks to provide an improved memory cell array which can avoid the destruction of the stored data due to minority carriers being injected into the memory cell from the peripheral circuitry.

According to the present invention, there is provided a DRAM memory cell array comprising: bit lines connected to a column decoder; word lines connected to a row decoder; memory cells for data storage connected between said bit lines and said word lines; and sense amplifiers for detection of data stored in said memory cells by the selection of an address by said column and row decoders; characterised by a respective dummy bit line positioned at each end of said memory cell array, the dummy bit lines being free from connections to any of the sense amplifiers.

Embodiments of the present invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram of the memory cell array of a conventional DRAM;

Figure 2 is a block diagram of a DRAM according to an embodiment of the present invention;

Figure 3 is a circuit diagram of a memory cell array according to an embodiment of the present invention; and

Figure 4 shows the layout of the memory cell array of Figure 3.

Referring to Figure 2 there is shown a DRAM chip which embodies the present invention. The memory chip 1 in this example is a 1M bit dynamic RAM composed of 4 blocks of 265K memory cell arrays 2a-2d which have dummy bit lines 3 at the outermost side of each block. Each block includes 512 rows (or word lines) and 512 columns (or bit lines) and these row and column lines are connected to a row decoder 6 and respective sense amplifier 4. Said column line is also connected to a column decoder 5. Each memory cell array block contains 512 sense amplifiers which are connected to the bit lines.

The peripheral circuitry (such as the clock generator address buffer for driving the row and column decoders 6,5, said memory cells array 2a-2d and the sense amplifier, and I/O buffer) is located in the external block 7 surrounding said memory cell array. The dummy bit lines 3 are not connected with the sense amplifiers 4.

It should be noted that said dummy bit lines 3 may be connected with the semiconductor substrate, to ground, or may be connected to a finite bias voltage.

Figure 3 shows a circuit diagram of a DRAM memory cell according to the present invention. Bit lines 40

are connected to sense amplifiers 10. Memory cells 11 are connected alternately to the word lines 50 in the folded bit line method, as is conventional. According to this invention, dummy bit lines 3 are positioned at each end of said memory cell array in addition to said conventional memory. The dummy bit lines (DBL) are not connected to any of the sense amplifiers 10. However, memory cells are connected, using the folded bit line method, to said dummy bit lines 3 and to the word lines 50. The memory cells 11 are of the 1-transistor memory cell type comprising one MOS transistor 30 and one storage capacitor 31, as is conventional. The source electrode 34 of each MOS transistor 30 is connected to the bit line 40 or dummy bit line 3. The drain electrode 33 is connected to electrode 35 which is fabricated on the surface of the semiconductor substrate by ion-implantation or inversion and connected to the storage capacitor 31, which is of gated capacitance. The other electrode 36 of said storage capacitor 31 is connected by a second polysilicon layer to the semiconductor substrate (ground) or to the power supply voltage V_{cc} .

The semiconductor region of the storage capacitor 31 connected to said drain 33 is the surface region of the semiconductor substrate under a dielectric insulator, which is itself under said second polysilicon layer. It is a well known fact that this region may be

ion-implanted using a dopant of opposite conductivity type to said semiconductor substrate or may be composed of an inversion layer, established by the power supply voltage V_{cc} being applied to electrode 36.

The gate of the MOS transistor 30 of each memory cell 11 is a polysilicon gate which is connected to a word line 50.

Each bit line 40, excluding the dummy bit lines 3, has a total capacitance of $C_B + 2C_f$, where C_B is its own parasitic capacitance and C_f is the parasitic capacitance due to the fringing effect between the adjacent bit lines. Therefore the bit lines adjacent to the dummy bit lines 3 do not cause an unbalance between the capacitive values and therefore the outermost sense amplifiers can function correctly.

It should be noted that the dummy bit lines 3, positioned at each end of the memory cell array are fabricated in the same process step and with the same dimensions as the usual bit lines 40.

Figure 4 is an enlarged view of a very small part of the memory cell array, showing the layout of a part of the arrangement shown in Figure 3. Various modifications of the disclosed layout, within the scope of the present invention, will be readily apparent to persons skilled in the art.

Reference numerals common to Figures 3 and 4 designate the same features in both Figures.

The dummy bit lines 3, positioned at the edge of the memory cell array, and bit lines 40 are made from a metal conducting layer. They are connected to the high concentration N type layer 100 on the P type substrate through openings 60.

The polysilicon word lines 50, isolated from said bit lines 40 by the insulation layer, provide the gates of the MOS transistors 30.

The MOS transistors 30 have gate oxides under said bit lines 40 with the channel region of each MOS transistor 30 being under the gate oxides. The N type region 35 on the surface of semiconductor substrate forms one electrode of the storage capacitor 31 and is connected to the drain of the respective transistor. Said semiconductor region 34 forms the source region of each transistor 30 and is connected to the bit line 40 or dummy bit line 3 through opening 60.

The dielectric insulation layer of the storage capacitor 31 is formed on said region 35. The second polysilicon layer, not shown, is provided on the dielectric insulation layer and is connected to the semiconductor substrate.

The word line 50 is connected to the row decoder, which is not shown in Figure 4, and the bit line 40 is connected to the sense amplifier 10 and the column decoder, which also is not shown in this Figure.

The dummy bit line 3 is connected to the semiconductor substrate but is not connected to the sense amplifier 10. Therefore, the memory cells connected to the dummy bit lines 3 do not store data.

However, a finite bias voltage may be applied to the dummy bit lines 3. In this case, said bias voltage forms a depletion layer at the interface between the P type semiconductor region and N type semiconductor region 100, through opening 60, and collects the minority carriers (in this case, electrons) generated in the external circuitry of said memory cell array. Hence, destruction of data stored on the storage capacitors 31 located at the edge of the memory cell array, as a result of said minority carriers, can be prevented.

As explained hereinabove, the device disclosed in U.S. Patent 4,339,766 must employ a pair of dummy columns (two bit lines) with a plurality of one-transistor cells having alternating large and small capacitors. In contrast, a memory cell array according to this invention can be provided with only half dummy columns (one bit line).

As explained above, the extra bit lines positioned at each end of the conventional memory cell array, in accordance to this invention, result in the advantage not only of prevention of the unbalance in the charging voltage of the bit lines connected to the sense amplifier, but also the prevention of malfunction of

memory cells which can be caused by minority carriers generated in the external circuitry.

The invention is not limited to the examples described hereinabove. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will be readily apparent to persons skilled in the art upon reference to the above description of this invention. Any such modifications or embodiments are intended to fall within the scope of the invention, as defined by the appended claims.

Claims:-

1. A DRAM memory cell array comprising: bit lines connected to a column decoder; word lines connected to a row decoder; memory cells for data storage connected between said bit lines and said word lines; and sense amplifiers for detection of data stored in said memory cells by the selection of an address by said column and row decoders; characterised by a respective dummy bit line positioned at each end of said memory cell array, the dummy bit lines being free from connections to any of the sense amplifiers.
2. A memory cell array as claimed in claim 1, characterised in that said dummy bit lines are connected to ground by connection to a semiconductor substrate of the array.
3. A memory cell array as claimed in claim 1, characterised in that the dummy bit lines are connected to have a finite bias voltage applied thereto.
4. A memory cell array substantially as hereinbefore described with reference to and as illustrated in Figures 2 to 4 of the accompanying drawings.

