WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor memory device, comprising:

a peripheral logic structure on a semiconductor substrate;

a horizontal semiconductor layer on the peripheral logic structure and including a cell array region and a connection region;

electrode structures extending in a first direction on the horizontal semiconductor layer and spaced apart in a second direction intersecting the first direction, a pair of the electrode structures adjacent to each other being symmetrically disposed to define a contact region partially exposing the horizontal semiconductor layer; and

a through via structure on the contact region and connecting the electrode structures to the peripheral logic structure,

wherein each of the electrode structures comprises a plurality of gate insulation regions extending along the first direction on the connection region, the gate insulation regions having different lengths from each other in the first direction.

2. The device of claim 1, wherein portions of the gate insulation regions extend in the second direction and surround at least a portion of the through via structure.

3. The device of claim 1 or claim 2, wherein the gate insulation regions extend along paths that are parallel to each other.

4. The device of any one of claims 1 to 3, wherein each of the electrode structures has a first part having a first width and a second part having a second width less than the first width,

wherein the first parts of the electrode structures are adjacent in the first direction

to the through via structure, and the second parts of the electrode structures are adjacent in the second direction to the through via structure.

5. The device of any one of claims 1 to 4, wherein each of the electrode structures further comprises:

a plurality of ground select lines spaced apart from each other in the second direction at a same level from the horizontal semiconductor layer as each other; and

a plurality of word lines vertically stacked on the plurality of ground select lines,

wherein each of the word lines overlaps the plurality of ground select lines, when viewed in a plan view.

6. The device of any one of claims 1 to 5, wherein the through via structure comprises:

a through insulation pattern extending in a third direction perpendicular to a top surface of the horizontal semiconductor layer and penetrating the horizontal semiconductor layer;

through plugs penetrating the through insulation pattern and connected to the peripheral logic structure;

contact plugs connected to the electrode structure; and

conductive lines connecting the through plugs to the contact plugs.

7. A three-dimensional semiconductor memory device, comprising:

a peripheral logic structure on a semiconductor substrate;

a horizontal semiconductor layer on the peripheral logic structure and including a cell array region and a connection region;

electrode structures extending in a first direction on the horizontal semiconductor

layer and spaced apart in a second direction intersecting the first direction, a pair of the electrode structures adjacent to each other being symmetrically disposed to define a contact region partially exposing the horizontal semiconductor layer; and

a through via structure penetrating the electrode structures and the horizontal semiconductor layer, the through via structure connecting the electrode structures to the peripheral logic structure,

wherein each of the electrode structures comprises:

first gate insulation regions extending in the first direction on the cell array region and spaced apart from each other in the second direction at a first interval; and

second gate insulation regions extending in the first direction on the connection region and spaced apart from each other in the second direction at a second interval less than the first interval.

8. The device of claim 7, wherein portions of the second gate insulation regions extend in the second direction and surround at least a portion of the through via structure.

9. The device of claim 7 or claim 8, wherein

each of the electrode structures has a first part having a first width and a second part having a second width less than the first width, and

the through via structure is disposed between the second parts of the electrode structures, when viewed in a plan view.

10. The device of any one of claims 7 to 9, wherein the second gate insulation regions are spaced apart in the first direction from the first gate insulation regions, and

wherein each of the electrode structures further comprises:

a plurality of ground select gate electrodes spaced apart from each other in the second direction at a same level from the horizontal semiconductor layer; and

gate openings provided between adjacent ones of the ground select gate electrodes in the second direction and between the first gate insulation regions and the second gate insulation regions in the first direction.

11. The device of any one of claims 7 to 10, wherein the second gate insulation regions of each of the electrode structures have different lengths from each other in the first direction.

12. The device of any one of claims 7 to 11, wherein each of the electrode structures further comprises:

a plurality of ground select lines spaced apart from each other in the second direction at a same level from the horizontal semiconductor layer; and

a plurality of word lines vertically stacked on the plurality of ground select lines,

wherein each of the word lines overlaps the plurality of ground select lines, when viewed in a plan view.

13. The device of claim 12, wherein each of the word lines comprises:

electrode portions extending in the first direction on the cell array region and having a first width;

first pad portions extending in the first direction on the connection region and having a second width less than the first width;

second pad portions extending in the second direction and connected to the electrode portions and the first pad portions; and

an electrode connection portion extending in the second direction and connecting

the plurality of electrode portions to each other.

14. The device of any one of claims 7 to 13, wherein the through via structure comprises:

a through insulation pattern extending in a third direction perpendicular to a top surface of the horizontal semiconductor layer and penetrating the horizontal semiconductor layer;

through plugs penetrating the through insulation pattern and connected to the peripheral logic structure;

contact plugs connected to the electrode structures; and

conductive lines connecting the through plugs to the contact plugs.

15. A three-dimensional semiconductor memory device, comprising:

a peripheral logic structure on a semiconductor substrate;

a horizontal semiconductor layer on the peripheral logic structure and including a cell array region and a connection region; and

electrode structures extending in a first direction on the horizontal semiconductor layer and spaced apart in a second direction intersecting the first direction, a pair of the electrode structures adjacent to each other being symmetrically disposed to define a contact region between the second parts of the electrode structures, the contact region partially exposing the horizontal semiconductor layer,

wherein each of the electrode structures comprises:

first gate insulation regions extending in the first direction on the cell array region and spaced apart from each other at a first interval;

second gate insulation regions spaced apart from the first gate insulation regions and extending in the first direction on the connection region, wherein the second

gate insulation regions are spaced apart from each other at a second interval less than the first interval; and

gate openings provided between ground select gate electrodes in the second direction and between the first gate insulation regions and the second gate insulation regions in the first direction, wherein the ground select gate electrodes are spaced apart from each other in the second direction at a same level from the horizontal semiconductor layer.

16. The device of claim 15, wherein the second gate insulation regions have different lengths from each other in the first direction.

17. The device of claim 15 or claim 16, wherein each of the electrode structures has a first part having a first width and a second part having a second width less than the first width.

18. The device of any one of claims 15 to 17, further comprising a through via structure between portions of a pair of the electrode structures adjacent to each other on the connection region and connecting the electrode structures to the peripheral logic structure,

wherein portions of the second gate insulation regions extend in the second direction and at least partially surround the through via structure.

19. The device of claim 18, wherein the through via structure comprises:

a through insulation pattern extending in a third direction perpendicular to a top surface of the horizontal semiconductor layer and penetrating the horizontal semiconductor layer;

through plugs penetrating the through insulation pattern and connected to the peripheral logic structure;

contact plugs connected to the electrode structures; and

conductive lines connecting the through plugs to the contact plugs.

20. The device of claim 18 or claim 19, wherein the electrode structure has a lower stepwise structure, an intermediate stepwise structure, and an upper stepwise structure sequentially provided along the first direction, and

wherein the through via structure is adjacent to the lower and upper stepwise structures in the first direction and is adjacent to the intermediate stepwise structure in the second direction.