

Abstract

Provided is a method for manufacturing a semiconductor device suitable for achieving low wiring resistance between semiconductor elements that is bonded via an adhesive layer and multi-layered. The method according to the present invention is as follows. First, a wafer laminate (W) is prepared, the wafer laminate (W) including a wafer (10) having a circuit forming surface (10a), a wafer (20) having a main surface (20a) and a back surface (20b), and an adhesive layer (30) containing an SiOC-based polymer. Then, a hole (H) is formed in the wafer laminate (W) by etching the wafer laminate (W) from the wafer (20) side via a mask pattern masking a portion of the main surface (20a) side of the wafer (20), the hole (H) extending through the wafer (20) and the adhesive layer (30) and reaching a wiring pattern (12b) in the wafer (10). Then, an insulating film (41) is formed on an inner surface of the hole (H). Then, the insulating film (41) on a bottom surface of the hole (H) is removed. Then, the wafer laminate (W) is subjected to a cleaning treatment (an oxygen plasma treatment and/or an Ar sputtering treatment). Then, a conductive portion is formed in the hole (H).

[Figure 2]