Claims

1. A method of making a semiconductor device, comprising:

providing a semiconductor die including a plurality of interconnect structures formed over a surface of the semiconductor die;

providing a substrate;

forming a plurality of conductive traces with interconnect sites disposed at intermediate locations along a length of the conductive traces over the substrate with the conductive traces extending in opposite directions from the interconnect sites;

forming a plurality of individual non-conductive masking patches over an area of the substrate interstitial between and physically separated from the interconnect sites, wherein the interconnect structures including a width substantially the same as a width of the conductive traces away from the interconnect sites and wider than the interconnect sites;

bonding the interconnect structures to the interconnect sites absent a mask opening so that the interconnect structures cover a top surface and side surfaces of the interconnect sites; and

depositing an encapsulant around the interconnect structures between the semiconductor die and substrate.

2. The method of claim 1, further including bonding the interconnect structures to the interconnect sites under pressure or reflow temperature.

3. The method of claim 1, further including forming a masking layer over an area of the substrate away from the interconnect sites.

4. The method of claim 1, wherein the interconnect structures include bumps or bump material.

5. The method of claim 1, wherein the interconnect structures include a fusible portion and non-fusible portion.

6. The method of claim 1, wherein the interconnect structures include a conductive pillar and bump formed over the conductive pillar.

7. The method of claim 1, further including forming asperities over the interconnect sites or interconnect structures.

8. A method of making a semiconductor device, comprising:

providing a semiconductor die including an interconnect structure formed over a surface of the semiconductor die;

providing a substrate;

forming a conductive trace with an interconnect site disposed at an intermediate location along the conductive trace over the substrate with the conductive trace extending in opposite directions from the interconnect site, the interconnect site being narrower than the interconnect structure;

forming a plurality of individual non-conductive masking patches over an area of the substrate interstitial around and physically separated from the interconnect site; and

bonding the interconnect structure to the interconnect site absent a mask opening so that the interconnect structure covers a top surface and side surfaces of the interconnect site.

9. The method of claim 8, further including bonding the interconnect structure to the interconnect site under pressure or reflow temperature.

10. The method of claim 8, further including depositing an encapsulant around the interconnect structure between the semiconductor die and substrate.

11. The method of claim 10, further including forming a masking layer over an area of the substrate away from the interconnect site.

12. The method of claim 11, wherein the masking layer forms a dam to block the encapsulant from extending beyond a footprint of the semiconductor die.

13. The method of claim 8, wherein the interconnect structure includes a fusible portion and non-fusible portion.

14. The method of claim 8, further including forming asperities over the interconnect site or interconnect structure.

15. A semiconductor device, comprising:

a semiconductor die including a plurality of interconnect structures formed over a surface of the semiconductor die;

a substrate;

a plurality of conductive traces with interconnect sites disposed at intermediate locations along a length of the conductive traces formed over the substrate with the conductive traces extending in opposite directions from the interconnect sites, the interconnect sites including a width substantially the same as a width of the conductive traces away from the interconnect sites and narrower than the interconnect structures to increase interconnect density;

a plurality of individual non-conductive masking patches formed over an area of the substrate interstitial between and physically separated from the interconnect sites, wherein the interconnect structures are bonded to the interconnect sites so that the interconnect structures cover a top surface and side surfaces of the interconnect sites; and

an encapsulant deposited around the interconnect structures between the semiconductor die and substrate.

16. The semiconductor device of claim 15, wherein the interconnect structures are bonded to the interconnect sites under pressure or reflow temperature.

17. The semiconductor device of claim 15, wherein the interconnect structures include a fusible portion and non-fusible portion.

18. The semiconductor device of claim 15, wherein the interconnect structures include a conductive pillar and bump formed over the conductive pillar.

19. The semiconductor device of claim 15, further including asperities formed over the interconnect sites or interconnect structures.

20. A semiconductor device, comprising:

a substrate;

a conductive trace with an interconnect site disposed at an intermediate location along the conductive trace formed over the substrate with the conductive trace extending in opposite directions from the interconnect site;

a plurality of individual non-conductive masking patches formed over an area of the substrate interstitial around and physically separated from the interconnect site;

a semiconductor die including an interconnect structure formed over a surface of the semiconductor die with the interconnect structure bonded to the interconnect site absent a mask opening so that the interconnect structure covers a top surface and side surfaces of the interconnect site; and

an encapsulant deposited around the interconnect structure between the semiconductor die and substrate.

21. The semiconductor device of claim 20, wherein the interconnect structure is bonded to the interconnect site under pressure or reflow temperature.

22. The semiconductor device of claim 20, wherein a masking layer is formed over an area of the substrate away from the interconnect site.

23. The semiconductor device of claim 20, wherein the interconnect structure includes a bump or bump material.

24. The semiconductor device of claim 20, wherein the interconnect structure includes a fusible portion and non-fusible portion.

25. The semiconductor device of claim 20, wherein the interconnect structure includes a conductive pillar and bump formed over the conductive pillar.

26. A semiconductor device, comprising:

a substrate;

a conductive trace with an interconnect site disposed at an intermediate location along a length of the conductive trace formed over the substrate;

a plurality of individual non-conductive masking patches formed over an area of the substrate interstitial around and physically separated from the interconnect site; and

a semiconductor die including an interconnect structure formed over a surface of the semiconductor die with the interconnect structure covering a top surface and side surfaces of the interconnect site.

27. The semiconductor device of claim 26, wherein the interconnect structure is bonded to the interconnect site under pressure or reflow temperature.

28. The semiconductor device of claim 26, wherein a masking layer is formed over an area of the substrate away from the interconnect site.

29. The semiconductor device of claim 26, wherein the interconnect structure includes a bump or bump material.

30. The semiconductor device of claim 26, wherein the interconnect structure includes a fusible portion and non-fusible portion.

31. A semiconductor device, comprising:

a substrate;

a conductive trace including an interconnect site formed over the substrate, the interconnect site including a width substantially equal to a width of the conductive trace away from the interconnect site;

a plurality of individual non-conductive masking patches formed over an area of the substrate interstitial around and physically separated from the interconnect site; and

a semiconductor die including an interconnect structure disposed over the interconnect site.

32. The semiconductor device of claim 31, further including a plurality of asperities formed over the interconnect structure.

33. The semiconductor device of claim 31, further including an opening formed in the conductive trace.

34. The semiconductor device of claim 33, further including the interconnect structure disposed within the opening.

35. The semiconductor device of claim 31, wherein the interconnect structure includes a tip narrower than a body of the interconnect structure and the conductive trace deforms around the tip.